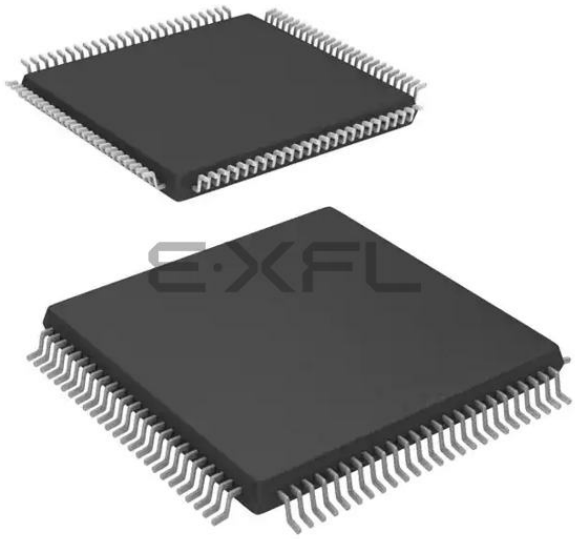

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38344wwv

Item	Description
Power-down modes	• Seven power-down modes • Sleep (high-speed) mode • Sleep (medium-speed) mode • Standby mode • Watch mode • Subsleep mode • Subactive mode • Active (medium-speed) mode
Memory	Large on-chip memory • H8/3842R, H8/38342, H8/38442: 16-Kbyte ROM, 1-Kbyte RAM • H8/3843R, H8/38343, H8/38443: 24-Kbyte ROM, 1-Kbyte RAM • H8/3844R, H8/3844S, H8/38344, H8/38444: 32-Kbyte ROM, 2-Kbyte RAM • H8/3845R, H8/3845S, H8/38345, H8/38445: 40-Kbyte ROM, 2-Kbyte RAM • H8/3846R, H8/3846S, H8/38346, H8/38446: 48-Kbyte ROM, 2-Kbyte RAM • H8/3847R, H8/3847S, H8/38347, H8/38447: 60-Kbyte ROM, 2-Kbyte RAM
I/O ports	84 pins • 71 I/O pins • 13 input pins

Item	Description
Timers	Six on-chip timers • Timer A: 8-bit timer Count-up timer with selection of eight internal clock signals divided from the system clock (ϕ)* and four clock signals divided from the watch clock (ϕw)* • Asynchronous event counter: 16-bit timer — Count-up timer able to count asynchronous external events independently of the MCU's internal clocks • Timer C: 8-bit timer — Count-up/down timer with selection of seven internal clock signals or event input from external pin — Auto-reloading • Timer F: 16-bit timer — Can be used as two independent 8-bit timers — Count-up timer with selection of four internal clock signals or event input from external pin — Provision for toggle output by means of compare-match function • Timer G: 8-bit timer — Count-up timer with selection of four internal clock signals — Incorporates input capture function (built-in noise canceler) • Watchdog timer — Reset signal generated by overflow of 8-bit counter
Serial communication interface	Three serial communication interface channels on chip • SCI1: Synchronous serial interface Choice of 8-bit or 16-bit transfer data • SCI3-1: 8-bit synchronous/asynchronous serial interface Incorporates multiprocessor communication function • SCI3-2: 8-bit synchronous/asynchronous serial interface Incorporates multiprocessor communication function
14-bit PWM	Pulse-division PWM output for reduced ripple • Can be used as a 14-bit D/A converter by connecting to an external low-pass filter.

6. Wakeup Interrupt Request Register (IWPR)

Bit	7	6	5	4	3	2	1	0
	IWPF7	IWPF6	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * All bits can only be written with 0, for flag clearing.

IWPR is an 8-bit read/write register containing wakeup interrupt request flags. When one of pins $\overline{WKP}_7$ to $\overline{WKP}_0$ is designated for wakeup input and a rising or falling edge is input at that pin, the corresponding flag in IWPR is set to 1. A flag is not cleared automatically when the corresponding interrupt is accepted. Flags must be cleared by writing 0.

Bits 7 to 0: Wakeup interrupt request flags (IWPF7 to IWPF0)

Bit n IWPFn	Description
0	Clearing condition: (initial value) When IWPFn= 1, it is cleared by writing 0
1	Setting condition: When pin $\overline{WKP}$n is designated for wakeup input and a rising or falling edge is input at that pin

(n = 7 to 0)

7. Wakeup Edge Select Register (WEGR)

Bit	7	6	5	4	3	2	1	0
	WKEGS7	WKEGS6	WKEGS5	WKEGS4	WKEGS3	WKEGS2	WKEGS1	WKEGS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WEGR is an 8-bit read/write register that specifies rising or falling edge sensing for pins $\overline{WKP}$n.

WEGR is initialized to H'00 by a reset.

Table 3.5 Conditions Under which Interrupt Request Flag is Set to 1

Interrupt Request Flags Set to 1		Conditions
IRR1	IRRI4	When PMR1 bit IRQ4 is changed from 0 to 1 while pin $\overline{IRQ_4}$ is low and IEGR bit IEG4 = 0.
		When PMR1 bit IRQ4 is changed from 1 to 0 while pin $\overline{IRQ_4}$ is low and IEGR bit IEG4 = 1.
	IRRI3	When PMR1 bit IRQ3 is changed from 0 to 1 while pin $\overline{IRQ_3}$ is low and IEGR bit IEG3 = 0.
		When PMR1 bit IRQ3 is changed from 1 to 0 while pin $\overline{IRQ_3}$ is low and IEGR bit IEG3 = 1.
	IRRI2	When PMR1 bit IRQ2 is changed from 0 to 1 while pin $\overline{IRQ_2}$ is low and IEGR bit IEG2 = 0.
		When PMR1 bit IRQ2 is changed from 1 to 0 while pin $\overline{IRQ_2}$ is low and IEGR bit IEG2 = 1.
	IRRI1	When PMR1 bit IRQ1 is changed from 0 to 1 while pin $\overline{IRQ_1}$ is low and IEGR bit IEG1 = 0.
		When PMR1 bit IRQ1 is changed from 1 to 0 while pin $\overline{IRQ_1}$ is low and IEGR bit IEG1 = 1.
	IRRI0	When PMR3 bit IRQ0 is changed from 0 to 1 while pin $\overline{IRQ_0}$ is low and IEGR bit IEG0 = 0.
		When PMR3 bit IRQ0 is changed from 1 to 0 while pin $\overline{IRQ_0}$ is low and IEGR bit IEG0 = 1.
IWPR	IWPF7	When PMR5 bit WKP7 is changed from 0 to 1 while pin $\overline{WKP_7}$ is low.
	IWPF6	When PMR5 bit WKP6 is changed from 0 to 1 while pin $\overline{WKP_6}$ is low.
	IWPF5	When PMR5 bit WKP5 is changed from 0 to 1 while pin $\overline{WKP_5}$ is low.
	IWPF4	When PMR5 bit WKP4 is changed from 0 to 1 while pin $\overline{WKP_4}$ is low.
	IWPF3	When PMR5 bit WKP3 is changed from 0 to 1 while pin $\overline{WKP_3}$ is low.
	IWPF2	When PMR5 bit WKP2 is changed from 0 to 1 while pin $\overline{WKP_2}$ is low.
	IWPF1	When PMR5 bit WKP1 is changed from 0 to 1 while pin $\overline{WKP_1}$ is low.
	IWPF0	When PMR5 bit WKP0 is changed from 0 to 1 while pin $\overline{WKP_0}$ is low.

Figure 3.7 shows the procedure for setting a bit in a port mode register and clearing the interrupt request flag.

When switching a pin function, mask the interrupt before setting the bit in the port mode register. After accessing the port mode register, execute at least one instruction (e.g., NOP), then clear the interrupt request flag from 1 to 0. If the instruction to clear the flag is executed immediately after the port mode register access without executing an intervening instruction, the flag will not be cleared.

6.10.8 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup period. After the programmer mode setup time, a transition is made to memory read mode.

Table 6.23 Stipulated Transition Times to Command Wait State

Item	Symbol	Min	Max	Unit	Notes
Oscillation stabilization time(crystal oscillator)	T_{osc1}	10	—	ms	Figure 6.20
Oscillation stabilization time(ceramic oscillator)	T_{osc1}	5	—	ms	
Programmer mode setup time	T_{bmv}	10	—	ms	
Vcc hold time	T_{dwn}	0	—	ms	

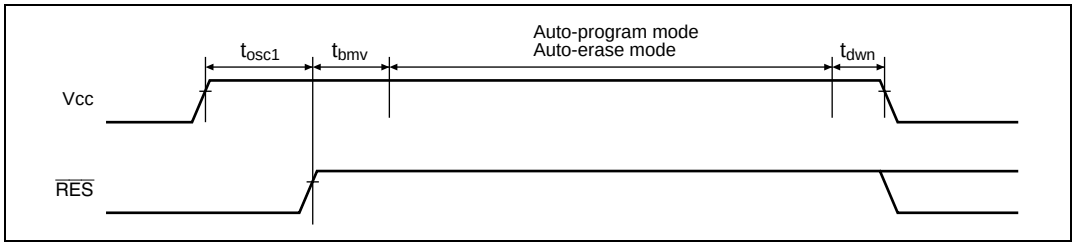


Figure 6.20 Oscillation Stabilization Time, Boot Program Transfer Time, and Power-Down Sequence

6.10.9 Notes on Memory Programming

1. When performing programming using programmer mode on a chip that has been programmed/erased in an on-board programming mode, auto-erasing is recommended before carrying out auto-programming.
2. The flash memory is initially in the erased state when the device is shipped by Renesas Technology. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.

8.9.3 Pin Functions

Table 8.24 shows the port 8 pin functions.

Table 8.24 Port 8 Pin Functions

Pin	Pin Functions and Selection Method
$P8_7/SEG_{32}$ to $P8_0/SEG_{25}$	The pin function depends on bit $PCR8_n$ in PCR8 and bits SGS3 to SGS0 in LPCR.

(n = 7 to 0)

SGS3 to SGS0	000*		001*, 01**,1***
$PCR8_n$	0	1	*
Pin function	$P8_n$ input pin	$P8_n$ output pin	SEG_{n+25} output pin

*: Don't care

8.9.4 Pin States

Table 8.25 shows the port 8 pin states in each operating mode.

Table 8.25 Port 8 Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P8_7/SEG_{32}$ to $P8_0/SEG_{25}$	High-impedance	Retains previous state	Retains previous state	High-impedance	Retains previous state	Functional	Functional

2. Block Diagram

Figure 9.2 shows a block diagram of timer C.

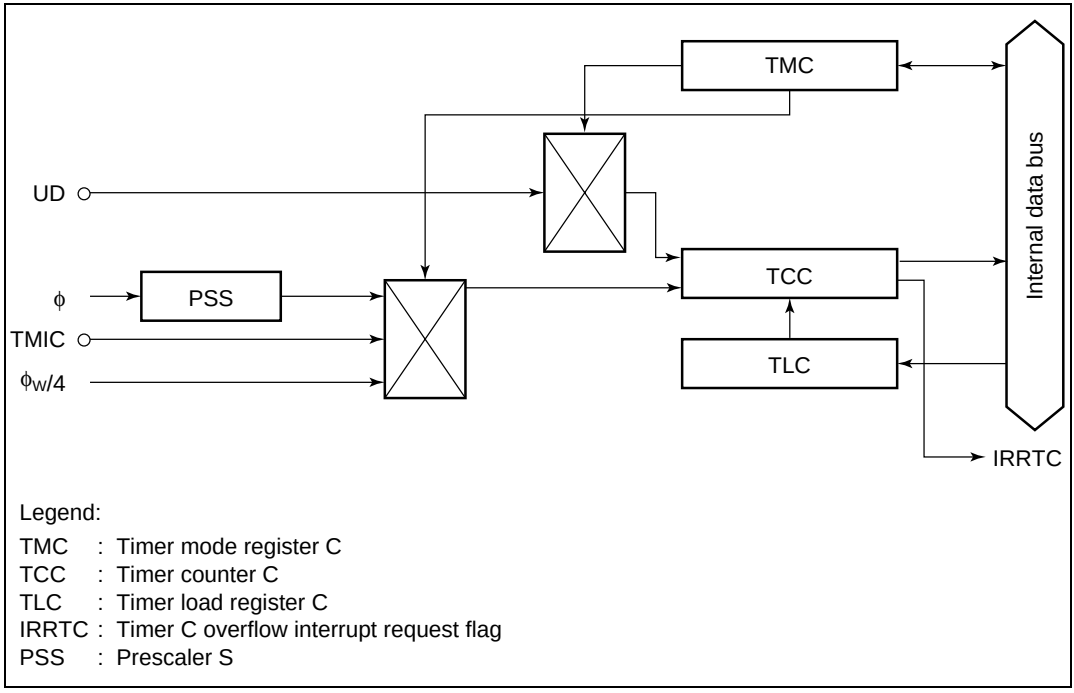


Figure 9.2 Block Diagram of Timer C

3. Pin Configuration

Table 9.5 shows the timer C pin configuration.

Table 9.5 Pin Configuration

Name	Abbr.	I/O	Function
Timer C event input	TMIC	Input	Input pin for event input to TCC
Timer C up/down-count selection	UD	Input	Timer C up/down select

4. Register Configuration

Table 9.6 shows the register configuration of timer C.

Table 9.6 Timer C Registers

Name	Abbr.	R/W	Initial Value	Address
Timer mode register C	TMC	R/W	H'18	H'FFB4
Timer counter C	TCC	R	H'00	H'FFB5
Timer load register C	TLC	W	H'00	H'FFB5
Clock stop register 1	CKSTPR1	R/W	H'FF	H'FFFA

9.3.2 Register Descriptions

1. Timer Mode Register C (TMC)

Bit	7	6	5	4	3	2	1	0
	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

TMC is an 8-bit read/write register for selecting the auto-reload function and input clock, and performing up/down-counter control.

Upon reset, TMC is initialized to H'18.

Bit 7: Auto-reload function select (TMC7)

Bit 7 selects whether timer C is used as an interval timer or auto-reload timer.

Bit 7 TMC7	Description	
0	Interval timer function selected	(initial value)
1	Auto-reload function selected	

2. Read Access

In access to TCF, when the upper byte is read the upper-byte data is transferred directly to the CPU and the lower-byte data is transferred to TEMP. Next, when the lower byte is read, the lower-byte data in TEMP is transferred to the CPU.

In access to OCRF, when the upper byte is read the upper-byte data is transferred directly to the CPU. When the lower byte is read, the lower-byte data is transferred directly to the CPU.

Figure 9.5 shows an example in which TCF is read when it contains H'AAFF.

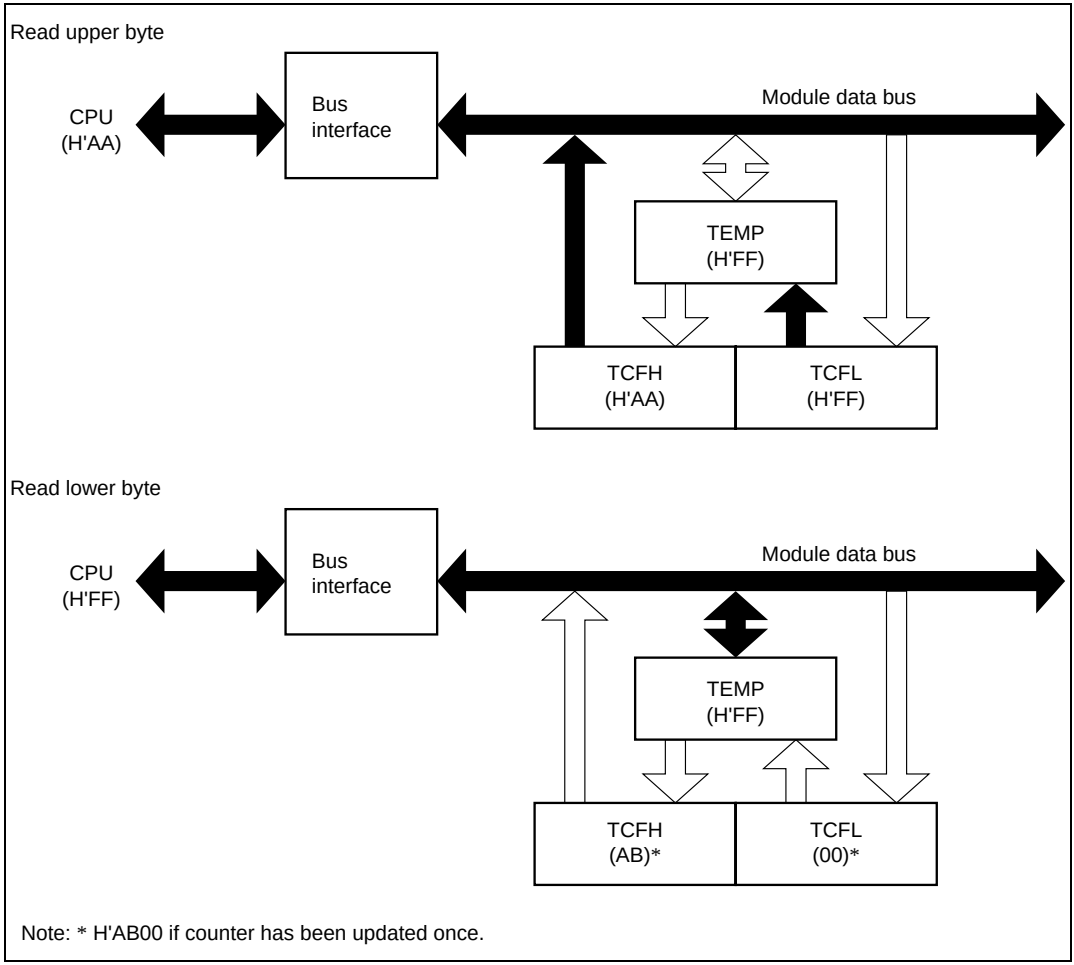


Figure 9.5 Read Access to TCF (TCF → CPU)

9.5.6 Timer G Application Example

Using timer G, it is possible to measure the high and low widths of the input capture input signal as absolute values. For this purpose, CCLR1 and CCLR0 should both be set to 1 in TMG.

Figure 9.16 shows an example of the operation in this case.

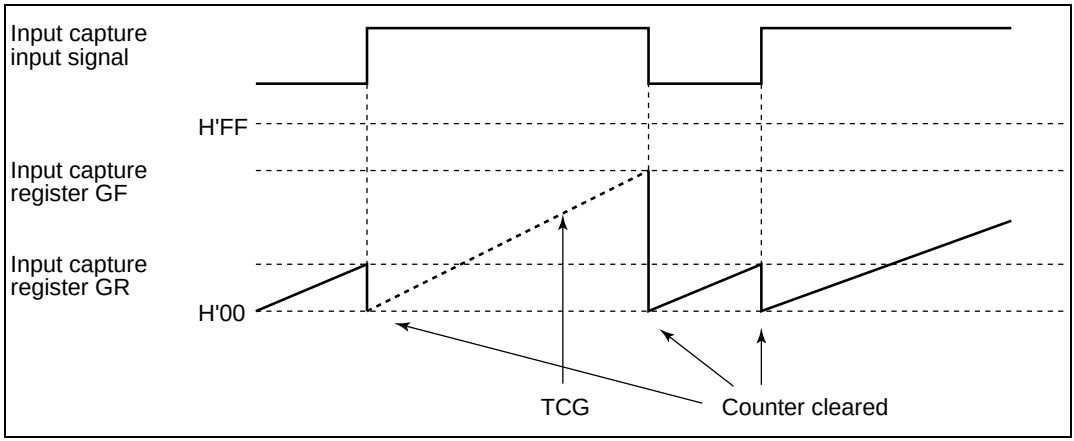


Figure 9.16 Timer G Application Example

9.7.4 Asynchronous Event Counter Operation Modes

Asynchronous event counter operation modes are shown in table 9.21.

Table 9.21 Asynchronous Event Counter Operation Modes

Operation Mode	Reset	Active	Sleep	Watch	Subactive	Subsleep	Standby	Module Standby
ECCSR	Reset	Functions	Functions	Held*	Functions	Functions	Held*	Held
ECH	Reset	Functions	Functions	Functions*	Functions	Functions	Functions*	Halted
ECL	Reset	Functions	Functions	Functions*	Functions	Functions	Functions*	Halted

Note: * When an asynchronous external event is input, the counter increments but the counter overflow H/L flags are not affected.

9.7.5 Application Notes

1. When reading the values in ECH and ECL, the correct value will not be returned if the event counter increments during the read operation. Therefore, if the counter is being used in the 8-bit mode, clear bits CUEH and CUEL in ECCSR to 0 before reading ECH or ECL. If the counter is being used in the 16-bit mode, clear CUEL only to 0 before reading ECH or ECL.
2. In the H8/3847R Group, if the internal power supply step-down circuit is not used, the maximum clock frequency to be input to the AEVH and AEVL pins is 16 MHz when Vcc = 4.5 to 5.5 V, 10 MHz when Vcc = 2.7 to 5.5 V, and 4 MHz when Vcc = 1.8 to 5.5 V. If the internal power step-down circuit is used, the maximum clock frequency to be input is 10 MHz when Vcc = 2.7 to 5.5 V, and 4 MHz when Vcc = 1.8 to 5.5 V. In the H8/3847S Group, the maximum clock frequency to be input is 10 MHz when Vcc = 2.7 to 3.6 V, and 4 MHz when Vcc = 1.8 to 3.6 V. In the H8/38347 Group and H8/38447 Group, the maximum clock frequency to be input is 16 MHz when Vcc = 2.7 to 5.5 V. In addition, ensure that the high and low widths of the clock are at least 32 ns. The duty cycle is immaterial.

Bit 3: Parity error (PER)

Bit 3 indicates that a parity error has occurred during reception with parity added in asynchronous mode.

Bit 3 PER	Description	
0	Reception in progress or completed[*1] Clearing condition: After reading PER = 1, cleared by writing 0 to PER	(initial value)
1	A parity error has occurred during reception[*2] Setting condition: When the number of 1 bits in the receive data plus parity bit does not match the parity designated by bit PM in the serial mode register (SMR)	

Notes: 1. When bit RE in SCR3 is cleared to 0, bit PER is not affected and retains its previous state.

2. Receive data in which it a parity error has occurred is still transferred to RDR, but bit RDRF is not set. Reception cannot be continued with bit PER set to 1. In synchronous mode, neither transmission nor reception is possible when bit FER is set to 1.

Bit 2: Transmit end (TEND)

Bit 2 indicates that bit TDRE is set to 1 when the last bit of a transmit character is sent.

Bit 2 is a read-only bit and cannot be modified.

Bit 2 TEND	Description	
0	Transmission in progress Clearing conditions: After reading TDRE = 1, cleared by writing 0 to TDRE When data is written to TDR by an instruction	
1	Transmission ended Setting conditions: When bit TE in SCR3 is cleared to 0 When bit TDRE is set to 1 when the last bit of a transmit character is sent	(initial value)

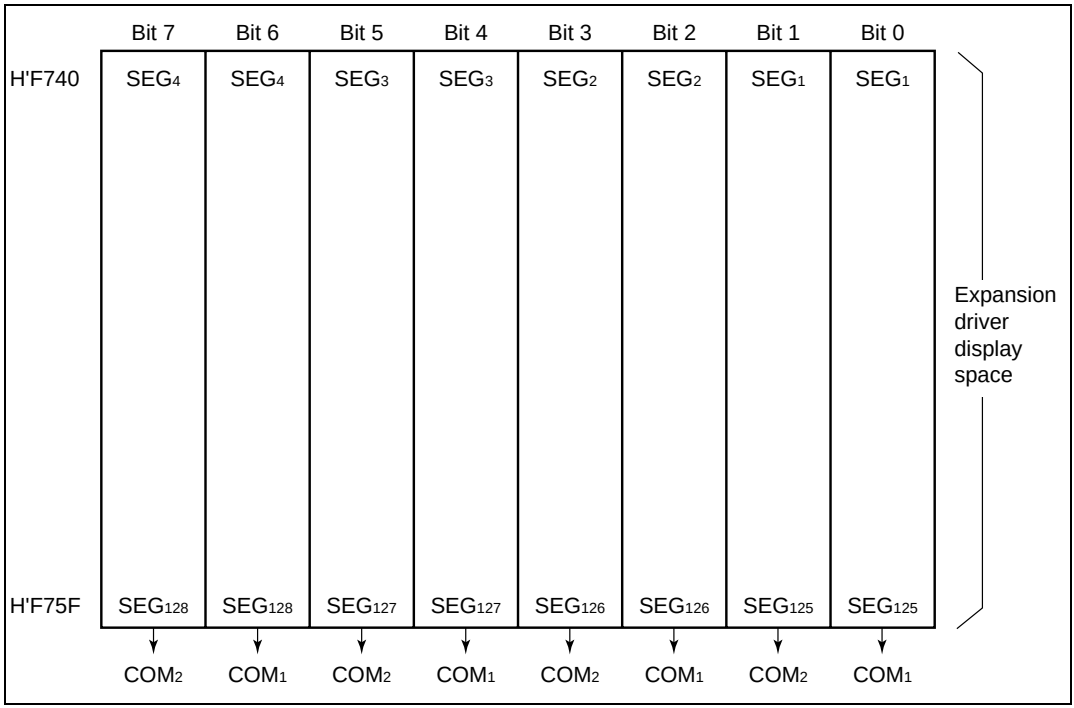


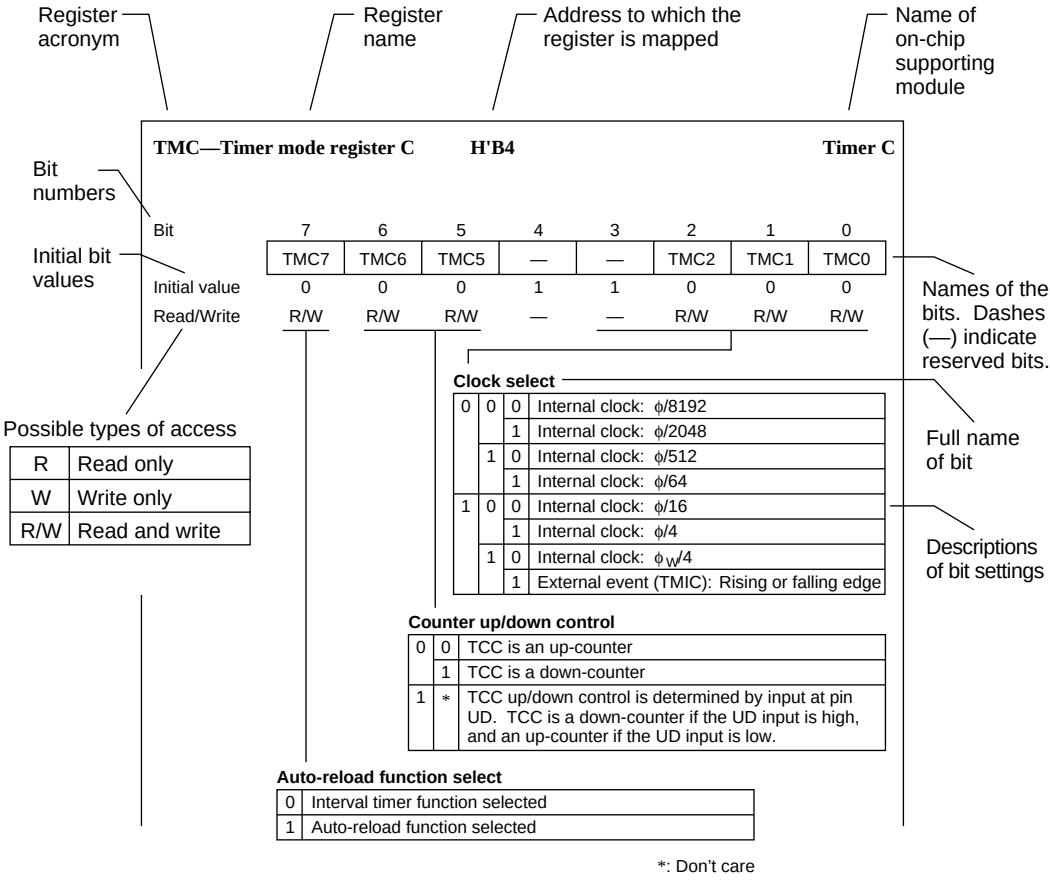
Figure 13.11 LCD RAM Map with Segment Externally Expanded (SGX = "1", SGS3 to SGS0 = "0000" 1/2 duty)

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
SUB	SUB.B Rs, Rd	1					
	SUB.W Rs, Rd	1					
SUBS	SUBS.W #1, Rd	1					
	SUBS.W #2, Rd	1					
POP	POP Rd	1		1			2
PUSH	PUSH Rs	1		1			2
SUBX	SUBX.B #xx:8, Rd	1					
	SUBX.B Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
XORC	XORC #xx:8, CCR	1					

Notes: 1. n: Initial value in R4L. The source and destination operands are accessed n + 1 times each.

2. 1 in the H8/3847R Group and 0 in the H8/3847S Group, H8/38347 Group, and H8/38447 Group.

B.2 Functions



EBR—Erase Block Register **H'F023** **Flash Memory**

Bit	7	6	5	4	3	2	1	0
	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Blocks 7 to 0

0	When a block of EB7 to EB0 is not selected (initial value)
1	When a block of EB7 to EB0 is selected

Note: Set the bit of EBR to H'00 when erasing.

FENR—Flash Memory Enable Register **H'F02B** **Flash Memory**

Bit	7	6	5	4	3	2	1	0
	FLSHE	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	—	—	—	—	—	—	—

Flash Memory Control Register Enable

0	The flash memory control register cannot be accessed
1	The flash memory control register can be accessed

TCSRF—Timer Control/Status Register F H'B7 Timer F

Bit	7	6	5	4	3	2	1	0
	OVFH	CMFH	OVIEH	CCLRH	OVFL	CMFL	OVIEL	CCLRL
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/W	R/W	R/(W)*	R/(W)*	R/W	R/W

Counter clear L

0	TCFL clearing by compare match is disabled
1	TCFL clearing by compare match is enabled

Timer overflow interrupt enable L

0	TCFL overflow interrupt request is disabled
1	TCFL overflow interrupt request is enabled

Compare match flag L

0	[Clearing condition] After reading CMFL = 1, cleared by writing 0 to CMFL
1	[Setting condition] Set when the TCFL value matches the OCRFL value

Timer overflow flag L

0	[Clearing condition] After reading OVFL = 1, cleared by writing 0 to OVFL
1	[Setting condition] Set when TCFL overflows from H'FF to H'00

Counter clear H

0	16-bit mode: TCF clearing by compare match is disabled 8-bit mode: TCFH clearing by compare match is disabled
1	16-bit mode: TCF clearing by compare match is enabled 8-bit mode: TCFH clearing by compare match is enabled

Timer overflow interrupt enable H

0	TCFH overflow interrupt request is disabled
1	TCFH overflow interrupt request is enabled

Compare match flag H

0	[Clearing condition] After reading CMFH = 1, cleared by writing 0 to CMFH
1	[Setting condition] Set when the TCFH value matches the OCRFH value

Timer overflow flag H

0	[Clearing condition] After reading OVFH = 1, cleared by writing 0 to OVFH
1	[Setting condition] Set when TCFH overflows from H'FF to H'00

Note: * Bits 7, 6, 3, and 2 can only be written with 0, for flag clearing.

CKSTPR2—Clock Stop Register 2 **H'FB** **System control**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	AECKSTP	WDCKSTP	PWCKSTP	LDCKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

LCD module standby mode control

0	LCD is set to module standby mode
1	LCD module standby mode is cleared

PWM module standby mode control

0	PWM is set to module standby mode
1	PWM module standby mode is cleared

WDT module standby mode control

0	WDT is set to module standby mode
1	WDT module standby mode is cleared

Asynchronous event counter module standby mode control

0	Asynchronous event counter is set to module standby mode
1	Asynchronous event counter module standby mode is cleared

Product Type				Product Code	Mark Code	Package (Package Code)
H8/38447 Group	H8/38442	Mask ROM versions	Regular products	HD64338442H	38442H	100-pin QFP (FP-100B)
				HD64338442W	38442W	100-pin TQFP (TFP-100G)
				HD64338442X	38442X	100-pin TQFP (TFP-100B)
				HCD64338442	—	Die
			Wide-range specification products	HD64338442HW	38442H	100-pin QFP (FP-100B)
				HD64338442WW	38442W	100-pin TQFP (TFP-100G)
				HD64338442XW	38442X	100-pin TQFP (TFP-100B)
	H8/38443	Mask ROM versions	Regular products	HD64338443H	38443H	100-pin QFP (FP-100B)
				HD64338443W	38443W	100-pin TQFP (TFP-100G)
				HD64338443X	38443X	100-pin TQFP (TFP-100B)
				HCD64338443	—	Die
			Wide-range specification products	HD64338443HW	38443H	100-pin QFP (FP-100B)
				HD64338443WW	38443W	100-pin TQFP (TFP-100G)
				HD64338443XW	38443X	100-pin TQFP (TFP-100B)
	H8/38444	Mask ROM versions	Regular products	HD64338444H	38444H	100-pin QFP (FP-100B)
				HD64338444W	38444W	100-pin TQFP (TFP-100G)
				HD64338444X	38444X	100-pin TQFP (TFP-100B)
				HCD64338444	—	Die
			Wide-range specification products	HD64338444HW	38444H	100-pin QFP (FP-100B)
				HD64338444WW	38444W	100-pin TQFP (TFP-100G)
				HD64338444XW	38444X	100-pin TQFP (TFP-100B)
		F-ZTAT versions	Regular products	HD64F38444H	F38444H	100-pin QFP (FP-100B)
				HD64F38444W	F38444W	100-pin TQFP (TFP-100G)
				HD64F38444X	F38444X	100-pin TQFP (TFP-100B)
			Wide-range specification products	HD64F38444HW	F38444H	100-pin QFP (FP-100B)
				HD64F38444WW	F38444W	100-pin TQFP (TFP-100G)
				HD64F38444XW	F38444X	100-pin TQFP (TFP-100B)

The specifications of the chip tray for the HCD6433847S, HCD6433846S, HCD6433845S, and HCD6433844S are shown in figure I.2.

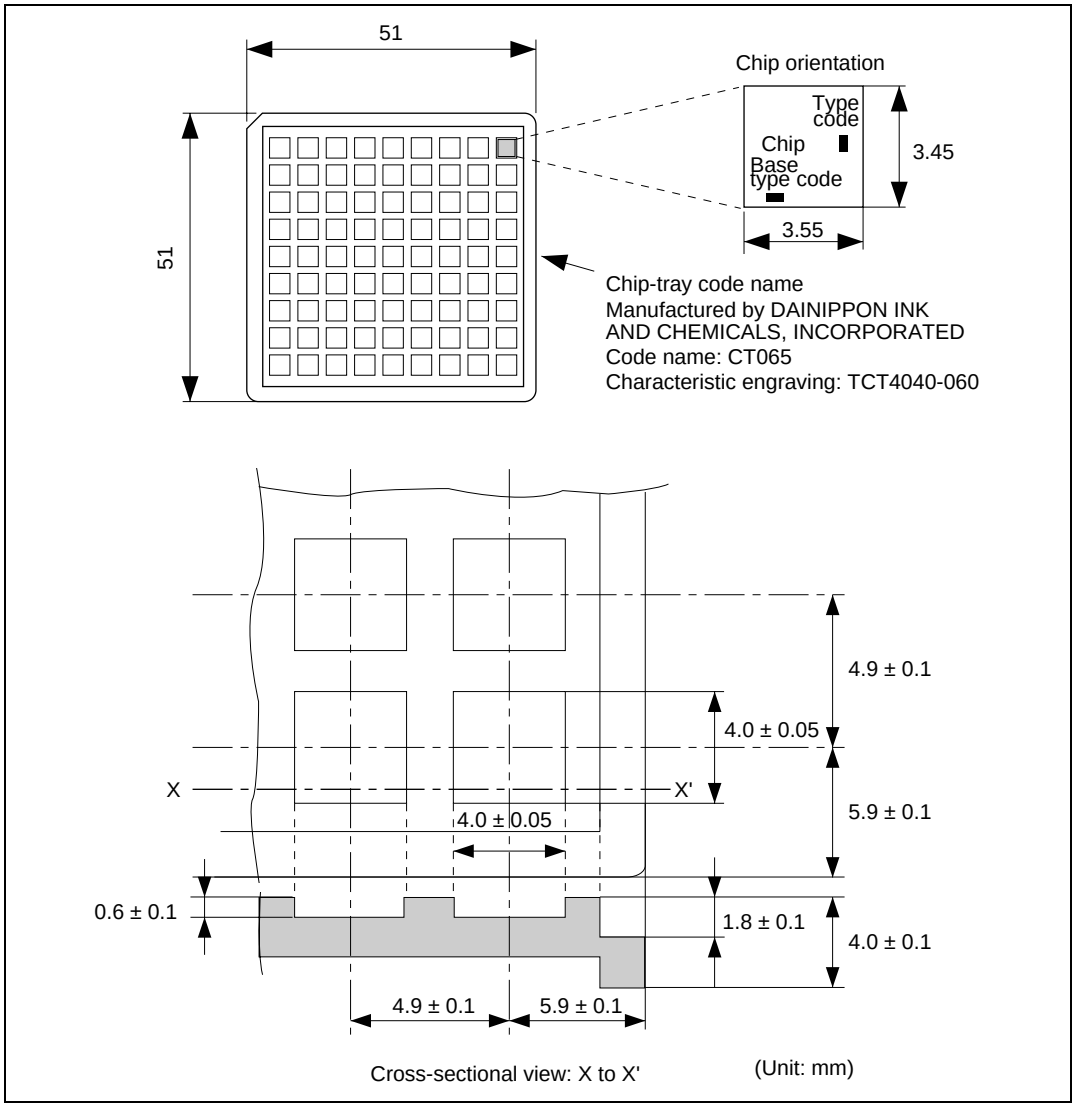


Figure I.2 Specifications of Chip Tray