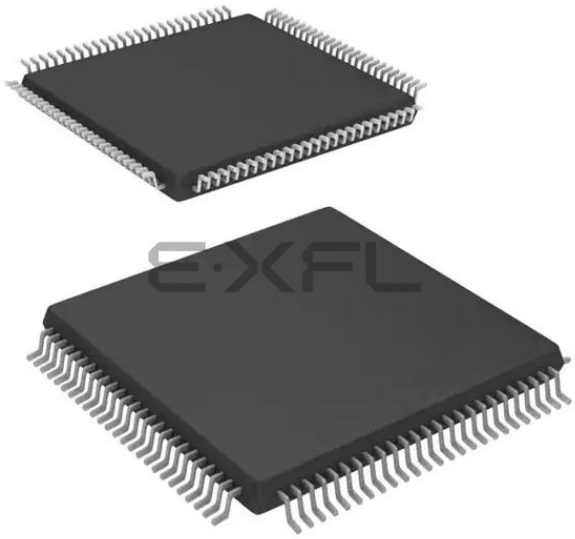

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | H8/300L |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | SCI |
| Peripherals | LCD, PWM, WDT |
| Number of I/O | 71 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df38344xv |

**Section 10 Serial Communication Interface**

**Section 14 Power Supply Circuit**



**Section 15 Electrical Characteristics**



**Appendix C I/O Port Block Diagrams**

| | | Coordinates* | |
|---|---|---|---|
| **Pad No.** | **Pad Name** | **X (µm)** | **Y (µm)** |
| 63 | $P7_4/SEG_{21}$ | 2866 | -76 |
| 64 | $P7_5/SEG_{22}$ | 2866 | 112 |
| 65 | $P7_6/SEG_{23}$ | 2866 | 300 |
| 66 | $P7_7/SEG_{24}$ | 2866 | 528 |
| 67 | $P8_0/SEG_{25}$ | 2866 | 756 |
| 68 | $P8_1/SEG_{26}$ | 2866 | 944 |
| 69 | $P8_2/SEG_{27}$ | 2866 | 1132 |
| 70 | $P8_3/SEG_{28}$ | 2866 | 1318 |
| 71 | $P8_4/SEG_{29}$ | 2866 | 1506 |
| 72 | $P8_5/SEG_{30}$ | 2866 | 1694 |
| 73 | $P8_6/SEG_{31}$ | 2866 | 1882 |
| 74 | $P8_7/SEG_{32}$ | 2866 | 2070 |
| 75 | $P9_0/SEG_{33}$ | 2866 | 2367 |
| 76 | $P9_1/SEG_{34}$ | 2866 | 2931 |
| 77 | $P9_2/SEG_{35}$ | 2654 | 2931 |
| 78 | $P9_3/SEG_{36}$ | 1998 | 2931 |
| 79 | $P9_4/SEG_{37}/M$ | 1803 | 2931 |
| 80 | $P9_5/SEG_{38}/DO$ | 1396 | 2931 |
| 81 | $P9_6/SEG_{39}/CL_2$ | 1209 | 2931 |
| 82 | $P9_7/SEG_{40}/CL_1$ | 977 | 2931 |
| 83 | $P4_0/SCK_{32}$ | 631 | 2931 |
| 84 | $P4_1/RXD_{32}$ | 456 | 2931 |
| 85 | $P4_2/TXD_{32}$ | 284 | 2931 |
| 86 | $P4_3/\overline{IRQ}_0$ | 109 | 2931 |
| 87 | $AV_{CC}$ | -64 | 2931 |
| 88 | $PB_0/AN_0$ | -236 | 2931 |
| 89 | $PB_1/AN_1$ | -409 | 2931 |
| 90 | $PB_2/AN_2$ | -581 | 2931 |
| 91 | $PB_3/AN_3$ | -753 | 2931 |
| 92 | $PB_4/AN_4$ | -925 | 2931 |
| 93 | $PB_5/AN_5$ | -1097 | 2931 |
| 94 | $PB_6/AN_6$ | -1268 | 2931 |

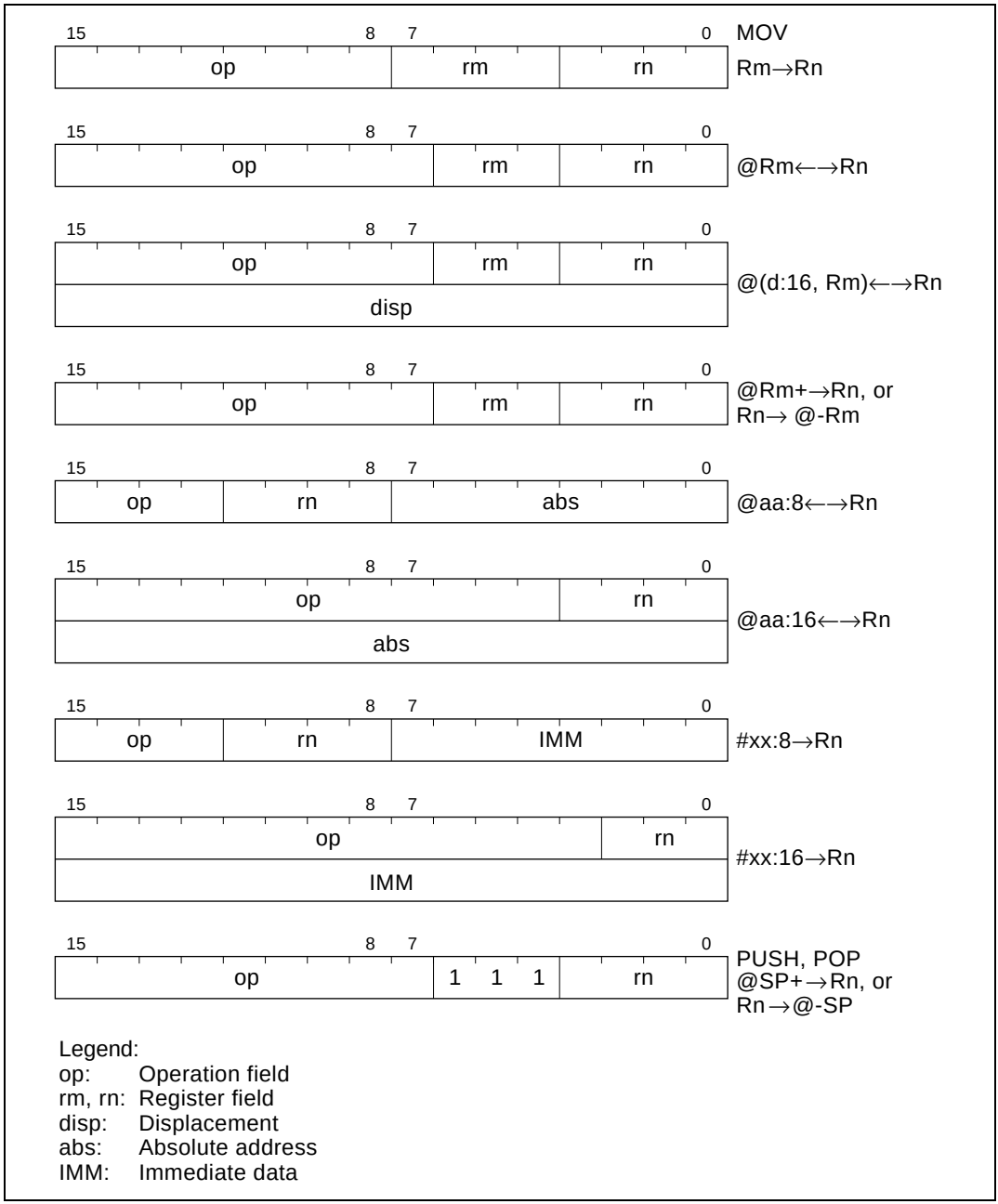



**Figure 2.5 Data Transfer Instruction Codes**

### 2.5.7 System Control Instructions

Table 2.10 describes the system control instructions. Figure 2.9 shows their object code formats.

**Table 2.10 System Control Instructions**

| Instruction | Size* | Function |
|---|---|---|
| RTE | — | Returns from an exception-handling routine |
| SLEEP | — | Causes a transition from active mode to a power-down mode. See section 5, Power-Down Modes, for details. |
| LDC | B | Rs → CCR, #IMM → CCR<br>Moves immediate data or general register contents to the condition code register |
| STC | B | CCR → Rd<br>Copies the condition code register to a specified general register |
| ANDC | B | CCR ∧ #IMM → CCR<br>Logically ANDs the condition code register with immediate data |
| ORC | B | CCR ∨ #IMM → CCR<br>Logically ORs the condition code register with immediate data |
| XORC | B | CCR ⊕ #IMM → CCR<br>Logically exclusive-ORs the condition code register with immediate data |
| NOP | — | PC + 2 → PC<br>Only increments the program counter |

Note: * Size: Operand size
B: Byte

**Bit n:** $\overline{\text{WKP}}$n edge select (WKEGSn)

Bit n selects $\overline{\text{WKP}}$n pin input sensing.

| Bit n WKEGSn | Description | |
|---|---|---|
| 0 | $\overline{\text{WKP}}$n pin falling edge detected | (initial value) |
| 1 | $\overline{\text{WKP}}$n pin rising edge detected | |

(n = 7 to 0)

### 3.3.3 External Interrupts

There are 13 external interrupts: $IRQ_4$ to $IRQ_0$ and $WKP_7$ to $WKP_0$.

#### 1. Interrupts $WKP_7$ to $WKP_0$

Interrupts $WKP_7$ to $WKP_0$ are requested by either rising or falling edge input to pins $\overline{\text{WKP}}_7$ to $\overline{\text{WKP}}_0$. When these pins are designated as pins $\overline{\text{WKP}}_7$ to $\overline{\text{WKP}}_0$ in port mode register 5 and a rising or falling edge is input, the corresponding bit in IWPR is set to 1, requesting an interrupt. Recognition of wakeup interrupt requests can be disabled by clearing the IENWP bit to 0 in IENR1. These interrupts can all be masked by setting the I bit to 1 in CCR.

When $WKP_7$ to $WKP_0$ interrupt exception handling is initiated, the I bit is set to 1 in CCR. Vector number 9 is assigned to interrupts $WKP_7$ to $WKP_0$. All eight interrupt sources have the same vector number, so the interrupt-handling routine must discriminate the interrupt source.

#### 2. Interrupts $IRQ_4$ to $IRQ_0$

Interrupts IRQ4 to $IRQ_0$ are requested by input signals to pins $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_0$. These interrupts are detected by either rising edge sensing or falling edge sensing, depending on the settings of bits $IEG_4$ to $IEG_0$ in IEGR.

When these pins are designated as pins $\overline{\text{IRQ}}_4$ to $\overline{\text{IRQ}}_0$ in port mode register 3 and 1 and the designated edge is input, the corresponding bit in IRR1 is set to 1, requesting an interrupt. Recognition of these interrupt requests can be disabled individually by clearing bits IEN4 to IEN0 to 0 in IENR1. These interrupts can all be masked by setting the I bit to 1 in CCR.

When $IRQ_4$ to $IRQ_0$ interrupt exception handling is initiated, the I bit is set to 1 in CCR. Vector numbers 8 to 4 are assigned to interrupts $IRQ_4$ to $IRQ_0$. The order of priority is from $IRQ_0$ (high) to $IRQ_4$ (low). Table 3.2 gives details.

## 5.7 Active (Medium-Speed) Mode

### 5.7.1 Transition to Active (Medium-Speed) Mode

If the $\overline{\text{RES}}$ pin is driven low, active (medium-speed) mode is entered. If the LSON bit in SYSCR2 is set to 1 while the LSON bit in SYSCR1 is cleared to 0, a transition to active (medium-speed) mode results from $IRQ_0$, $IRQ_1$, or $WKP_7$ to $WKP_0$ interrupts in standby mode, timer A, timer F, timer G, $IRQ_0$, or $WKP_7$ to $WKP_0$ interrupts in watch mode, or any interrupt in sleep mode. A transition to active (medium-speed) mode does not take place if the I bit of CCR is set to 1 or the particular interrupt is disabled in the interrupt enable register.

The CPU may operate at a 1/2 state faster timing at transition to active (medium-speed) mode.

### 5.7.2 Clearing Active (Medium-Speed) Mode

Active (medium-speed) mode is cleared by a SLEEP instruction.

- Clearing by SLEEP instruction

  A transition to standby mode takes place if the SLEEP instruction is executed while the SSBY bit in SYSCR1 is set to 1, the LSON bit in SYSCR1 is cleared to 0, and the TMA3 bit in TMA is cleared to 0. The system goes to watch mode if the SSBY bit in SYSCR1 is set to 1 and bit TMA3 in TMA is set to 1 when a SLEEP instruction is executed.

  When both SSBY and LSON are cleared to 0 in SYSCR1 and a SLEEP instruction is executed, sleep mode is entered. Direct transfer to active (high-speed) mode or to subactive mode is also possible. See section 5.8, Direct Transfer, below for details.

- Clearing by $\overline{\text{RES}}$ pin

  When the $\overline{\text{RES}}$ pin is driven low, a transition is made to the reset state and active (medium-speed) mode is cleared.

### 5.7.3 Operating Frequency in Active (Medium-Speed) Mode

Operation in active (medium-speed) mode is clocked at the frequency designated by the MA1 and MA0 bits in SYSCR1.

### 6.7.2 Programming/Erasing in User Program Mode

The term user mode refers to the status when a user program is being executed. On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user program/erase control program or a program that provides the user program/erase control program from external memory. As the flash memory itself cannot be read during programming/erasing, transfer the user program/erase control program to on-chip RAM, as in boot mode. Figure 6.9 shows a sample procedure for programming/erasing in user program mode. Prepare a user program/erase control program in accordance with the description in section 6.8, Flash Memory Programming/Erasing.

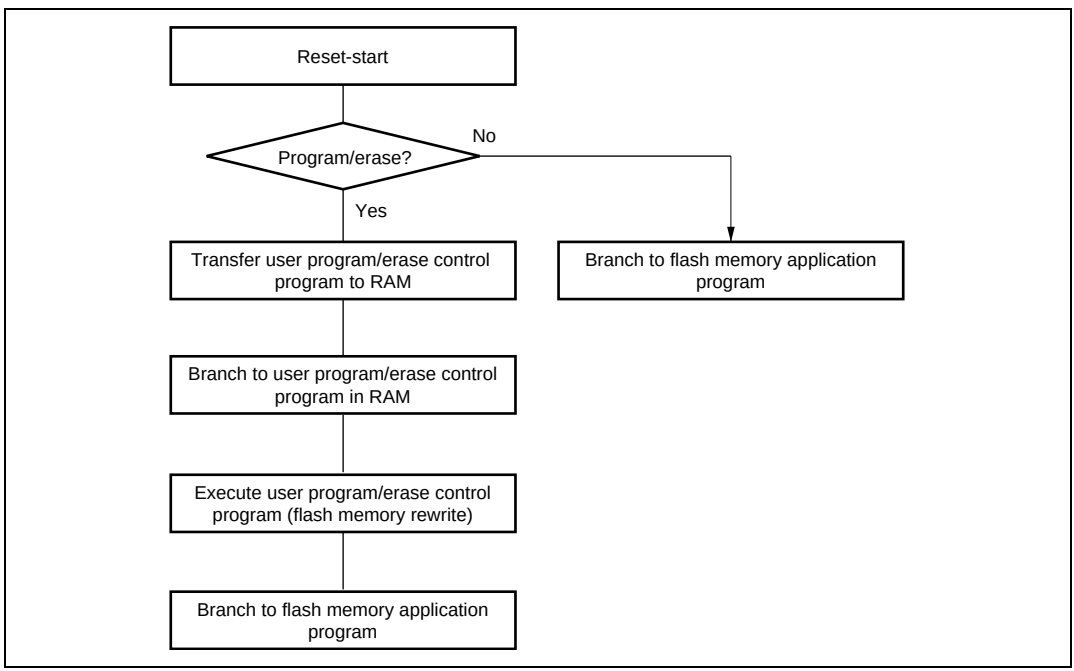



**Figure 6.9 Programming/Erasing Flowchart Example in User Program Mode**

## 6.8 Flash Memory Programming/Erasing

A software method using the CPU is employed to program and erase flash memory in the on-board programming modes. Depending on the FLMCR1 setting, the flash memory operates in one of the following four modes: Program mode, program-verify mode, erase mode, and erase-verify mode. The programming control program in boot mode and the user program/erase control

program in user program mode use these operating modes in combination to perform programming/erasing. Flash memory programming and erasing should be performed in accordance with the descriptions in section 6.8.1, Program/Program-Verify and section 6.8.2, Erase/Erase-Verify, respectively.

### 6.8.1 Program/Program-Verify

When writing data or programs to the flash memory, the program/program-verify flowchart shown in figure 6.10 should be followed. Performing programming operations according to this flowchart will enable data or programs to be written to the flash memory without subjecting the chip to voltage stress or sacrificing program data reliability.

1. Programming must be done to an empty address. Do not reprogram an address to which programming has already been performed.
2. Programming should be carried out 128 bytes at a time. A 128-byte data transfer must be performed even if writing fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
3. Prepare the following data storage areas in RAM: A 128-byte programming data area, a 128-byte reprogramming data area, and a 128-byte additional-programming data area. Perform reprogramming data computation according to table 6.11, and additional programming data computation according to table 6.12.
4. Consecutively transfer 128 bytes of data in byte units from the reprogramming data area or additional-programming data area to the flash memory. The program address and 128-byte data are latched in the flash memory. The lower 8 bits of the start address in the flash memory destination area must be H'00 or H'80.
5. The time during which the P bit is set to 1 is the programming time. Figure 6.12 shows the allowable programming times.
6. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. An overflow cycle of approximately 6.6 ms is allowed.
7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 1 bit is b'0. Verify data can be read in word size from the address to which a dummy write was performed.
8. The maximum number of repetitions of the program/program-verify sequence of the same bit is 1,000.

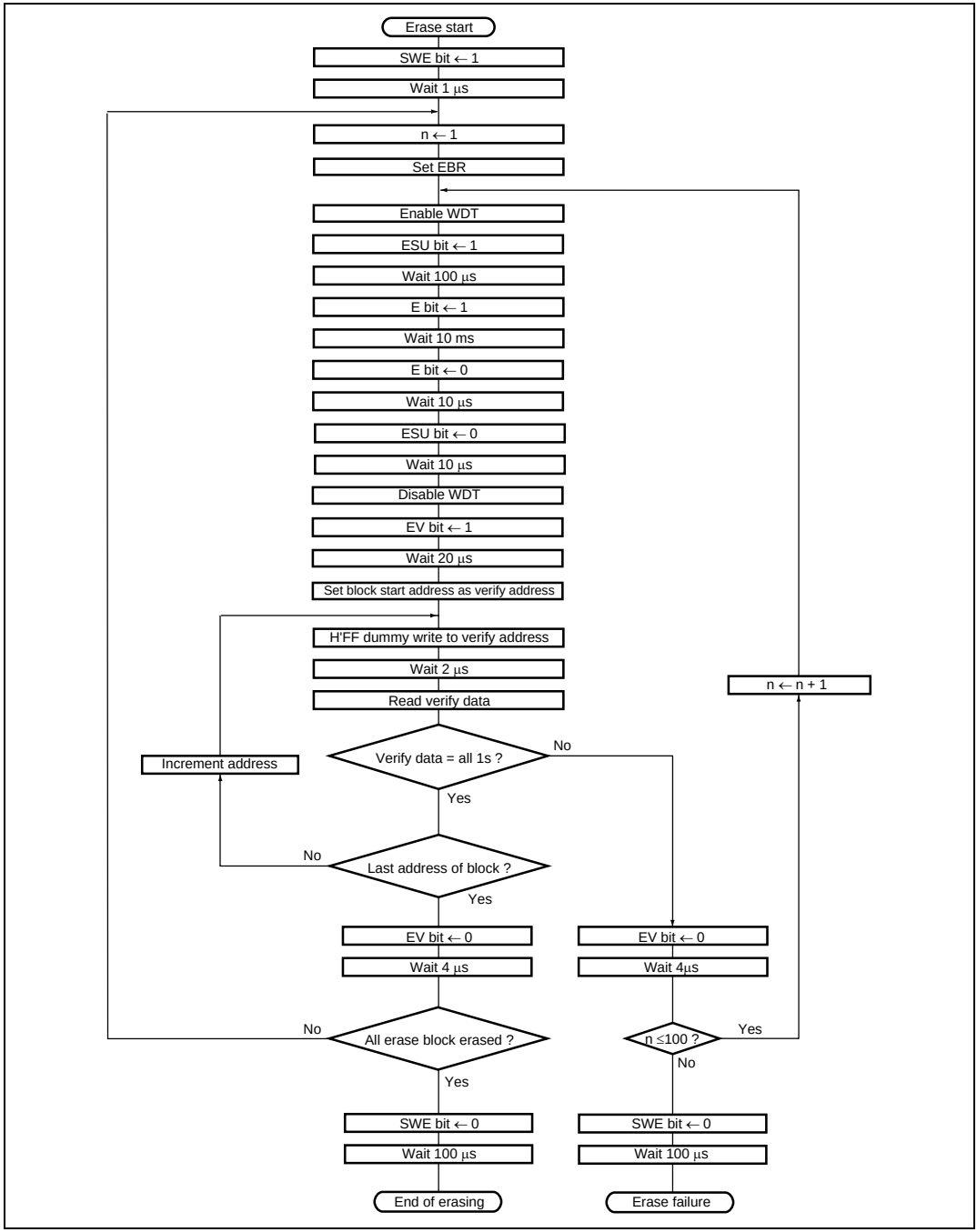



**Figure 6.11 Erase/Erase-Verify Flowchart**

## 8.7 Port 6

### 8.7.1 Overview

Port 6 is an 8-bit I/O port. The port 6 pin configuration is shown in figure 8.6.

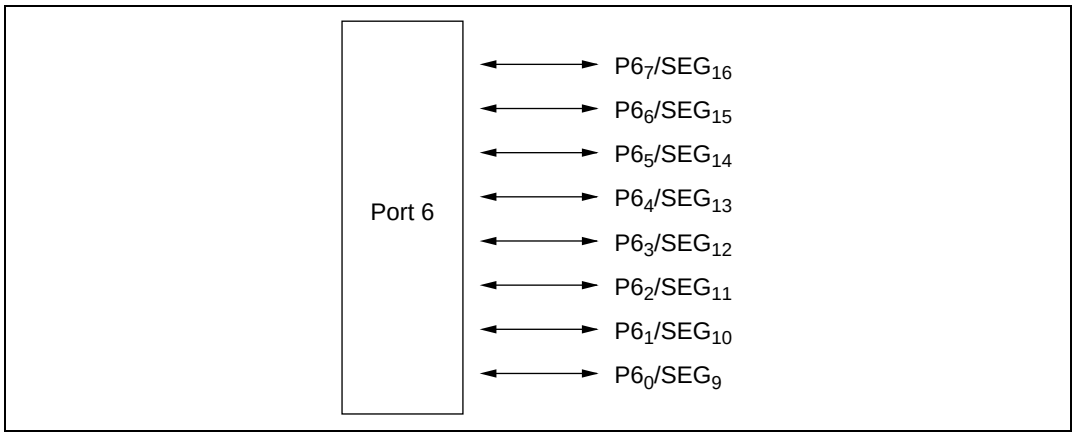



**Figure 8.6 Port 6 Pin Configuration**

### 8.7.2 Register Configuration and Description

Table 8.17 shows the port 6 register configuration.

**Table 8.17 Port 6 Registers**

| Name | Abbr. | R/W | Initial Value | Address |
|---|---|---|---|---|
| Port data register 6 | PDR6 | R/W | H'00 | H'FFD9 |
| Port control register 6 | PCR6 | W | H'00 | H'FFE9 |
| Port pull-up control register 6 | PUCR6 | R/W | H'00 | H'FFE3 |

**Table 10.11 SMR Settings and Corresponding Data Transfer Formats**

| SMR | | | | | | Data Transfer Format | | | |
|---|---|---|---|---|---|---|---|---|---|
| bit 7 COM | bit 6 CHR | bit 2 MP | bit 5 PE | bit 3 STOP | Mode | Data Length | Multiprocessor Bit | Parity Bit | Stop Bit Length |
| 0 | 0 | 0 | 0 | 0 | Asynchronous mode | 8-bit data | No | No | 1 bit |
| 0 | 0 | 0 | 0 | 1 | | | | | 2 bits |
| 0 | 0 | 0 | 1 | 0 | | | | Yes | 1 bit |
| 0 | 0 | 0 | 1 | 1 | | | | | 2 bits |
| 0 | 1 | 0 | 0 | 0 | | 7-bit data | | No | 1 bit |
| 0 | 1 | 0 | 0 | 1 | | | | | 2 bits |
| 0 | 1 | 0 | 1 | 0 | | | | Yes | 1 bit |
| 0 | 1 | 0 | 1 | 1 | | | | | 2 bits |
| 0 | 0 | 1 | 0 | 0 | | 8-bit data | Yes | No | 1 bit |
| 0 | 0 | 1 | 0 | 1 | | | | | 2 bits |
| 0 | 0 | 1 | 1 | 0 | | 5-bit data | No | | 1 bit |
| 0 | 0 | 1 | 1 | 1 | | | | | 2 bits |
| 0 | 1 | 1 | 0 | 0 | | 7-bit data | Yes | | 1 bit |
| 0 | 1 | 1 | 0 | 1 | | | | | 2 bits |
| 0 | 1 | 1 | 1 | 0 | | 5-bit data | No | Yes | 1 bit |
| 0 | 1 | 1 | 1 | 1 | | | | | 2 bits |
| 1 | * | 0 | * | * | Synchronous mode | 8-bit data | No | No | No |

*: Don’t care

**Bit 4:** Display data control (DISP)

Bit 4 specifies whether the LCD RAM contents are displayed or blank data is displayed regardless of the LCD RAM contents.

| Bit 4 DISP | Description | |
|---|---|---|
| 0 | Blank data is displayed | (initial value) |
| 1 | LCD RAM data is display | |

**Bits 3 to 0:** Frame frequency select 3 to 0 (CKS3 to CKS0)

Bits 3 to 0 select the operating clock and the frame frequency. In subactive mode, watch mode, and subsleep mode, the system clock (φ) is halted, and therefore display operations are not performed if one of the clocks from φ/2 to φ/256 is selected. If LCD display is required in these modes, φw, φw/2, or φw/4 must be selected as the operating clock.

| Bit 3 CKS3 | Bit 2 CKS2 | Bit 1 CKS1 | Bit 0 CKS0 | Operating Clock | Frame Frequency*2 φ = 2 MHz | Frame Frequency*2 φ = 250 kHz*1 |
|---|---|---|---|---|---|---|
| 0 | * | 0 | 0 | φw | 128 Hz*3 (initial value) | |
| 0 | * | 0 | 1 | φw/2 | 64 Hz*3 | |
| 0 | * | 1 | * | φw/4 | 32 Hz*3 | |
| 1 | 0 | 0 | 0 | φ/2 | — | 244 Hz |
| 1 | 0 | 0 | 1 | φ/4 | 977 Hz | 122 Hz |
| 1 | 0 | 1 | 0 | φ/8 | 488 Hz | 61 Hz |
| 1 | 0 | 1 | 1 | φ/16 | 244 Hz | 30.5 Hz |
| 1 | 1 | 0 | 0 | φ/32 | 122 Hz | — |
| 1 | 1 | 0 | 1 | φ/64 | 61 Hz | — |
| 1 | 1 | 1 | 0 | φ/128 | 30.5 Hz | — |
| 1 | 1 | 1 | 1 | φ/256 | — | — |

*: Don't care

Notes: 1. This is the frame frequency in active (medium-speed, φosc/16) mode when φ = 2 MHz.
2. When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.
3. This is the frame frequency when φw = 32.768 kHz.

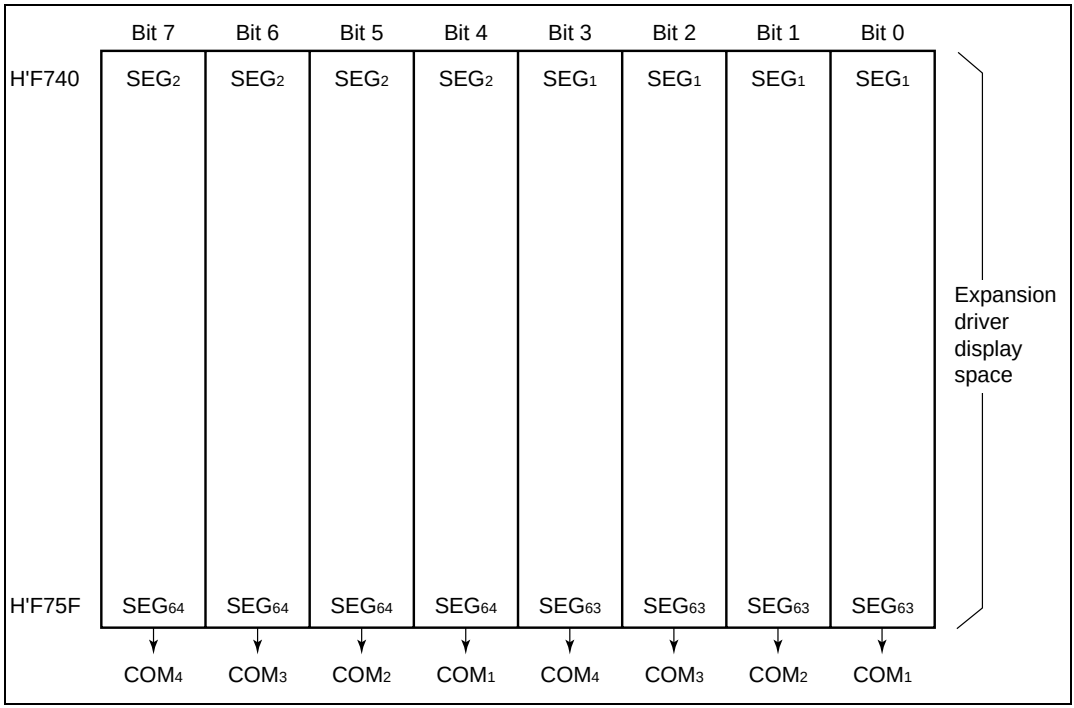
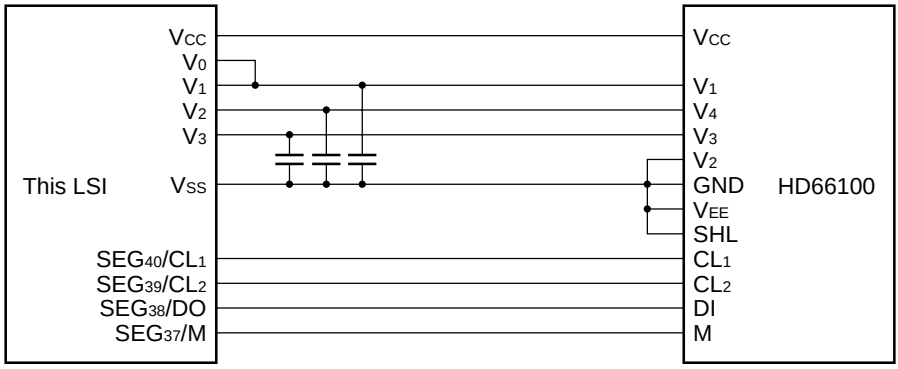
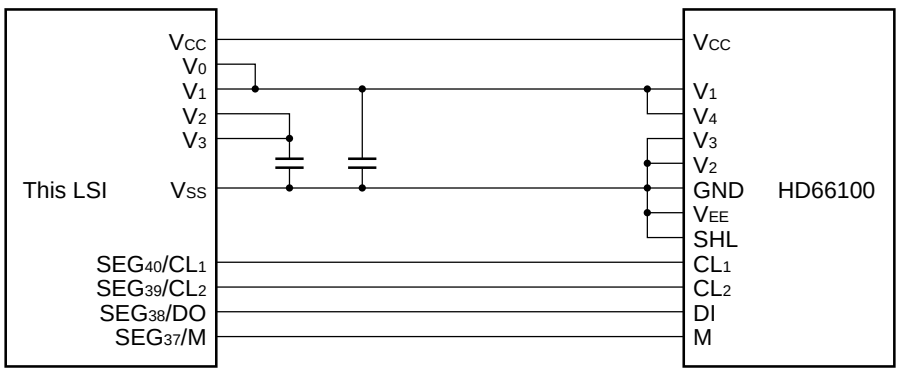


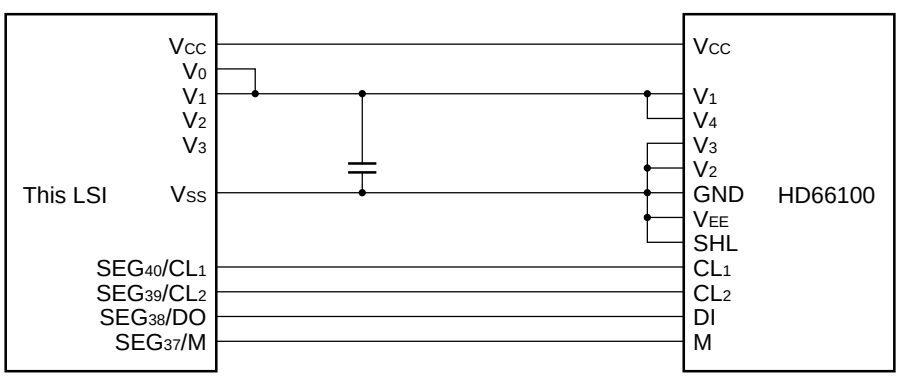

**Figure 13.9 LCD RAM Map with Segment Externally Expanded (SGX = "1", SGS3 to SGS0 = "0000" 1/4 duty)**




(a) 1/3 bias, 1/4 duty or 1/3 duty




(b) 1/2 duty




(c) Static

**Figure 13.18 Connection to HD66100**

### 15.2.5 LCD Characteristics

Table 15.7 shows the LCD characteristics.

**Table 15.7 LCD Characteristics**

$V_{CC}$ = 1.8 V to 5.5 V, $AV_{CC}$ = 1.8 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, Ta = –20°C to +75°C*3 (including subactive mode) unless otherwise indicated.

| Item | Symbol | Applicable Pins | Values Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| Segment driver drop voltage | $V_{DS}$ | $SEG_1$ to $SEG_{40}$ | — | — | 0.6 | V | $I_D$ = 2 µA<br>$V_1$ = 2.7 V to 5.5 V | *1 |
| Common driver drop voltage | $V_{DC}$ | $COM_1$ to $COM_4$ | — | — | 0.3 | V | $I_D$ = 2 µA<br>$V_1$ = 2.7 V to 5.5 V | *1 |
| LCD power supply split-resistance | $R_{LCD}$ | | 0.5 | 3.0 | 9.0 | MΩ | Between $V_1$ and $V_{SS}$ | |
| Liquid crystal display voltage | $V_{LCD}$ | $V_1$ | 2.2 | — | 5.5 | V | | *2 |

Notes: 1. The voltage drop from power supply pins $V_1$, $V_2$, $V_3$, and $V_{SS}$ to each segment pin or common pin.
2. When the liquid crystal display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V_1 \geq V_2 \geq V_3 \geq V_{SS}$.
3. The guaranteed temperature as an electrical characteristic for Die products is 75°C.

### 15.4.4 A/D Converter Characteristics

Table 15.14 shows the A/D converter characteristics.

**Table 15.14 A/D Converter Characteristics**

$V_{CC}$ = 1.8 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, Ta = –40°C to +85°C unless otherwise indicated.

| Item | Symbol | Applicable Pins | Values Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Analog power supply voltage | $AV_{CC}$ | $AV_{CC}$ | 1.8 | — | 5.5 | V | | *1 |
| Analog input voltage | $AV_{IN}$ | $AN_0$ to $AN_{11}$ | – 0.3 | — | $AV_{CC}$ + 0.3 | V | | |
| Analog power supply current | $AI_{OPE}$ | $AV_{CC}$ | — | — | 1.5 | mA | $AV_{CC}$ = 5.0 V | |
| | $AI_{STOP1}$ | $AV_{CC}$ | — | 600 | — | µA | | *2 Reference value |
| | $AI_{STOP2}$ | $AV_{CC}$ | — | — | 5 | µA | | *3 |
| Analog input capacitance | $C_{AIN}$ | $AN_0$ to $AN_{11}$ | — | — | 15.0 | pF | | |
| Allowable signal source impedance | $R_{AIN}$ | | — | — | 10.0 | kΩ | | |
| Resolution (data length) | | | — | — | 10 | bit | | |
| Nonlinearity error | | | — | — | ±2.5 | LSB | $AV_{CC}$ = 2.7 V to 5.5 V<br>$V_{CC}$ = 2.7 V to 5.5 V | *4 |
| | | | — | — | ±5.5 | | $AV_{CC}$ = 2.0 V to 5.5 V<br>$V_{CC}$ = 2.0 V to 5.5 V | |
| | | | — | — | ±7.5 | | Except the above | *5 |
| Quantization error | | | — | — | ±0.5 | LSB | | |
| Absolute accuracy | | | — | — | ±3.0 | LSB | $AV_{CC}$ = 2.7 V to 5.5 V<br>$V_{CC}$ = 2.7 V to 5.5 V | *4 |
| | | | — | — | ±6.0 | | $AV_{CC}$ = 2.0 V to 5.5 V<br>$V_{CC}$ = 2.0 V to 5.5 V | |
| | | | — | — | ±8.0 | | Except the above | *5 |
| Conversion time | | | 12.4 | — | 124 | µs | $AV_{CC}$ = 2.7 V to 5.5 V<br>$V_{CC}$ = 2.7 V to 5.5 V | *4 |
| | | | 62 | — | 124 | | Except the above | |

Notes: 1. Set $AV_{CC}$ = $V_{CC}$ when the A/D converter is not used.
2. $AI_{STOP1}$ is the current in active and sleep modes while the A/D converter is idle.
3. $AI_{STOP2}$ is the current at reset and in standby, watch, subactive, and subsleep modes while the A/D converter is idle.
4. When internal power supply step-down circuit is not used.
5. Conversion time: 62 µs

| Item | Symbol | Applicable Pins | Values Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Allowable output high current (total) | $\sum -I_{OH}$ | All output pins | — | — | 10.0 | mA | | |

Notes: Connect the TEST pin to $V_{SS}$.

1. Pin States during Current Dissipation Measurement.

| Mode | $\overline{RES}$ Pin | Internal State | Other Pins | Constant-Voltage | Oscillator Pins |
|---|---|---|---|---|---|
| Active (high-speed) mode | $V_{CC}$ | Only CPU Operates | $V_{CC}$ | Halted | System clock oscillator: Crystal |
| Active (medium-speed) mode | | | | | Subclock oscillator: Pin $X_1$ = GND |
| Sleep mode | $V_{CC}$ | Only timers operate | $V_{CC}$ | | |
| Subactive mode | $V_{CC}$ | Only CPU Operates | $V_{CC}$ | Halted | System clock oscillator: crystal |
| Subsleep mode | $V_{CC}$ | Only timers operate, CPU stops | $V_{CC}$ | Halted | Subclock oscillator: crystal |
| Watch mode | $V_{CC}$ | Only time base operates, CPU stops | $V_{CC}$ | Halted | |
| Standby mode | $V_{CC}$ | CPU and timers both stop | $V_{CC}$ | Halted | System clock oscillator: crystal<br>Subclock oscillator: Pin $X_1$ = GND |

2. Excludes current in pull-up MOS transistors and output buffers.
3. The maximum current consumption value (standard) is 1.1 × typ.

| Item | Symbol | Applicable Pins | Values Min | Typ | Max | Unit | Test Condition | Reference Figure |
|---|---|---|---|---|---|---|---|---|
| Oscillation stabilization time | $t_{rc}$ | $OSC_1$, $OSC_2$ | — | 4.0 | — | | Crystal Oscillator Parameters Except the above | Figure 15.10 |
| | | | — | — | 50 | | Except the above | |
| | | X1, X2 | — | — | 2 | s | $V_{CC}$ = 2.2 V to 3.6 V | |
| | | | — | 4 | — | | Except the above | |
| External clock high width | $t_{CPH}$ | $OSC_1$ | 40 | — | — | ns | $V_{CC}$ = 2.7 V to 3.6 V | Figure 15.1 |
| | | | 100 | — | — | | $V_{CC}$ = 1.8 V to 3.6 V | |
| | | $X_1$ | — | 15.26 or 13.02 | — | µs | | |
| External clock low width | $t_{CPL}$ | $OSC_1$ | 40 | — | — | ns | $V_{CC}$ = 2.7 V to 3.6 V | Figure 15.1 |
| | | | 100 | — | — | | $V_{CC}$ = 1.8 V to 3.6 V | |
| | | $X_1$ | — | 15.26 or 13.02 | — | µs | | |
| External clock rise time | $t_{CPr}$ | $OSC_1$ | — | — | 10 | ns | $V_{CC}$ = 2.7 V to 3.6 V | Figure 15.1 |
| | | | — | — | 25 | | $V_{CC}$ = 1.8 V to 3.6 V | |
| | | $X_1$ | — | — | 55.0 | ns | | Figure 15.1 |
| External clock fall time | $t_{CPf}$ | $OSC_1$ | — | — | 10 | ns | $V_{CC}$ = 2.7 V to 3.6 V | Figure 15.1 |
| | | | — | — | 25 | | $V_{CC}$ = 1.8 V to 3.6 V | |
| | | $X_1$ | — | — | 55.0 | ns | | Figure 15.1 |
| Pin $\overline{RES}$ low width | $t_{REL}$ | $\overline{RES}$ | 10 | — | — | $t_{cyc}$ | | Figure 15.2 |
| Input pin high width | $t_{IH}$ | $\overline{IRQ_0}$ to $\overline{IRQ_4}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{ADTRG}$, TMIC TMIF, TMIG, AEVL, AEVH | 2 | — | — | $t_{cyc}$ $t_{subcyc}$ | | Figure 15.3 |
| Input pin low width | $t_{IL}$ | $\overline{IRQ_0}$ to $\overline{IRQ_4}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{ADTRG}$, TMIC, TMIF, TMIG, AEVL, AEVH | 2 | — | — | $t_{cyc}$ $t_{subcyc}$ | | Figure 15.3 |

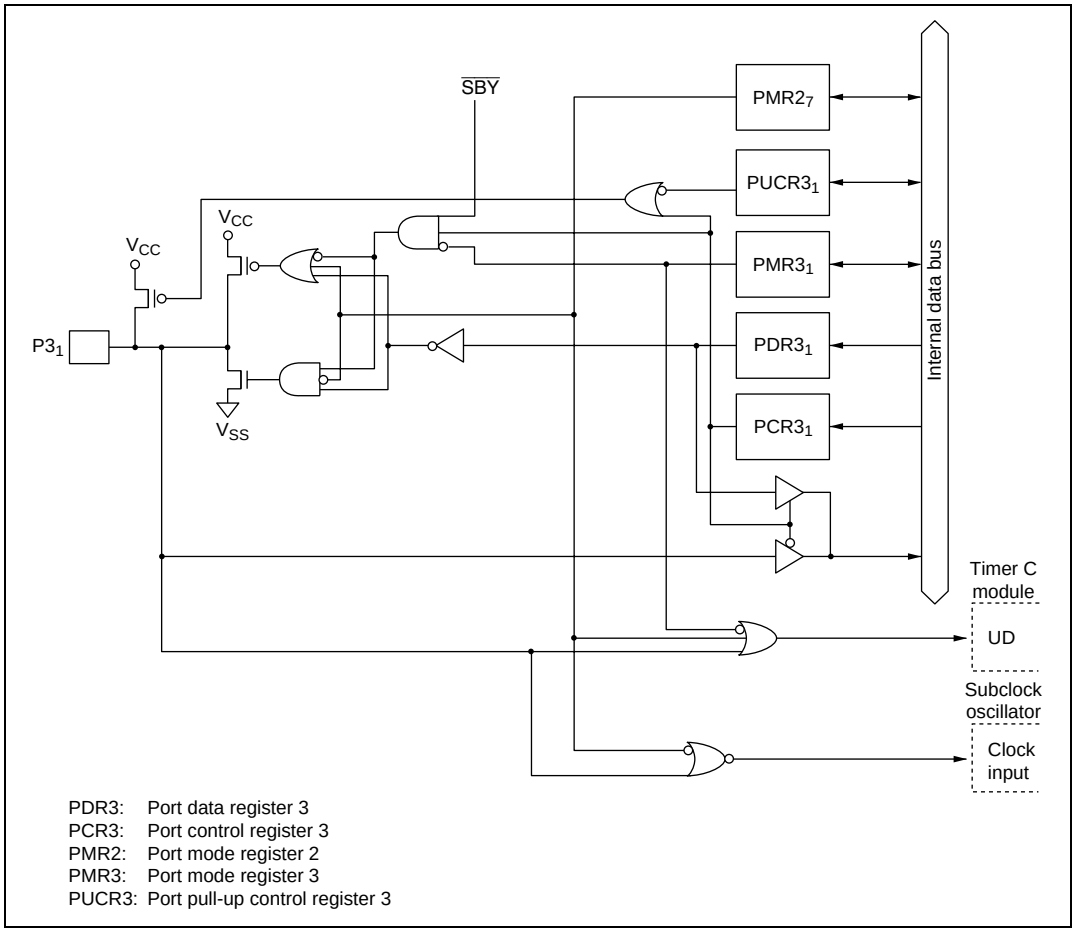



**Figure C.3 (f-2) Port 3 Block Diagram (Pin P3$_1$, H8/38347 Group and H8/38447 Group)**