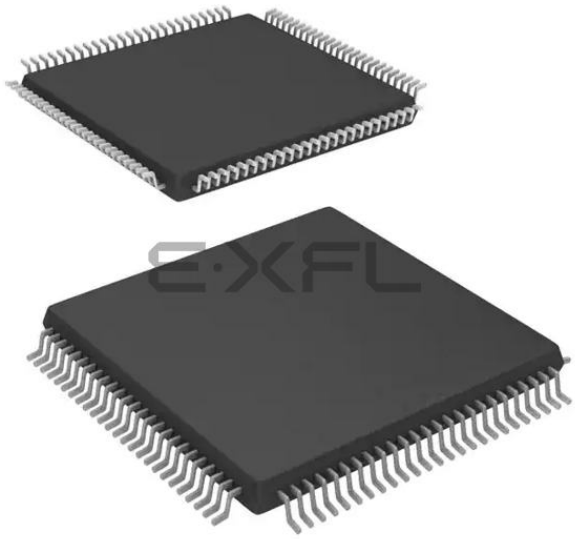

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38344xwv

2.5.7 System Control Instructions

Table 2.10 describes the system control instructions. Figure 2.9 shows their object code formats.

Table 2.10 System Control Instructions

Instruction	Size*	Function
RTE	—	Returns from an exception-handling routine
SLEEP	—	Causes a transition from active mode to a power-down mode. See section 5, Power-Down Modes, for details.
LDC	B	Rs → CCR, #IMM → CCR Moves immediate data or general register contents to the condition code register
STC	B	CCR → Rd Copies the condition code register to a specified general register
ANDC	B	CCR ∧ #IMM → CCR Logically ANDs the condition code register with immediate data
ORC	B	CCR ∨ #IMM → CCR Logically ORs the condition code register with immediate data
XORC	B	CCR ⊕ #IMM → CCR Logically exclusive-ORs the condition code register with immediate data
NOP	—	PC + 2 → PC Only increments the program counter

Note: * Size: Operand size
B: Byte

Section 3 Exception Handling

3.1 Overview

Exception handling is performed in the H8/3847R Group when a reset or interrupt occurs. Table 3.1 shows the priorities of these two types of exception handling.

Table 3.1 Exception Handling Types and Priorities

Priority	Exception Source	Time of Start of Exception Handling
High	Reset	Exception handling starts as soon as the reset state is cleared
▲	Interrupt	When an interrupt is requested, exception handling starts after execution of the present instruction or the exception handling in progress is completed
Low		

3.2 Reset

3.2.1 Overview

A reset is the highest-priority exception. The internal state of the CPU and the registers of the on-chip peripheral modules are initialized.

3.2.2 Reset Sequence

As soon as the $\overline{\text{RES}}$ pin goes low, all processing is stopped and the chip enters the reset state.

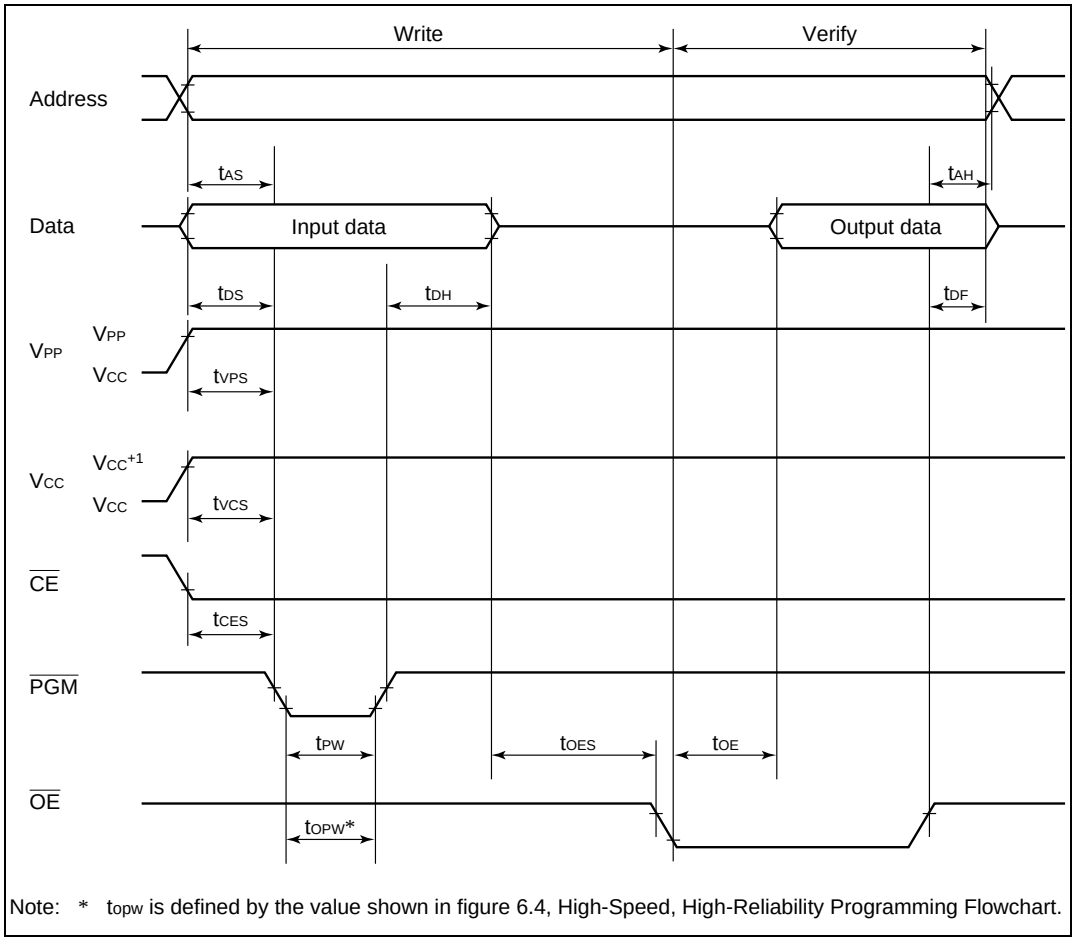
To make sure the chip is reset properly, observe the following precautions.

- At power on: Hold the $\overline{\text{RES}}$ pin low until the clock pulse generator output stabilizes.
- Resetting during operation: Hold the $\overline{\text{RES}}$ pin low for at least 10 system clock cycles.

Reset exception handling takes place as follows.

- The CPU internal state and the registers of on-chip peripheral modules are initialized, with the I bit of the condition code register (CCR) set to 1.
- The PC is loaded from the reset exception handling vector address (H'0000 to H'0001), after which the program starts executing from the address indicated in PC.

Figure 6.5 shows a PROM write/verify timing diagram.



Note: * t_{opw} is defined by the value shown in figure 6.4, High-Speed, High-Reliability Programming Flowchart.

Figure 6.5 PROM Write/Verify Timing

8. Do not change the TEST pin and P24 pin input levels in boot mode.

Table 6.9 Boot Mode Operation

Item	Host Operation Processing Contents	LSI Operation Processing Contents
		Branches to boot program at reset-start.
Bit rate adjustment	Continuously transmits data H'00 at specified bit rate.	· Measures low-level period of receive data H'00. · Calculates bit rate and sets it in BRR of SCI3. · Transmits data H'00 to the host to indicate that the adjustment has ended.
Flash memory erase	Transmits data H'55 when data H'00 is received and no error occurs.	Checks flash memory data, erases all flash memory blocks in case of written data existing, and transmits data H'AA to host. (If erase could not be done, transmits data H'FF to host and aborts operation.)
Transfer of programming control program	Transmits number of bytes (N) of programming control program to be transferred as 2-byte data (low-order byte following high-order byte)	Echobacks the 2-byte received data to host.
Transfer of programming control program (repeated for N times)	Transmits 1-byte of programming control program	Echobacks received data to host and also transfers it to RAM.
Execution of Programming control program		Transmits 1-byte data H'AA to host. Branches to programming control program transferred to on-chip RAM and starts execution.

Table 6.10 Oscillating Frequencies (f_{OSC}) for which Automatic Adjustment of LSI Bit Rate Is Possible

Product Group	Host Bit Rate	Oscillating Frequencies (f_{OSC}) Range of LSI
H8/38347F-ZTAT	19,200 bps	16 MHz
H8/38344F-ZTAT	9,600 bps	8 to 16 MHz
H8/38447F-ZTAT	4,800 bps	6 to 16 MHz
H8/38444F-ZTAT	2,400 bps	2 to 16 MHz
	1,200 bps	2 to 16 MHz

Port	Description	Pins	Other Functions	Function Switching Registers
Port 3	• 8-bit I/O port • MOS input pull-up option • Large-current port (H8/3847R Group, H8/38347 Group and H8/38447 Group)	$P3_7$/AEVL $P3_6$/AEVH $P3_5$/TXD_{31} $P3_4$/RXD_{31} $P3_3$/SCK_{31}	SCI3-1 data output (TXD_{31}), data input (RXD_{31}), clock input/output (SCK_{31}), and asynchronous counter event inputs AEVL, AEVH	PMR3 SCR31 SMR31
		$P3_2$/$\overline{RESO}$*1 $P3_1$/UD/EXCL*2 $P3_0$/PWM	Reset output*1, timer C count-up/down select input, and 14-bit PWM output, external subclock input*2	PMR2 PMR3
Port 4	• 1-bit input port • 3-bit I/O port	$P4_3$/$\overline{IRQ}_0$	External interrupt 0	PMR3
		$P4_2$/TXD_{32} $P4_1$/RXD_{32} $P4_0$/SCK_{32}	SCI3-2 data output (TXD_{32}), data input (RXD_{32}), clock input/output (SCK_{32})	SCR32 SMR32
Port 5	• 8-bit I/O port • MOS input pull-up option	$P5_7$ to $P5_0$/ $\overline{WKP}_7$ to $\overline{WKP}_0$/ SEG_8 to SEG_1	Wakeup input ($\overline{WKP}_7$ to $\overline{WKP}_0$), segment output (SEG_8 to SEG_1)	PMR5 LPCR
Port 6	• 8-bit I/O port • MOS input pull-up option	$P6_7$ to $P6_0$/ SEG_{16} to SEG_9	Segment output (SEG_{16} to SEG_9)	LPCR
Port 7	• 8-bit I/O port	$P7_7$ to $P7_0$/ SEG_{24} to SEG_{17}	Segment output (SEG_{24} to SEG_{17})	LPCR
Port 8	• 8-bit I/O port	$P8_7$ to $P8_0$/ SEG_{32} to SEG_{25}	Segment output (SEG_{32} to SEG_{25})	LPCR
Port 9	• 8-bit I/O port	$P9_7$/SEG_{40}/CL_1*3 $P9_6$/SEG_{39}/CL_2*3 $P9_5$/SEG_{38}/DO*3 $P9_4$/SEG_{37}/M*3 $P9_3$ to $P9_0$/ SEG_{36} to SEG_{33}	• Segment output (SEG_{40} to SEG_{37}) • Latch clock (CL_1)*3, shift clock (CL_2)*3, display data (DO)*3 and alternating signal (M)*3 for external expansion of segment • Segment output (SEG_{36} to SEG_{33})	LPCR
Port A	• 4-bit I/O port	PA_3 to PA_0/ COM_4 to COM_1	Common output (COM_4 to COM_1)	LPCR
Port B	• 8-bit input port	PB_7 to PB_0/ AN_7 to AN_0	A/D converter analog input	AMR
Port C	• 4-bit input port	PC_3 to PC_0/ AN_{11} to AN_8	A/D converter analog input	AMR

Notes: 1. The $\overline{RESO}$ function is not implemented in the H8/38347 Group and H8/38447 Group.
2. The EXCL function is only implemented in the H8/38347 Group and H8/38447 Group.
3. The external expansion function for LCD segments is not implemented in the H8/38347 Group and H8/38447 Group.

8.8 Port 7

8.8.1 Overview

Port 7 is an 8-bit I/O port, configured as shown in figure 8.7.

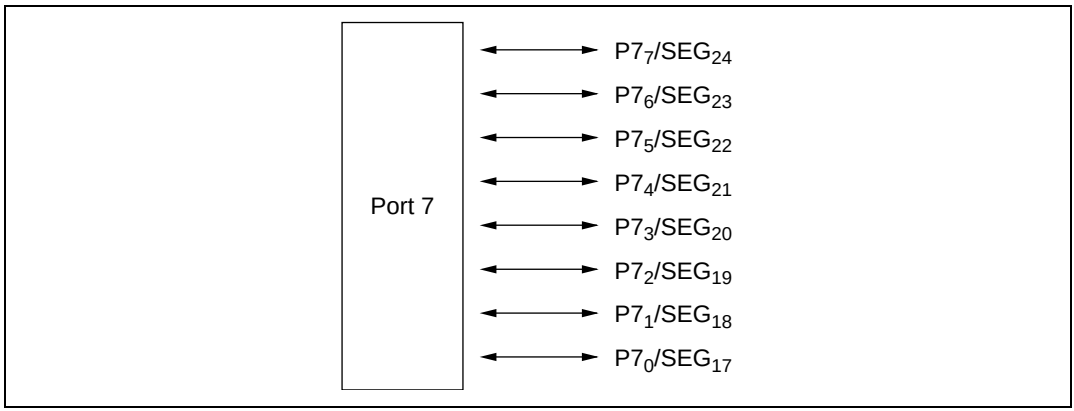


Figure 8.7 Port 7 Pin Configuration

8.8.2 Register Configuration and Description

Table 8.20 shows the port 7 register configuration.

Table 8.20 Port 7 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 7	PDR7	R/W	H'00	H'FFDA
Port control register 7	PCR7	W	H'00	H'FFEA

4. Register Configuration

Table 9.6 shows the register configuration of timer C.

Table 9.6 Timer C Registers

Name	Abbr.	R/W	Initial Value	Address
Timer mode register C	TMC	R/W	H'18	H'FFB4
Timer counter C	TCC	R	H'00	H'FFB5
Timer load register C	TLC	W	H'00	H'FFB5
Clock stop register 1	CKSTPR1	R/W	H'FF	H'FFFA

9.3.2 Register Descriptions

1. Timer Mode Register C (TMC)

Bit	7	6	5	4	3	2	1	0
	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0
Initial value	0	0	0	1	1	0	0	0
Read/Write	R/W	R/W	R/W	—	—	R/W	R/W	R/W

TMC is an 8-bit read/write register for selecting the auto-reload function and input clock, and performing up/down-counter control.

Upon reset, TMC is initialized to H'18.

Bit 7: Auto-reload function select (TMC7)

Bit 7 selects whether timer C is used as an interval timer or auto-reload timer.

Bit 7 TMC7	Description	
0	Interval timer function selected	(initial value)
1	Auto-reload function selected	

2. Timer Counter C (TCC)

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCC is an 8-bit read-only up-counter, which is incremented by internal clock or external event input. The clock source for input to this counter is selected by bits TMC2 to TMC0 in timer mode register C (TMC). TCC values can be read by the CPU at any time.

When TCC overflows from H'FF to H'00 or to the value set in TLC, or underflows from H'00 to H'FF or to the value set in TLC, the IRRTC bit in IRR2 is set to 1.

TCC is allocated to the same address as TLC.

Upon reset, TCC is initialized to H'00.

3. Timer Load Register C (TLC)

Bit	7	6	5	4	3	2	1	0
	TLC7	TLC6	TLC5	TLC4	TLC3	TLC2	TLC1	TLC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLC is an 8-bit write-only register for setting the reload value of timer counter C (TCC).

When a reload value is set in TLC, the same value is loaded into timer counter C as well, and TCC starts counting up from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded into TCC. Accordingly, overflow/underflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLC as to TCC.

Upon reset, TLC is initialized to H'00.

Bit 2: Watchdog timer on (WDON)

Bit 2 enables watchdog timer operation.

Bit 2 WDON	Description	
0	Watchdog timer operation is disabled Clearing condition: Reset, or when TCSRWE = 1 and 0 is written in both B2WI and WDON	(initial value)
1	Watchdog timer operation is enabled Setting condition: When TCSRWE = 1 and 0 is written in B2WI and 1 is written in WDON	

Counting starts when this bit is set to 1, and stops when this bit is cleared to 0.

Bit 1: Bit 0 write inhibit (B0WI)

Bit 1 controls the writing of data to bit 0 in TCSRW.

Bit 1 B0WI	Description	
0	Bit 0 is write-enabled	
1	Bit 0 is write-protected	(initial value)

This bit is always read as 1. Data written to this bit is not stored.

Bit 0: Watchdog timer reset (WRST)

Bit 0 indicates that TCW has overflowed, generating an internal reset signal. The internal reset signal generated by the overflow resets the entire chip. WRST is cleared to 0 by a reset from the $\overline{\text{RES}}$ pin, or when software writes 0.

Bit 0 WRST	Description
0	Clearing condition: Reset by $\overline{\text{RES}}$ pin When TCSRWE = 1, and 0 is written in both B0WI and WRST
1	Setting condition: When TCW overflows and an internal reset signal is generated

10.2.5 Interrupt Source

SCI1 has one interrupt source: transfer completion.

When SCI1 completes transfer, IRRS1 is set to 1 in IRR1. The SCI1 interrupt source can be enabled or disabled by the IENS1 bit in IENR1.

For details, see section 3.3, Interrupts.

10.2.6 Application Notes

(1) When SCK_1 is designated as an input pin and an external clock is selected as the clock source, the external clock must not be input before transfer operation is started by setting STF to 1 in SCSR1.

(2) In subactive or subsleep mode, SCI1 can be used only when the CPU operation clock is $\phi_W/2$.

(3) Do not read or write to SCSRI during serial transfer. Use one of the following methods to confirm that serial transfer has ended.

(a) Use SCI1 interrupt exception handling.

Set IENSI to 1 in IENR1, and execute interrupt exception handling.

(b) Perform IRR1 polling.

Confirm that IRRS1 has been set to 1 in IRRI while SCI interrupts are disabled (IENS1 = 0 in IEHR1).

Bit 1: Multiprocessor bit receive (MPBR)

Bit 1 stores the multiprocessor bit in a receive character during multiprocessor format reception in asynchronous mode.

Bit 1 is a read-only bit and cannot be modified.

Bit 1 MPBR	Description	
0	Data in which the multiprocessor bit is 0 has been received*	(initial value)
1	Data in which the multiprocessor bit is 1 has been received	

Note: * When bit RE is cleared to 0 in SCR3 with the multiprocessor format, bit MPBR is not affected and retains its previous state.

Bit 0: Multiprocessor bit transfer (MPBT)

Bit 0 stores the multiprocessor bit added to transmit data when transmitting in asynchronous mode. The bit MPBT setting is invalid when synchronous mode is selected, when the multiprocessor communication function is disabled, and when not transmitting.

Bit 0 MPBT	Description	
0	A 0 multiprocessor bit is transmitted	(initial value)
1	A 1 multiprocessor bit is transmitted	

8. Bit Rate Register (BRR)

Bit	7	6	5	4	3	2	1	0
	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BRR is an 8-bit register that designates the transmit/receive bit rate in accordance with the baud rate generator operating clock selected by bits CKS1 and CKS0 of the serial mode register (SMR).

BRR can be read or written by the CPU at any time.

BRR is initialized to H'FF upon reset, and in standby, module standby, or watch mode.

10.3.3 Operation

1. Overview

SCI3 can perform serial communication in two modes: asynchronous mode in which synchronization is provided character by character, and synchronous mode in which synchronization is provided by clock pulses. The serial mode register (SMR) is used to select asynchronous or synchronous mode and the data transfer format, as shown in table 10.11.

The clock source for SCI3 is determined by bit COM in SMR and bits CKE1 and CKE0 in SCR3, as shown in table 10.12.

a. Asynchronous mode

- Choice of 5-, 7-, or 8-bit data length
- Choice of parity addition, multiprocessor bit addition, and addition of 1 or 2 stop bits. (The combination of these parameters determines the data transfer format and the character length.)
- Framing error (FER), parity error (PER), overrun error (OER), and break detection during reception
- Choice of internal or external clock as the clock source

  When internal clock is selected: SCI3 operates on the baud rate generator clock, and a clock with the same frequency as the bit rate can be output.

  When external clock is selected: A clock with a frequency 16 times the bit rate must be input. (The on-chip baud rate generator is not used.)

b. Synchronous mode

- Data transfer format: Fixed 8-bit data length
- Overrun error (OER) detection during reception
- Choice of internal or external clock as the clock source

  When internal clock is selected: SCI3 operates on the baud rate generator clock, and a serial clock is output.

  When external clock is selected: The on-chip baud rate generator is not used, and SCI3 operates on the input serial clock.

- Transmitting

Figure 10.11 shows an example of a flowchart for data transmission. This procedure should be followed for data transmission after initializing SCI3.

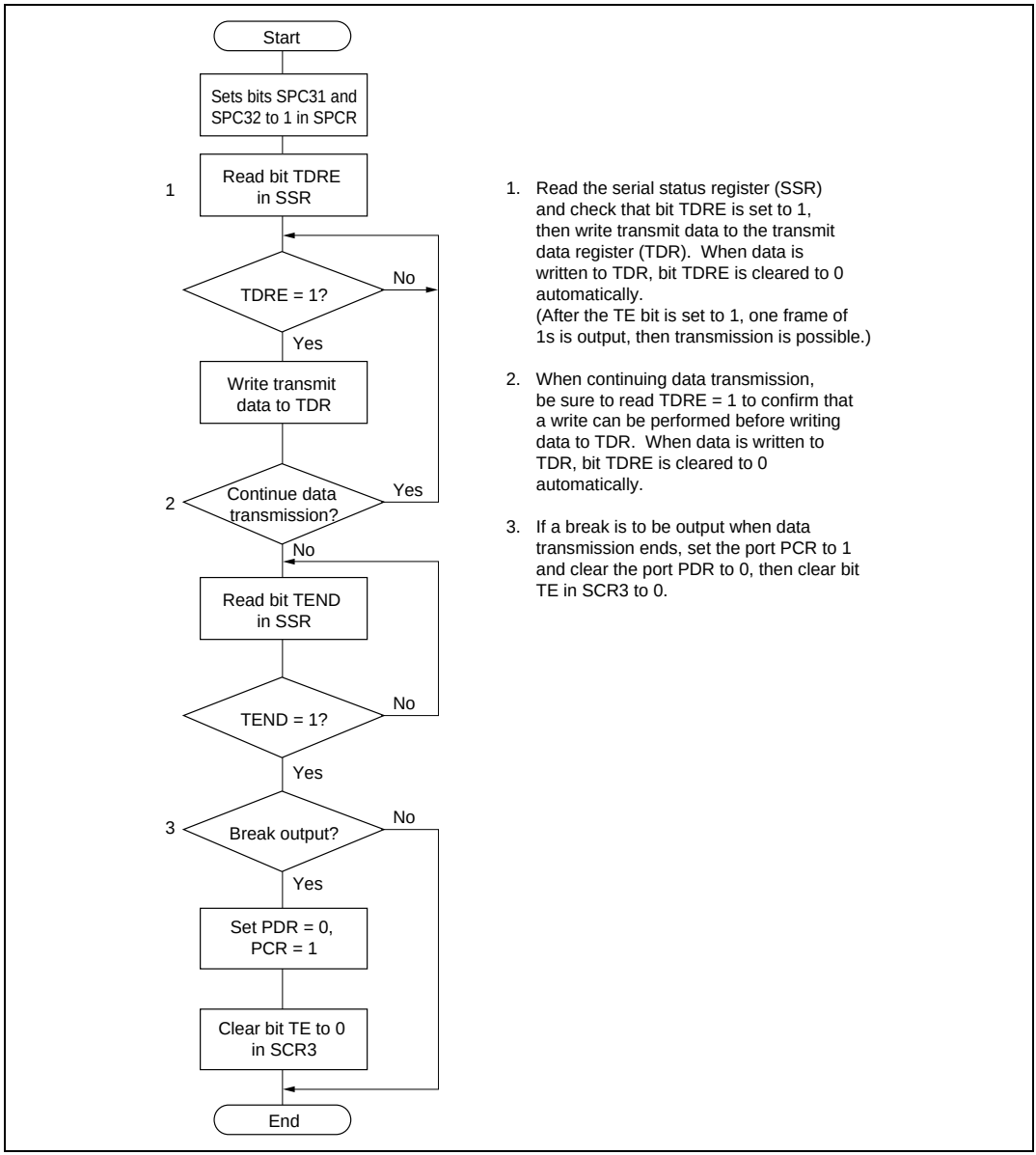


Figure 10.11 Example of Data Transmission Flowchart (Asynchronous Mode)

SCI3 operates as follows when transmitting data.

SCI3 monitors bit TDRE in SSR, and when it is cleared to 0, recognizes that data has been written to TDR and transfers data from TDR to TSR. It then sets bit TDRE to 1 and starts transmitting. If bit TIE in SCR3 is set to 1 at this time, a TXI request is made.

Serial data is transmitted from the TXD pin using the relevant data transfer format in table 10.14. When the stop bit is sent, SCI3 checks bit TDRE. If bit TDRE is cleared to 0, SCI3 transfers data from TDR to TSR, and when the stop bit has been sent, starts transmission of the next frame. If bit TDRE is set to 1 bit TEND in SSR bit is set to 1, the mark state, in which 1s are transmitted, is established after the stop bit has been sent. If bit TEIE in SCR3 is set to 1 at this time, a TEI request is made.

Figure 10.23 shows an example of the operation when transmitting using the multiprocessor format.

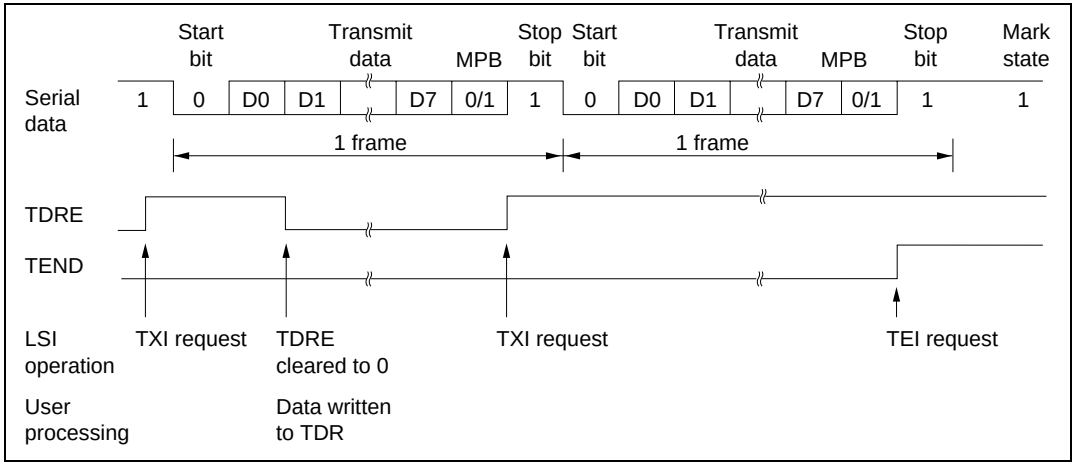


Figure 10.23 Example of Operation when Transmitting Using Multiprocessor Format (8-bit data, multiprocessor bit, 1 stop bit)

- Multiprocessor receiving

Figure 10.24 shows an example of a flowchart for multiprocessor data reception. This procedure should be followed for multiprocessor data reception after initializing SCI3.

11.2.2 PWM Data Registers U and L (PWDRU, PWDRL)

PWDRU

Bit	7	6	5	4	3	2	1	0
	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

PWDRL

Bit	7	6	5	4	3	2	1	0
	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PWDRU and PWDRL form a 14-bit write-only register, with the upper 6 bits assigned to PWDRU and the lower 8 bits to PWDRL. The value written to PWDRU and PWDRL gives the total high-level width of one PWM waveform cycle.

When 14-bit data is written to PWDRU and PWDRL, the register contents are latched in the PWM waveform generator, updating the PWM waveform generation data. The 14-bit data should always be written in the following sequence:

1. Write the lower 8 bits to PWDRL.

2. Write the upper 6 bits to PWDRU.

PWDRU and PWDRL are write-only registers. If they are read, all bits are read as 1.

Upon reset, PWDRU and PWDRL are initialized to H'C000.

15.2.3 AC Characteristics

Table 15.3 lists the control signal timing, and tables 15.4 and 15.5 list the serial interface timing.

Table 15.3 Control Signal Timing

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –20°C to +75°C*4 (including subactive mode) unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2	—	16	MHz	V_{CC} = 4.5 V to 5.5 V	*2
			2	—	10		V_{CC} = 2.7 V to 5.5 V	
			2	—	4		V_{CC} = 1.8 V to 5.5 V	
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC_1, OSC_2	62.5	—	500 (1000)	ns	V_{CC} = 4.5 V to 5.5 V	Figure 15.1 *2 *3
			100	—	500 (1000)		V_{CC} = 2.7 V to 5.5 V	Figure 15.1 *3
			250	—	500 (1000)		V_{CC} = 1.8 V to 5.5 V	
System clock (ϕ) cycle time	t_{cyc}		2	—	128	t_{OSC}		
			—	—	244.1	µs		
Subclock oscillation frequency	f_W	X_1, X_2	—	32.768 or 38.4	—	kHz		
Watch clock (ϕ_W) cycle time	t_W	X_1, X_2	—	30.5 or 26.0	—	µs		Figure 15.1
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}		2	—	8	t_W		*1
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time	t_{rc}	OSC_1, OSC_2	—	20	45	µs	Figure 15.10 V_{CC} = 2.2 V to 5.5 V	Figure 15.10 *2
			—	0.1	8	ms	Figure 15.10 V_{CC} = 2.2 V to 5.5 V	Figure 15.10
			—	—	50	ms	Except the above	
		X_1, X_2	—	—	2.0	s		

Table 15.21 Serial Interface (SCI3-1, SCI3-2) Timing

Item		Symbol	Values Min	Typ	Max	Unit	Test Conditions	Reference Figure
Input clock cycle	Asynchronous	t_{Scyc}	4	—	—	t_{cyc} or		Figure 15.6
	Synchronous		6	—	—	t_{subcyc}		
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{Scyc}		Figure 15.6
Transmit data delay time (synchronous)		t_{TXD}	—	—	1	t_{cyc} or t_{subcyc}		Figure 15.7
Receive data setup time (synchronous)		t_{RXS}	400.0	—	—	ns		Figure 15.7
Receive data hold time (synchronous)		t_{RXH}	400.0	—	—	ns		Figure 15.7

FLMCR1—Flash Memory Control Register 1 H'F020 Flash Memory

Bit	7	6	5	4	3	2	1	0
	—	SWE	ESU	PSU	EV	PV	E	P
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Program

0	Program mode cleared (initial value)
1	Transition to program mode [Setting condition] When SWE = 1 and PSU = 1

Erase

0	Erase mode cleared (initial value)
1	Transition to erase mode [Setting condition] When SWE = 1 and ESU = 1

Program-Verify

0	Program-verify mode cleared (initial value)
1	Transition to program-verify mode [Setting condition] When SWE = 1

Erase-Verify

0	Erase-verify mode cleared (initial value)
1	Transition to erase-verify mode [Setting condition] When SWE = 1

Program-Setup

0	Program-setup cleared (initial value)
1	Program setup [Setting condition] When SWE = 1

Erase-Setup

0	Erase-setup cleared (initial value)
1	Erase setup [Setting condition] When SWE = 1

Software write enable bit

0	Writing/erasing disabled (initial value)
1	Writing/erasing enabled

Product Type				Product Code	Mark Code	Package (Package Code)
H8/3847R Group	H8/3845R	Mask ROM versions	Regular products	HD6433845RH	HD6433845R(***)H	100-pin QFP (FP-100B)
				HD6433845RF	HD6433845R(***)F	100-pin QFP (FP-100A)
				HD6433845RX	HD6433845R(***)X	100-pin TQFP (TFP-100B)
				HD6433845RW	HD6433845R(***)W	100-pin TQFP (TFP-100G)
				HCD6433845R	—	Die
		Mask ROM versions	Wide-range specification products	HD6433845RD	HD6433845R(***)H	100-pin QFP (FP-100B)
				HD6433845RE	HD6433845R(***)F	100-pin QFP (FP-100A)
				HD6433845RL	HD6433845R(***)X	100-pin TQFP (TFP-100B)
				HD6433845RWI	HD6433845R(***)W	100-pin TQFP (TFP-100G)
	H8/3846R	Mask ROM versions	Regular products	HD6433846RH	HD6433846R(***)H	100-pin QFP (FP-100B)
				HD6433846RF	HD6433846R(***)F	100-pin QFP (FP-100A)
				HD6433846RX	HD6433846R(***)X	100-pin TQFP (TFP-100B)
				HD6433846RW	HD6433846R(***)W	100-pin TQFP (TFP-100G)
				HCD6433846R	—	Die
			Wide-range specification products	HD6433846RD	HD6433846R(***)H	100-pin QFP (FP-100B)
				HD6433846RE	HD6433846R(***)F	100-pin QFP (FP-100A)
				HD6433846RL	HD6433846R(***)X	100-pin TQFP (TFP-100B)
				HD6433846RWI	HD6433846R(***)W	100-pin TQFP (TFP-100G)
	H8/3847R	Mask ROM versions	Regular products	HD6433847RH	HD6433847R(***)H	100-pin QFP (FP-100B)
				HD6433847RF	HD6433847R(***)F	100-pin QFP (FP-100A)
				HD6433847RX	HD6433847R(***)X	100-pin TQFP (TFP-100B)
				HD6433847RW	HD6433847R(***)W	100-pin TQFP (TFP-100G)
				HCD6433847R	—	Die
			Wide-range specification products	HD6433847RD	HD6433847R(***)H	100-pin QFP (FP-100B)
				HD6433847RE	HD6433847R(***)F	100-pin QFP (FP-100A)
				HD6433847RL	HD6433847R(***)X	100-pin TQFP (TFP-100B)
				HD6433847RWI	HD6433847R(***)W	100-pin TQFP(TFP-100G)
		ZTAT versions	Regular products	HD6473847RH	HD6473847RH	100-pin QFP (FP-100B)
				HD6473847RF	HD6473847RF	100-pin QFP (FP-100A)
				HD6473847RX	HD6473847RX	100-pin TQFP (TFP-100B)
				HD6473847RW	HD6473847RW	100-pin TQFP(TFP-100G)
			Wide-range specification products	HD6473847RD	HD6473847RH	100-pin QFP (FP-100B)
				HD6473847RE	HD6473847RF	100-pin QFP (FP-100A)
				HD6473847RL	HD6473847RX	100-pin TQFP (TFP-100B)
				HD6473847RWI	HD6473847RW	100-pin TQFP (TFP-100G)