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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38347hv

Figures

Section 1 Overview

Section 2 CPU

Appendix F Package Dimensions

Appendix G Specifications of Chip Form

Section 13 LCD Controller/Driver

Section 15 Electrical Characteristics

2.1.3 Register Configuration

Figure 2.1 shows the register structure of the H8/300L CPU. There are two groups of registers: the general registers and control registers.

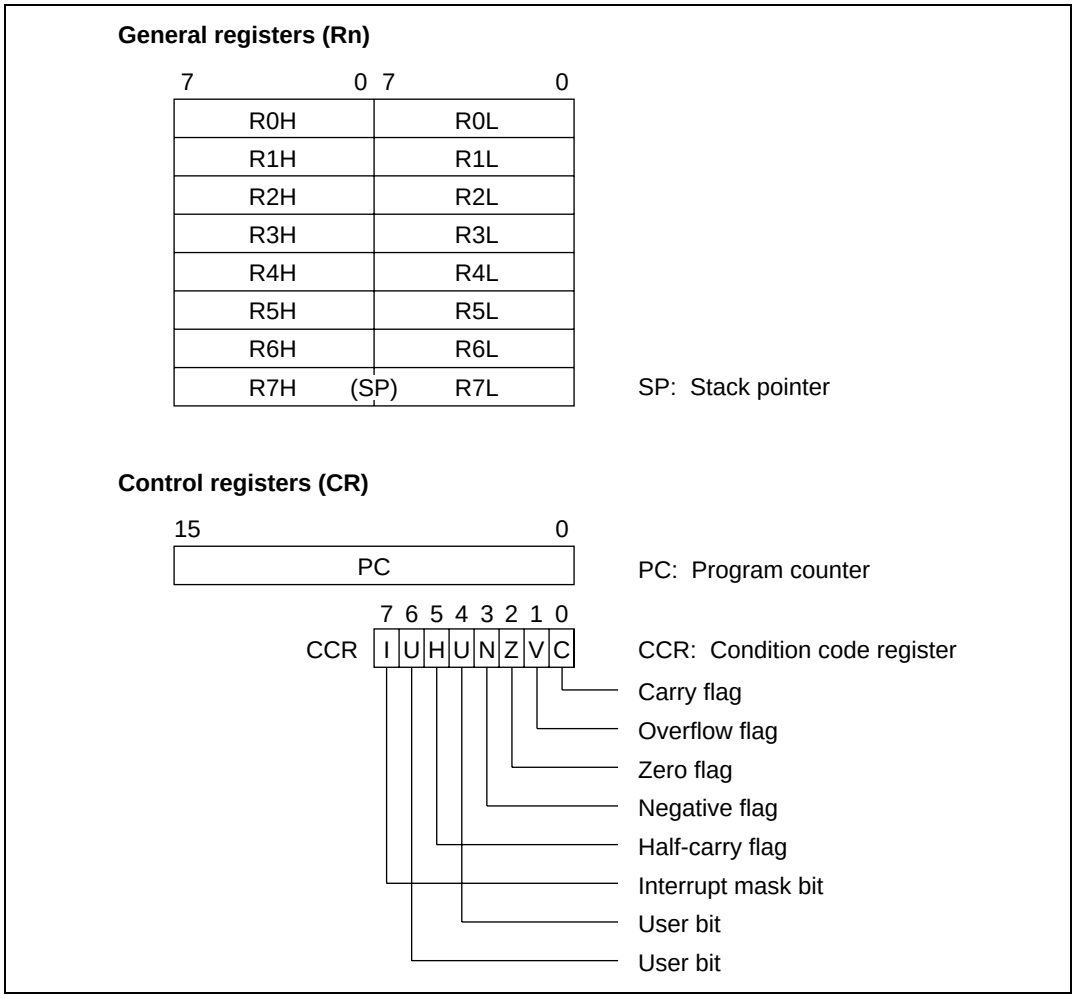


Figure 2.1 CPU Registers

3.4.2 Notes on Rewriting Port Mode Registers

When a port mode register is rewritten to switch the functions of external interrupt pins, the following points should be observed.

When an external interrupt pin function is switched by rewriting the port mode register that controls pins $\overline{IRQ}_4$ to $\overline{IRQ}_0$, $\overline{WKP}_7$ to $\overline{WKP}_0$, the interrupt request flag may be set to 1 at the time the pin function is switched, even if no valid interrupt is input at the pin. Be sure to clear the interrupt request flag to 0 after switching pin functions. Table 3.5 shows the conditions under which interrupt request flags are set to 1 in this way.

Table 6.7 Division of Blocks to Be Erased

EBR	Bit Name	Block (Size)	Address
0	EB0	EB0 (1 Kbyte)	H'0000 to H'03FF
1	EB1	EB1 (1 Kbyte)	H'0400 to H'07FF
2	EB2	EB2 (1 Kbyte)	H'0800 to H'0BFF
3	EB3	EB3 (1 Kbyte)	H'0C00 to H'0FFF
4	EB4	EB4 (28 Kbytes)	H'1000 to H'7FFF
5	EB5	EB5 (16 Kbyte)	H'8000 to H'BFFF
6	EB6	EB6 (8 Kbyte)	H'C000 to H'DFFF
7	EB7	EB7 (4 Kbytes)	H'E000 to H'EFFF

6.6.4 Flash Memory Power Control Register (FLPWCR)

Bit	7	6	5	4	3	2	1	0
	PDWND	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	—	—	—	—	—	—	—

FLPWCR enables or disables a transition to the flash memory power-down mode when the LSI switches to subactive mode. The power supply circuit can be read in the subactive mode, although it is partly halted in the power-down mode.

Bit 7—Power-down Disable (PDWND)

This bit selects the power-down mode of the flash memory when a transition to the subactive mode is made.

Bit 7 PDWND	Description
0	When this bit is 0 and a transition is made to the subactive mode, the flash memory enters the power-down mode. (initial value)
1	When this bit is 1, the flash memory remains in the normal mode even after a transition is made to the subactive mode.

Bits 6 to 0—Reserved

These bits are always read as 0 and cannot be modified.

by re-setting the P or E bit. However, PV and EV bit setting is enabled, and a transition can be made to verify mode. Error protection can be cleared only by a power-on reset.

6.10 Programmer Mode

In programmer mode, a PROM programmer can be used to perform programming/erasing via a socket adapter, just as a discrete flash memory. Use a PROM programmer that supports the MCU device type with the on-chip Renesas Technology (former Hitachi Ltd.) 64-Kbyte flash memory (F-ZTAT64V3). A 10-MHz input clock is required. For the conditions for transition to programmer mode, see table 6.8.

6.10.1 Socket Adapter

The socket adapter converts the pin allocation of the F-ZTAT device to that of the discrete flash memory HN28F101. The address of the on-chip flash memory is H'0000 to H'EFFF. Figure 6.12 shows a socket-adapter-pin correspondence diagram.

6.10.2 Programmer Mode Commands

The following commands are supported in programmer mode.

- Memory Read Mode
- Auto-Program Mode
- Auto-Erase Mode
- Status Read Mode

Status polling is used for auto-programming, auto-erasing, and status read modes. In status read mode, detailed internal information is output after the execution of auto-programming or auto-erasing. Table 6.14 shows the sequence of each command. In auto-programming mode, 129 cycles are required since 128 bytes are written at the same time. In memory read mode, the number of cycles depends on the number of address write cycles (n).

- H8/38347 Group and H8/38447 Group

Bit	7	6	5	4	3	2	1	0
	EXCL	—	POF1	—	—	SO1	SI1	SCK1
Initial value	0	1	0	1	1	0	0	0
Read/Write	R/W	—	R/W	—	—	R/W	R/W	R/W

PMR2 is an 8-bit read/write register that controls the selection of pin functions for pins $P2_0$, $P2_1$, and $P2_3$, the PMOS on/off state for the $P2_2/SO_1$ pin, and external clock input to pin P31.

Upon reset, PMR2 is initialized to H'58.

- H8/3847R Group and H8/3847S Group

Bit 7: Reserved bit

Bit 7 is reserved. It is always read as 1 and cannot be modified.

- H8/38347 Group and H8/38447 Group

Bit 7: P31/UD/EXCL pin function switch (EXCL)

This bit selects whether pin P31/UD/EXCL is used as P31/UD or as EXCL. When the pin is used as EXCL an external clock should be input to it. See section 4, Clock Pulse Generators, for a connection example.

Bit 7 EXCL	Description	
0	Functions as P31/UD I/O pin	(initial value)
1	Functions as EXCL input pin	

Bits 6, 4, and 3: Reserved bits

Bits 6, 4, and 3 are reserved; they are always read as 1 and cannot be modified.

Bit 5: $P2_2/SO_1$ pin PMOS control (POF1)

This bit controls the on/off state of the $P2_2/SO_1$ pin output buffer PMOS.

Bit 5 POF1	Description	
0	CMOS output	(initial value)
1	NMOS open-drain output	

8.6.4 Pin States

Table 8.16 shows the port 5 pin states in each operating mode.

Table 8.16 Port 5 Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P5_7/\overline{WKP_7}/SEG_8$ to $P5_0/\overline{WKP_0}/SEG_1$	High-impedance	Retains previous state	Retains previous state	High-impedance*	Retains previous state	Functional	Functional

Note: * A high-level signal is output when the MOS pull-up is in the on state.

8.6.5 MOS Input Pull-Up

Port 5 has a built-in MOS input pull-up function that can be controlled by software. When a PCR5 bit is cleared to 0, setting the corresponding PUCR5 bit to 1 turns on the MOS pull-up for that pin. The MOS pull-up function is in the off state after a reset.

$PCR5_n$	0	0	1
$PUCR5_n$	0	1	*
MOS input pull-up	Off	On	Off

(n = 7 to 0)

*: Don't care

8.9 Port 8

8.9.1 Overview

Port 8 is an 8-bit I/O port configured as shown in figure 8.8.

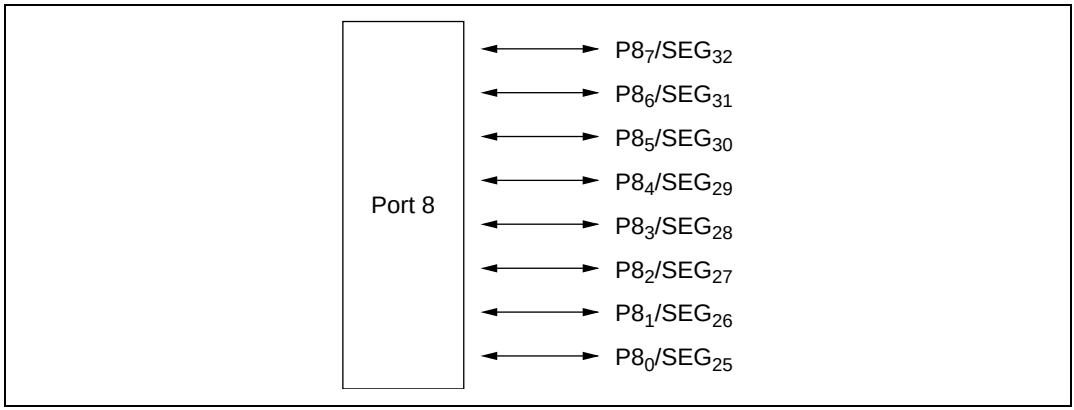


Figure 8.8 Port 8 Pin Configuration

8.9.2 Register Configuration and Description

Table 8.23 shows the port 8 register configuration.

Table 8.23 Port 8 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 8	PDR8	R/W	H'00	H'FFDB
Port control register 8	PCR8	W	H'00	H'FFEB

Bits 3 and 2: Counter clear 1 and 0 (CCLR1, CCLR0)

Bits 3 and 2 specify whether or not TCG is cleared by the rising edge, falling edge, or both edges of the input capture input signal.

Bit 3 CCLR1	Bit 2 CCLR0	Description	
0	0	TCG clearing is disabled	(initial value)
0	1	TCG cleared by falling edge of input capture input signal	
1	0	TCG cleared by rising edge of input capture input signal	
1	1	TCG cleared by both edges of input capture input signal	

Bits 1 and 0: Clock select (CKS1, CKS0)

Bits 1 and 0 select the clock input to TCG from among four internal clock sources.

Bit 1 CKS1	Bit 0 CKS0	Description	
0	0	Internal clock: counting on ϕ/64	(initial value)
0	1	Internal clock: counting on ϕ/32	
1	0	Internal clock: counting on ϕ/2	
1	1	Internal clock: counting on ϕw/4	

5. Clock Stop Register 1 (CKSTPR1)

Bit:	7	6	5	4	3	2	1	0
	S1CKSTP	S31CKSTP	S32CKSTP	ADCKSTP	TGCKSTP	TFCKSTP	TCCKSTP	TACKSTP
Initial value:	1	1	1	1	1	1	1	1
Read/Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CKSTPR1 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to timer G is described here. For details of the other bits, see the sections on the relevant modules.

10.2 SCI1

10.2.1 Overview

Serial communication interface 1 (SCI1) can carry out 8-bit or 16-bit serial data transfer in synchronous mode. It is also provided with a communication function called a Synchronized Serial Bus (SSB) that enables a number of ICs to be controlled.

1. Features

Features of SCI1 are listed below.

- Choice of 8-bit or 16-bit transfer data length
- Choice of 8 internal clocks (ϕ/1024, ϕ/256, ϕ/64, ϕ/32, ϕ/16, ϕ/8, ϕ/4, or ϕ_W/4) or external clock as clock source
- Interrupt request generated on completion of transfer
- Choice of hold mode or latch mode in SSB mode

- Receiving

Figure 10.18 shows an example of a flowchart for data reception. This procedure should be followed for data reception after initializing SCI3.

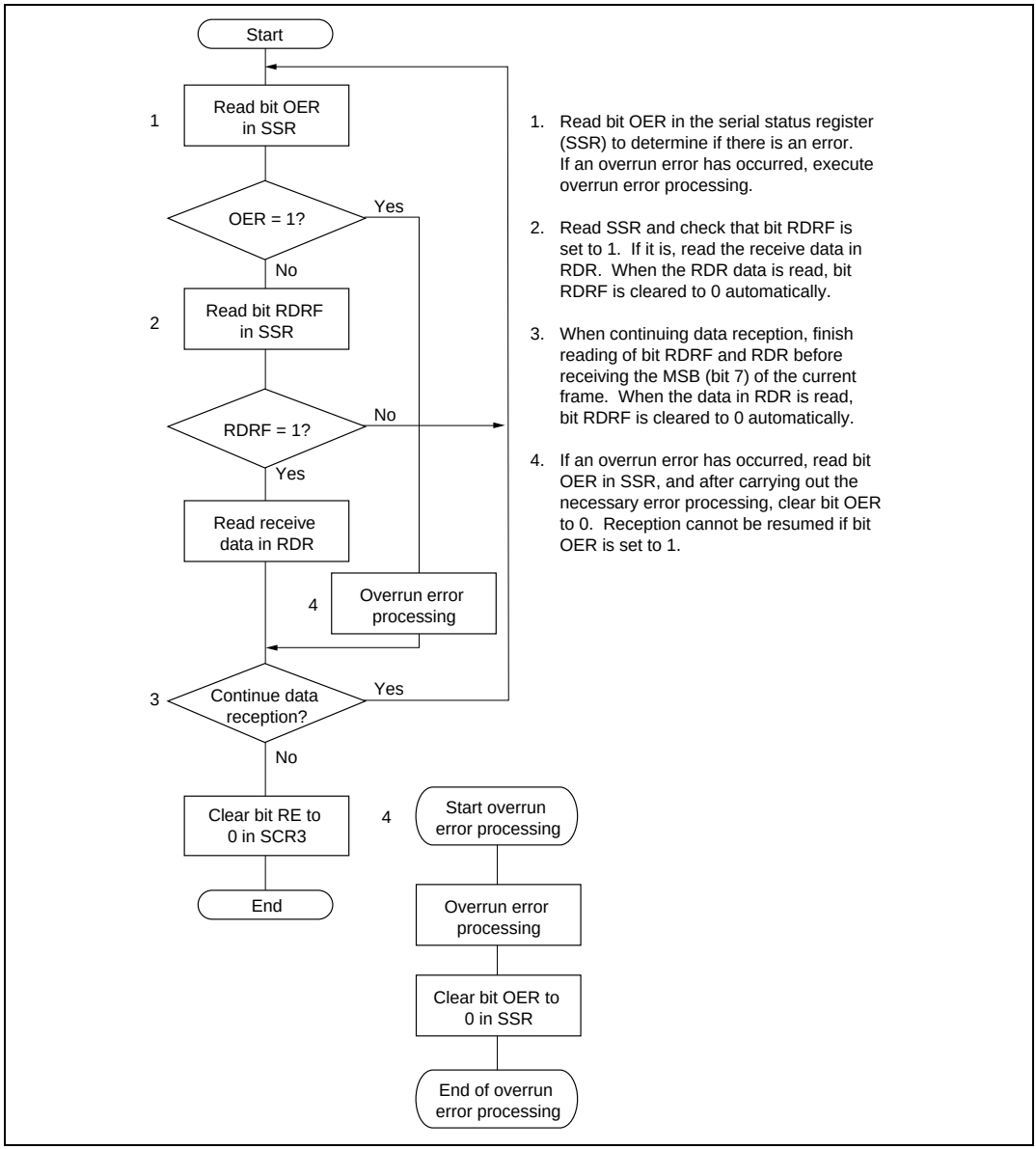


Figure 10.18 Example of Data Reception Flowchart (Synchronous Mode)

12.1.2 Block Diagram

Figure 12.1 shows a block diagram of the A/D converter.

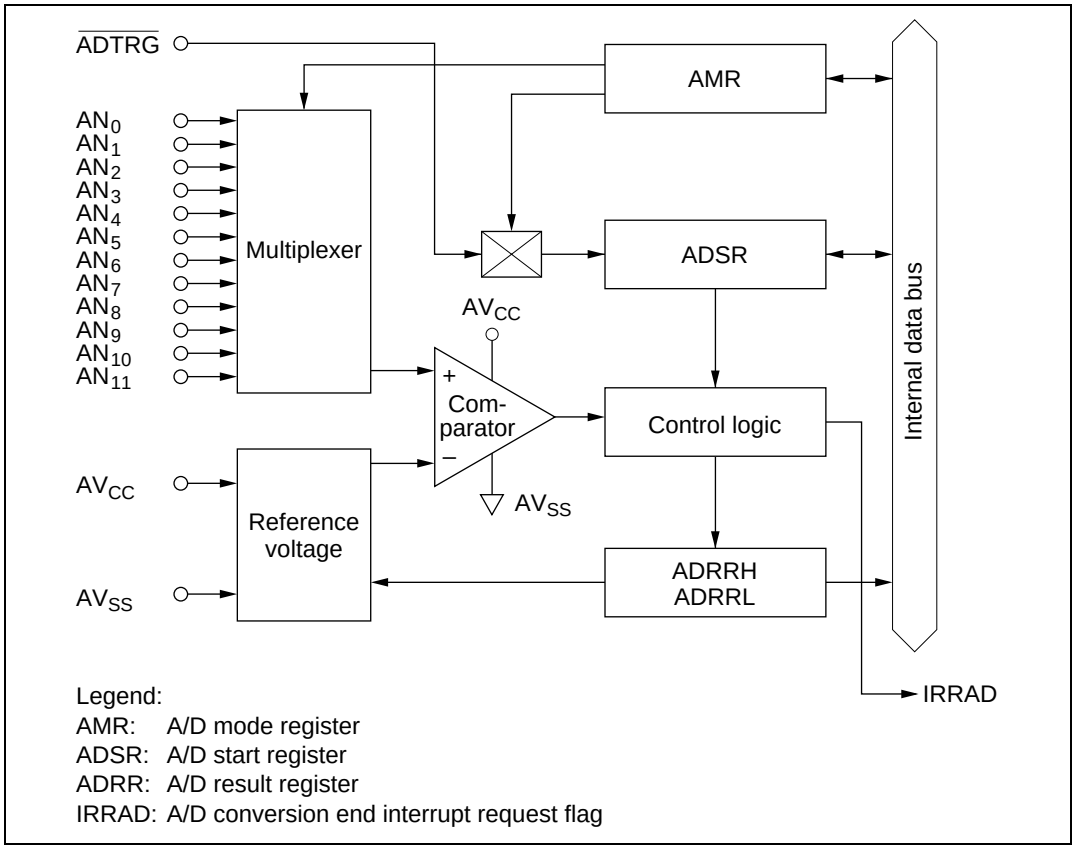


Figure 12.1 Block Diagram of the A/D Converter

15.7 Absolute Maximum Ratings of H8/38347 Group and H8/38447 Group

Table 15.25 lists the absolute maximum ratings.

Table 15.25 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Note
Power supply voltage		V_{CC}	–0.3 to +7.0	V	*1
		CV_{CC}	–0.3 to +4.3	V	
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V	
Input voltage	Other than ports B, C	V_{in}	–0.3 to V_{CC} +0.3	V	
	Ports B, C	AV_{in}	–0.3 to AV_{CC} +0.3	V	
Operating temperature		T_{opr}	–20 to +75*2 (regular specifications)	°C	
			–40 to +85*2 (wide-range temperature specifications)		
			+75*3 (chip shipment specifications)		
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

2. The operating temperature ranges from –20°C to +75°C when programming or erasing the flash memory.

3. The temperature range in which power may be applied to the device is –20 to +75°C.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$P1_0$ to $P1_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, PA_0 to PA_3	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P2_0$ to $P2_7$, $P3_0$ to $P3_7$	—	—	1.0		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
Input/ output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$, OSC_1, X_1, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, PA_0 to PA_3	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7, PC_0 to PC_3	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_0$ to $P1_7$, $P2_4$*6, $P3_0$ to $P3_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$	20	—	200	µA	V_{CC} = 5.0 V, V_{IN} = 0.0 V	
			—	40	—		V_{CC} = 2.7 V, V_{IN} = 0.0 V	Reference value
Input capacitance	C_{in}	All input pins except power supply pin	—	—	15.0	pF	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	

Mnemonic	Operand Size	Operation		Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
				#xx: 8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa: 8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	
BIAND #xx:3, Rd	B	C∧(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BIAND #xx:3, @Rd	B	C∧(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BIAND #xx:3, @aa:8	B	C∧(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BOR #xx:3, Rd	B	C∨(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BOR #xx:3, @Rd	B	C∨(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BIOR #xx:3, Rd	B	C∨(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BIOR #xx:3, @Rd	B	C∨(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BIOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BXOR #xx:3, Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BXOR #xx:3, @Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BIXOR #xx:3, @Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BIXOR #xx:3, @Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BIXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BRA d:8 (BT d:8)	—	PC ← PC+d:8								2			—	—	—	—	—	—	4
BRN d:8 (BF d:8)	—	PC ← PC+2								2			—	—	—	—	—	—	4
BHI d:8	—	If condition	C ∨ Z = 0							2			—	—	—	—	—	—	4
BLS d:8	—	is true then	C ∨ Z = 1							2			—	—	—	—	—	—	4
BCC d:8 (BHS d:8)	—	PC ← PC+d:8	C = 0							2			—	—	—	—	—	—	4
BCS d:8 (BLO d:8)	—	else next;	C = 1							2			—	—	—	—	—	—	4
BNE d:8	—		Z = 0							2			—	—	—	—	—	—	4
BEQ d:8	—		Z = 1							2			—	—	—	—	—	—	4
BVC d:8	—		V = 0							2			—	—	—	—	—	—	4
BVS d:8	—		V = 1							2			—	—	—	—	—	—	4
BPL d:8	—		N = 0							2			—	—	—	—	—	—	4
BMI d:8	—		N = 1							2			—	—	—	—	—	—	4
BGE d:8	—		N⊕V = 0							2			—	—	—	—	—	—	4
BLT d:8	—		N⊕V = 1							2			—	—	—	—	—	—	4
BGT d:8	—		Z ∨ (N⊕V) = 0							2			—	—	—	—	—	—	4
BLE d:8	—		Z ∨ (N⊕V) = 1							2			—	—	—	—	—	—	4

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
SUB	SUB.B Rs, Rd	1					
	SUB.W Rs, Rd	1					
SUBS	SUBS.W #1, Rd	1					
	SUBS.W #2, Rd	1					
POP	POP Rd	1		1			2
PUSH	PUSH Rs	1		1			2
SUBX	SUBX.B #xx:8, Rd	1					
	SUBX.B Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
XORC	XORC #xx:8, CCR	1					

Notes: 1. n: Initial value in R4L. The source and destination operands are accessed n + 1 times each.

2. 1 in the H8/3847R Group and 0 in the H8/3847S Group, H8/38347 Group, and H8/38447 Group.

SCSR1—Serial Control Status Register 1 **H'A1** **SCI1**

Bit	7	6	5	4	3	2	1	0
	—	SOL	ORER	—	—	—	MTRF	STF
Initial value	1	0	0	1	1	1	0	0
Read/Write	—	R/W	R/(W)*	—	—	—	R	R/W

Start flag

0	Read	Transfer operation stopped
	Write	Invalid
1	Read	Transfer operation in progress
	Write	Starts transfer operation

Tail mark transmission flag

0	Idle state, or 8-bit/16-bit data transfer in progress
1	Tail mark transmission in progress

Overrun error flag

0	[Clearing condition] After reading ORER = 1, cleared by writing 0 to ORER
1	[Setting condition] When an external clock is used and the clock is input after transfer is completed

Extension data bit

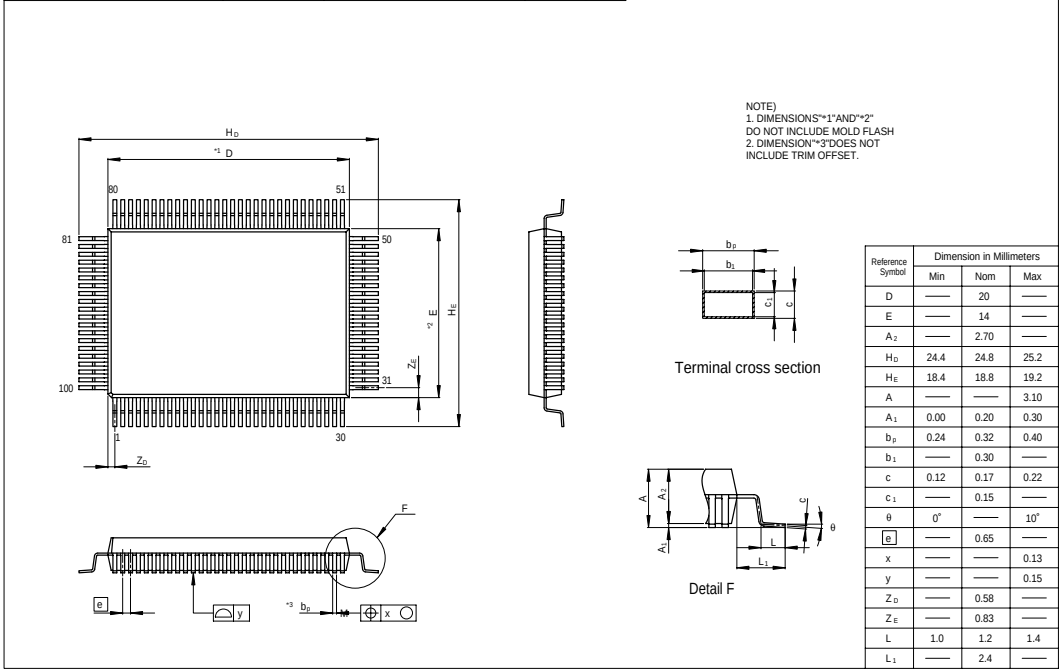
0	Read	SO_1 pin output level is low
	Write	Changes SO_1 pin output to low level
1	Read	SO_1 pin output level is high
	Write	Changes SO_1 pin output to high level

Note: * Only a write of 0 for flag clearing is possible.

Appendix F Package Dimensions

Dimensional drawings of H8/3847R Group, H8/3847S Group, H8/38347 Group, and H8/38447 Group packages FP-100A (only H8/3847R Group), FP-100B, TFP-100B and TFP-100G are shown in following figures F.1, F.2, F.3, and F.4, respectively.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JE-B	FP-100A/FP-100AV	1.7g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	20	——
E	——	14	——
A_2	——	2.70	——
H_D	24.4	24.8	25.2
H_E	18.4	18.8	19.2
A	——	——	3.10
A_1	0.00	0.20	0.30
b_p	0.24	0.32	0.40
b_1	——	0.30	——
c	0.12	0.17	0.22
c_1	——	0.15	——
θ	0°	——	10°
e	——	0.65	——
x	——	——	0.13
y	——	——	0.15
Z_D	——	0.58	——
Z_E	——	0.83	——
L	1.0	1.2	1.4
L_1	——	2.4	——

Figure F.1 FP-100A Package Dimensions