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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38347hwv

Notes: The following limitations apply when using the on-chip emulator for program development and debugging.

1. Pin P24 is reserved for use exclusively by the on-chip emulator and cannot be used for other operations.
2. Pins P25, P26, and P27 cannot be used. In order to use these pins it is necessary to install additional hardware on the user board.
3. The address area from H'E000 to H'EFFF is used by the on-chip emulator and therefore cannot be accessed by the user.
4. The address area from H'F300 to H'F6FF must not be accessed under any circumstances.
5. When the on-chip emulator is used, pin P24 functions as an I/O pin, pins P25 and P26 function as input pins, and pin P27 functions as an output pin.
6. During a break, the watchdog timer continues to operate. Therefore, an internal reset is generated if an overflow occurs during the break.

Related Material: The latest information is available at our Web Site. Please make sure that you have the most up-to-date information available. (http://www.renesas.com/)

User's Manuals on the H8/3847:

Manual Title	Document No.
H8/3847R Group, H8/3847S Group, H8/38347 Group, H8/38447 Group Hardware Manual	This manual
H8/300L Series Programming Manual	REJ09B0214-0200

User's manuals for development tools:

Manual Title	Document No.
C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual	REJ10B0161-0100
H8S, H8/300 Series Simulator/Debugger User's Manual	REJ10B0211-0200
High-Performance Embedded Workshop User's Manual	ADE-702-201
H8S, H8/300 Series High-Performance Embedded Workshop, High-Performance Debugging Interface User's Manual	ADE-702-231

2.8 Memory Map

2.8.1 Memory Map

The memory map of the H8/3842R, H8/38342, and H8/38442 is shown in figure 2.16 (1), that of the H8/3843R, H8/38343, and H8/38443 in figure 2.16 (2), that of the H8/3844R, H8/3844S, H8/38344, and H8/38444 in figure 2.16 (3), that of the H8/3845R, H8/3845S, H8/38345, and H8/38445 in figure 2.16 (4), that of the H8/3846R, H8/3846S, H8/38346, and H8/38446 in figure 2.16 (5), and that of the H8/3847R, H8/3847S, H8/38347, and H8/38447 in figure 2.16 (6).

[B: BSET instruction executed]

```
BSET    #0   ,   @RAM0
```

The BSET instruction is executed designating the PDR3 work area (RAM0).

[C: After executing BSET]

```
MOV. B  @RAM0,    R0L
MOV. B  R0L,      @PDR3
```

The work area (RAM0) value is written to PDR3.

	$P3_7$	**$P3_6$**	**$P3_5$**	**$P3_4$**	**$P3_3$**	**$P3_2$**	**$P3_1$**	**$P3_0$**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR3	0	0	1	1	1	1	1	1
PDR3	1	0	0	0	0	0	0	1
RAM0	1	0	0	0	0	0	0	1

2. Bit Manipulation in a Register Containing a Write-only Bit

Example 3: BCLR instruction executed designating port 3 control register PCR3

As in the examples above, $P3_7$ and $P3_6$ are input pins, with a low-level signal input at $P3_7$ and a high-level signal at $P3_6$. The remaining pins, $P3_5$ to $P3_0$, are output pins that output low-level signals. In this example, the BCLR instruction is used to change pin $P3_0$ to an input port. It is assumed that a high-level signal will be input to this input pin.

[A: Prior to executing BCLR]

	$P3_7$	**$P3_6$**	**$P3_5$**	**$P3_4$**	**$P3_3$**	**$P3_2$**	**$P3_1$**	**$P3_0$**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR3	0	0	1	1	1	1	1	1
PDR3	1	0	0	0	0	0	0	0

5.3 Standby Mode

5.3.1 Transition to Standby Mode

The system goes from active mode to standby mode when a SLEEP instruction is executed while the SSBY bit in SYSCR1 is set to 1, the LSON bit in SYSCR1 is cleared to 0, and bit TMA3 in TMA is cleared to 0. In standby mode the clock pulse generator stops, so the CPU and on-chip peripheral modules stop functioning, but as long as the rated voltage is supplied, the contents of CPU registers, on-chip RAM, and some on-chip peripheral module registers are retained. On-chip RAM contents will be further retained down to a minimum RAM data retention voltage. The I/O ports go to the high-impedance state.

5.3.2 Clearing Standby Mode

Standby mode is cleared by an interrupt (IRQ_1 or IRQ_0), WKP_7 to WKP_0 or by input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, the system clock pulse generator starts. After the time set in bits STS2 to STS0 in SYSCR1 has elapsed, a stable system clock signal is supplied to the entire chip, standby mode is cleared, and interrupt exception handling starts. Operation resumes in active (high-speed) mode if MSON = 0 in SYSCR2, or active (medium-speed) mode if MSON = 1. Standby mode is not cleared if the I bit of CCR is set to 1 or the particular interrupt is disabled in the interrupt enable register.

- Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the system clock pulse generator starts. After the pulse generator output has stabilized, if the $\overline{RES}$ pin is driven high, the CPU starts reset exception handling. Since system clock signals are supplied to the entire chip as soon as the system clock pulse generator starts functioning, the $\overline{RES}$ pin should be kept at the low level until the pulse generator output stabilizes.

5.3.3 Oscillator Settling Time after Standby Mode is Cleared

Bits STS2 to STS0 in SYSCR1 should be set as follows.

- When a crystal oscillator is used

  The table below gives settings for various operating frequencies. Set bits STS2 to STS0 for a waiting time at least as long as the oscillation settling time.

Pin	Pin Functions and Selection Method
$P1_3$/TMIG	The pin function depends on bit TMIG in PMR1 and bit $PCR1_3$ in PCR1.

TMIG	0		1
$PCR1_3$	0	1	*
Pin function	$P1_3$ input pin	$P1_3$ output pin	TMIG input pin

$P1_2$/TMOFH — The pin function depends on bit TMOFH in PMR1 and bit $PCR1_2$ in PCR1.

TMOFH	0		1
$PCR1_2$	0	1	*
Pin function	$P1_2$ input pin	$P1_2$ output pin	TMOFH output pin

$P1_1$/TMOFL — The pin function depends on bit TMOFL in PMR1 and bit $PCR1_1$ in PCR1.

TMOFL	0		1
$PCR1_1$	0	1	*
Pin function	$P1_1$ input pin	$P1_1$ output pin	TMOFL output pin

$P1_0$/TMOW — The pin function depends on bit TMOW in PMR1 and bit $PCR1_0$ in PCR1.

TMOW	0		1
$PCR1_0$	0	1	*
Pin function	$P1_0$ input pin	$P1_0$ output pin	TMOW output pin

*: Don't care

8.2.4 Pin States

Table 8.4 shows the port 1 pin states in each operating mode.

Table 8.4 Port 1 Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P1_7$/$\overline{IRQ_3}$/TMIF $P1_6$/$\overline{IRQ_2}$ $P1_5$/$\overline{IRQ_1}$/TMIC $P1_4$/IRQ_4/$\overline{ADTRG}$ $P1_3$/TMIG $P1_2$/TMOFH $P1_1$/TMOFL $P1_0$/TMOW	High-impedance	Retains previous state	Retains previous state	High-impedance*	Retains previous state	Functional	Functional

Note: * A high-level signal is output when the MOS pull-up is in the on state.

9.3.4 Timer C Operation States

Table 9.7 summarizes the timer C operation states.

Table 9.7 Timer C Operation States

Operation Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCC	Interval	Reset	Functions	Functions	Halted	Functions/ Halted*	Functions/ Halted*	Halted	Halted
	Auto reload	Reset	Functions	Functions	Halted	Functions/ Halted*	Functions/ Halted*	Halted	Halted
TMC		Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: * When $\phi w/4$ is selected as the TCC internal clock in active mode or sleep mode, since the system clock and internal clock are mutually asynchronous, synchronization is maintained by a synchronization circuit. This results in a maximum count cycle error of $1/\phi$ (s). When the counter is operated in subactive mode or subsleep mode, either select $\phi w/4$ as the internal clock or select an external clock. The counter will not operate on any other internal clock. If $\phi w/4$ is selected as the internal clock for the counter when $\phi w/8$ has been selected as subclock ϕ_{SUB}, the lower 2 bits of the counter operate on the same cycle, and the operation of the least significant bit is unrelated to the operation of the counter.

9.7.4 Asynchronous Event Counter Operation Modes

Asynchronous event counter operation modes are shown in table 9.21.

Table 9.21 Asynchronous Event Counter Operation Modes

Operation Mode	Reset	Active	Sleep	Watch	Subactive	Subsleep	Standby	Module Standby
ECCSR	Reset	Functions	Functions	Held*	Functions	Functions	Held*	Held
ECH	Reset	Functions	Functions	Functions*	Functions	Functions	Functions*	Halted
ECL	Reset	Functions	Functions	Functions*	Functions	Functions	Functions*	Halted

Note: * When an asynchronous external event is input, the counter increments but the counter overflow H/L flags are not affected.

9.7.5 Application Notes

1. When reading the values in ECH and ECL, the correct value will not be returned if the event counter increments during the read operation. Therefore, if the counter is being used in the 8-bit mode, clear bits CUEH and CUEL in ECCSR to 0 before reading ECH or ECL. If the counter is being used in the 16-bit mode, clear CUEL only to 0 before reading ECH or ECL.
2. In the H8/3847R Group, if the internal power supply step-down circuit is not used, the maximum clock frequency to be input to the AEVH and AEVL pins is 16 MHz when Vcc = 4.5 to 5.5 V, 10 MHz when Vcc = 2.7 to 5.5 V, and 4 MHz when Vcc = 1.8 to 5.5 V. If the internal power step-down circuit is used, the maximum clock frequency to be input is 10 MHz when Vcc = 2.7 to 5.5 V, and 4 MHz when Vcc = 1.8 to 5.5 V. In the H8/3847S Group, the maximum clock frequency to be input is 10 MHz when Vcc = 2.7 to 3.6 V, and 4 MHz when Vcc = 1.8 to 3.6 V. In the H8/38347 Group and H8/38447 Group, the maximum clock frequency to be input is 16 MHz when Vcc = 2.7 to 5.5 V. In addition, ensure that the high and low widths of the clock are at least 32 ns. The duty cycle is immaterial.

Bit 5: Transmit enable (TE)

Bit 5 selects enabling or disabling of the start of transmit operation.

Bit 5 TE	Description	
0	Transmit operation disabled[*1] (TXD pin is I/O port)	(initial value)
1	Transmit operation enabled[*2] (TXD pin is transmit data pin)	

Notes: 1. Bit TDRE in SSR is fixed at 1.
2. When transmit data is written to TDR in this state, bit TDR in SSR is cleared to 0 and serial data transmission is started. Be sure to carry out serial mode register (SMR) settings, and setting of bit SPC31 or SPC32 in SPCR, to decide the transmission format before setting bit TE to 1.

Bit 4: Receive enable (RE)

Bit 4 selects enabling or disabling of the start of receive operation.

Bit 4 RE	Description	
0	Receive operation disabled[*1] (RXD pin is I/O port)	(initial value)
1	Receive operation enabled[*2] (RXD pin is receive data pin)	

Notes: 1. Note that the RDRF, FER, PER, and OER flags in SSR are not affected when bit RE is cleared to 0, and retain their previous state.
2. In this state, serial data reception is started when a start bit is detected in asynchronous mode or serial clock input is detected in synchronous mode. Be sure to carry out serial mode register (SMR) settings to decide the reception format before setting bit RE to 1.

Table 10.9 Examples of BRR Settings for Various Bit Rates (Synchronous Mode) (1)

	OSC								
	38.4 kHz			2 MHz			4 MHz		
Bit Rate (bit/s)	n	N	Error	n	N	Error	n	N	Error
200	0	23	0	—	—	—	—	—	—
250	—	—	—	—	—	—	2	124	0
300	2	0	0	—	—	—	—	—	—
500			—	—	—	—	—	—	
1k			0	249	0	—	—	—	
2.5k			0	99	0	0	199	0	
5k			0	49	0	0	99	0	
10k			0	24	0	0	49	0	
25k			0	9	0	0	19	0	
50k			0	4	0	0	9	0	
100k			—	—	—	0	4	0	
250k			0	0	0	0	1	0	
500k						0	0	0	
1M									

9. Clock Stop Register 1 (CKSTPR1)

Bit	7	6	5	4	3	2	1	0
	S1CKSTP	S31CKSTP	S32CKSTP	ADCKSTP	TGCKSTP	TFCKSTP	TCCKSTP	TACKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CKSTPR1 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bits relating to SCI3 are described here. For details of the other bits, see the sections on the relevant modules.

Bit 6: SCI3-1 module standby mode control (S31CKSTP)

Bit 6 controls setting and clearing of module standby mode for SCI31.

S31CKSTP	Description	
0	SCI3-1 is set to module standby mode*	
1	SCI3-1 module standby mode is cleared	(initial value)

Note: * Setting to module standby mode resets all the registers in SCI31.

Bit 5: SCI3-2 module standby mode control (S32CKSTP)

Bit 5 controls setting and clearing of module standby mode for SCI32.

S32CKSTP	Description	
0	SCI3-2 is set to module standby mode*	
1	SCI3-2 module standby mode is cleared	(initial value)

Note: * Setting to module standby mode resets all the registers in SCI32.

10. Serial Port Control Register (SPCR)

Bit	7	6	5	4	3	2	1	0
	—	—	SPC32	SPC31	SCINV3	SCINV2	SCINV1	SCINV0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

SPCR is an 8-bit readable/writable register that performs RXD_{31}, RXD_{32}, TXD_{31}, and TXD_{32} pin input/output data inversion switching. SPCR is initialized to H'C0 by a reset.

11.1.4 Register Configuration

Table 11.2 shows the register configuration of the 14-bit PWM.

Table 11.2 Register Configuration

Name	Abbr.	R/W	Initial Value	Address
PWM control register	PWCR	W	H'FC	H'FFD0
PWM data register U	PWDRU	W	H'C0	H'FFD1
PWM data register L	PWDRL	W	H'00	H'FFD2
Clock stop register 2	CKSTPR2	R/W	H'FF	H'FFFB

11.2 Register Descriptions

11.2.1 PWM Control Register (PWCR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PWCR1	PWCR0
Initial value	1	1	1	1	1	1	0	0
Read/Write	—	—	—	—	—	—	W	W

PWCR is an 8-bit write-only register for input clock selection.

Upon reset, PWCR is initialized to H'FC.

Bits 7 to 2: Reserved bits

Bits 7 to 2 are reserved; they are always read as 1, and cannot be modified.

Section 12 A/D Converter

12.1 Overview

This LSI includes on-chip a resistance-ladder-based successive-approximation analog-to-digital converter, and can convert up to 12 channels of analog input.

12.1.1 Features

The A/D converter has the following features.

- 10-bit resolution
- 12 input channels
- Conversion time: approx. 12.4 µs per channel (at 5 MHz operation)
- Built-in sample-and-hold function
- Interrupt requested on completion of A/D conversion
- A/D conversion can be started by external trigger input
- Use of module standby mode enables this module to be placed in standby mode independently when not used.

12.1.3 Pin Configuration

Table 12.1 shows the A/D converter pin configuration.

Table 12.1 Pin Configuration

Name	Abbr.	I/O	Function
Analog power supply	AV_{CC}	Input	Power supply and reference voltage of analog part
Analog ground	AV_{SS}	Input	Ground and reference voltage of analog part
Analog input 0	AN_0	Input	Analog input channel 0
Analog input 1	AN_1	Input	Analog input channel 1
Analog input 2	AN_2	Input	Analog input channel 2
Analog input 3	AN_3	Input	Analog input channel 3
Analog input 4	AN_4	Input	Analog input channel 4
Analog input 5	AN_5	Input	Analog input channel 5
Analog input 6	AN_6	Input	Analog input channel 6
Analog input 7	AN_7	Input	Analog input channel 7
Analog input 8	AN_8	Input	Analog input channel 8
Analog input 9	AN_9	Input	Analog input channel 9
Analog input 10	AN_{10}	Input	Analog input channel 10
Analog input 11	AN_{11}	Input	Analog input channel 11
External trigger input	$\overline{ADTRG}$	Input	External trigger input for starting A/D conversion

12.1.4 Register Configuration

Table 12.2 shows the A/D converter register configuration.

Table 12.2 Register Configuration

Name	Abbr.	R/W	Initial Value	Address
A/D mode register	AMR	R/W	H'30	H'FFC6
A/D start register	ADSR	R/W	H'7F	H'FFC7
A/D result register H	ADRRH	R	Not fixed	H'FFC4
A/D result register L	ADRRL	R	Not fixed	H'FFC5
Clock stop register 1	CKSTPRT1	R/W	H'FF	H'FFFA

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$P1_0$ to $P1_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, PA_0 to PA_3	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P2_0$ to $P2_7$, $P3_0$ to $P3_7$	—	—	1.0		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
Input/ output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$, OSC_1, X_1, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, PA_0 to PA_3	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7, PC_0 to PC_3	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_0$ to $P1_7$, $P2_4$*6, $P3_0$ to $P3_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$	20	—	200	µA	V_{CC} = 5.0 V, V_{IN} = 0.0 V	
			—	40	—		V_{CC} = 2.7 V, V_{IN} = 0.0 V	Reference value
Input capacitance	C_{in}	All input pins except power supply pin	—	—	15.0	pF	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	

PUCR1—Port Pull-Up Control Register 1 **H'E0** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$PUCR1_7$	$PUCR1_6$	$PUCR1_5$	$PUCR1_4$	$PUCR1_3$	$PUCR1_2$	$PUCR1_1$	$PUCR1_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 1 input pull-up MOS control

0	Input pull-up MOS is off
1	Input pull-up MOS is on

Note: When the PCR1 specification is 0. (Input port specification)

PUCR3—Port Pull-Up Control Register 3 **H'E1** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$PUCR3_7$	$PUCR3_6$	$PUCR3_5$	$PUCR3_4$	$PUCR3_3$	$PUCR3_2$	$PUCR3_1$	$PUCR3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 3 input pull-up MOS control

0	Input pull-up MOS is off
1	Input pull-up MOS is on

Note: When the PCR3 specification is 0. (Input port specification)

CKSTPR2—Clock Stop Register 2 **H'FB** **System control**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	AECKSTP	WDCKSTP	PWCKSTP	LDCKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

LCD module standby mode control

0	LCD is set to module standby mode
1	LCD module standby mode is cleared

PWM module standby mode control

0	PWM is set to module standby mode
1	PWM module standby mode is cleared

WDT module standby mode control

0	WDT is set to module standby mode
1	WDT module standby mode is cleared

Asynchronous event counter module standby mode control

0	Asynchronous event counter is set to module standby mode
1	Asynchronous event counter module standby mode is cleared

C.8 Block Diagrams of Port 8

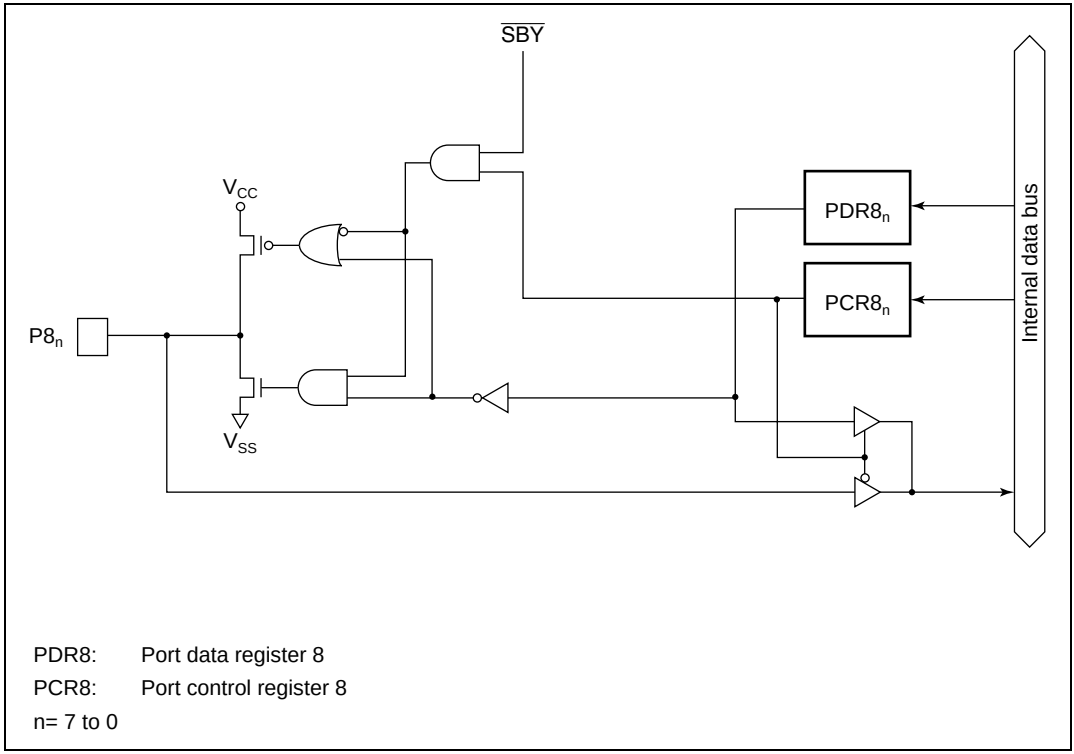

Figure C.8 Port 8 Block Diagram

C.12 Block Diagram of Port C

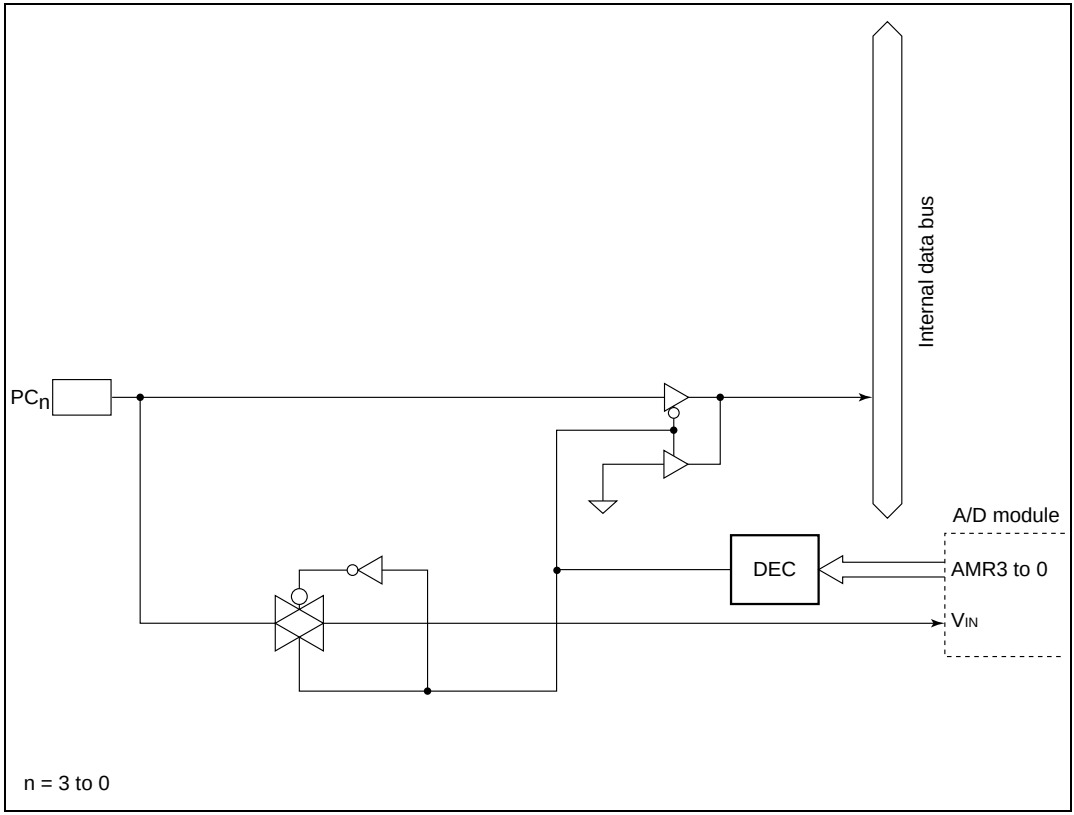

Figure C.12 Port C Block Diagram