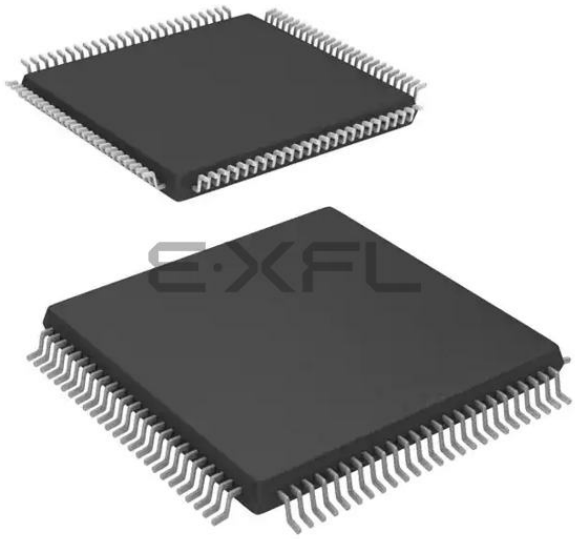


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38347wv

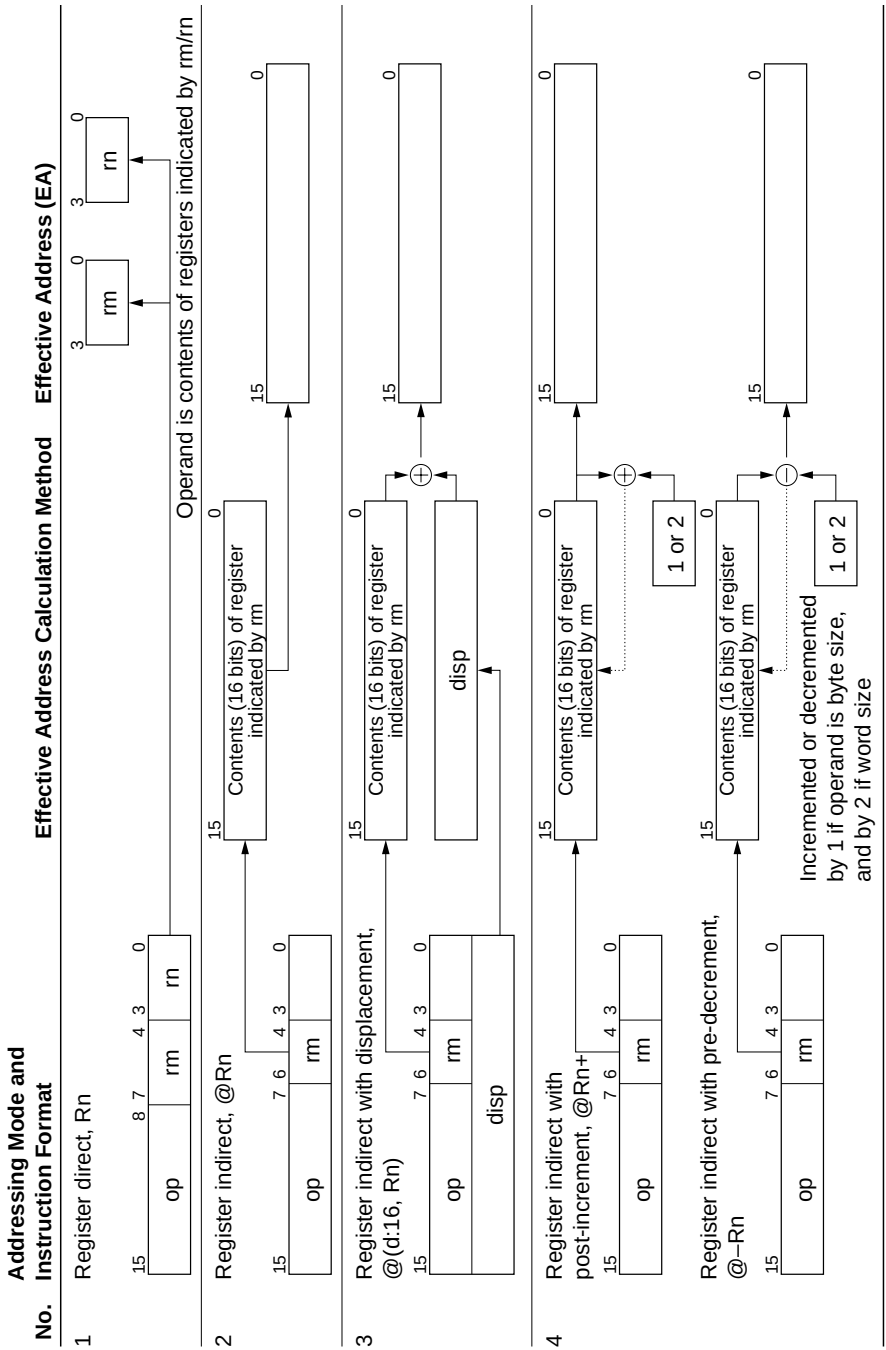
Section 6 ROM

Section 8 I/O Ports

Pad No.	Pad Name	Coordinates* X (µm)	Y (µm)
95	PB_7/AN_7	-767	1605
96	PC_0/AN_8	-879	1605
97	PC_1/AN_9	-991	1605
98	PC_2/AN_{10}	-1103	1605
99	PC_3/AN_{11}	-1290	1605
100	AV_{SS}	-1523	1605

Note: * These values show the coordinates of the centers of pads. The accuracy is ±5 µm. The home-point position is the chip's center and the center is located at half the distance between the upper and lower pads and left and right pads.

Table 2.2 Effective Address Calculation



4.4 Prescalers

The H8/3847R Group is equipped with two on-chip prescalers having different input clocks (prescaler S and prescaler W). Prescaler S is a 13-bit counter using the system clock (φ) as its input clock. Its prescaled outputs provide internal clock signals for on-chip peripheral modules. Prescaler W is a 5-bit counter using a 32.768 kHz or 38.4 kHz signal divided by 4 ($\phi_W/4$) as its input clock. Its prescaled outputs are used by timer A as a time base for timekeeping.

1. Prescaler S (PSS)

Prescaler S is a 13-bit counter using the system clock (φ) as its input clock. It is incremented once per clock period.

Prescaler S is initialized to H'0000 by a reset, and starts counting on exit from the reset state.

In standby mode, watch mode, subactive mode, and subsleep mode, the system clock pulse generator stops. Prescaler S also stops and is initialized to H'0000.

The CPU cannot read or write prescaler S.

The output from prescaler S is shared by timer A, timer C, timer F, timer G, SCI1, SCI3-1, SC3-2, the A/D converter, the LCD controller, the watchdog timer, and the 14-bit PWM. The divider ratio can be set separately for each on-chip peripheral function.

In active (medium-speed) mode the clock input to prescaler S is φosc/16, φosc/32, φosc/64, or φosc/128.

2. Prescaler W (PSW)

Prescaler W is a 5-bit counter using a 32.768 kHz/38.4 kHz signal divided by 4 ($\phi_W/4$) as its input clock.

Prescaler W is initialized to H'00 by a reset, and starts counting on exit from the reset state.

Even in standby mode, watch mode, subactive mode, or subsleep mode, prescaler W continues functioning so long as clock signals are supplied to pins X1 and X2.

Prescaler W can be reset by setting 1s in bits TMA3 and TMA2 of timer mode register A (TMA).

Output from prescaler W can be used to drive timer A, in which case timer A functions as a time base for timekeeping.

If the same kind of erroneous operation occurs after a reset as after a state transition, hold the $\overline{\text{RES}}$ pin low for a longer period.

Bit 5—Erase Setup (ESU)

This bit is to prepare for changing to erase mode. Set this bit to 1 before setting the E bit to 1 in FLMCR1 (do not set SWE, PSU, EV, PV, E, and P bits at the same time).

Bit 5 ESU	Description	
0	The erase setup state is cancelled	(initial value)
1	The flash memory changes to the erase setup state. Set this bit to 1 before setting the E bit to 1 in FLMCR1.	

Bit 4—Program Setup (PSU)

This bit is to prepare for changing to program mode. Set this bit to 1 before setting the P bit to 1 in FLMCR1 (do not set SWE, ESU, EV, PV, E, and P bits at the same time).

Bit 4 PSU	Description	
0	The program setup state is cancelled	(initial value)
1	The flash memory changes to the program setup state. Set this bit to 1 before setting the P bit to 1 in FLMCR1.	

Bit 3—Erase-Verify (EV)

This bit is to set changing to or cancelling erase-verify mode (do not set SWE, ESU, PSU, PV, E, and P bits at the same time).

Bit 3 EV	Description	
0	Erase-verify mode is cancelled	(initial value)
1	The flash memory changes to erase-verify mode	

8.12 Port B

8.12.1 Overview

Port B is an 8-bit input-only port, configured as shown in figure 8.11.

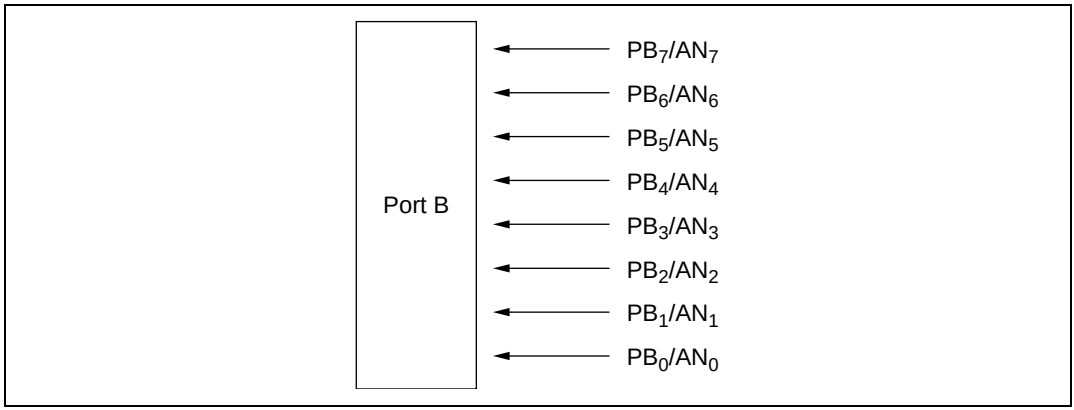


Figure 8.11 Port B Pin Configuration

8.12.2 Register Configuration and Description

Table 8.32 shows the port B register configuration.

Table 8.32 Port B Register

Name	Abbr.	R/W	Address
Port data register B	PDRB	R	H'FFDE

1. Port Data Register B (PDRB)

Bit	7	6	5	4	3	2	1	0
	PB 7	PB 6	PB 5	PB 4	PB 3	PB 2	PB 1	PB 0
Read/Write	R	R	R	R	R	R	R	R

Reading PDRB always gives the pin states. However, if a port B pin is selected as an analog input channel for the A/D converter by AMR bits CH3 to CH0, that pin reads 0 regardless of the input voltage.

9.3.4 Timer C Operation States

Table 9.7 summarizes the timer C operation states.

Table 9.7 Timer C Operation States

Operation Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCC	Interval	Reset	Functions	Functions	Halted	Functions/ Halted*	Functions/ Halted*	Halted	Halted
	Auto reload	Reset	Functions	Functions	Halted	Functions/ Halted*	Functions/ Halted*	Halted	Halted
TMC		Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: * When $\phi w/4$ is selected as the TCC internal clock in active mode or sleep mode, since the system clock and internal clock are mutually asynchronous, synchronization is maintained by a synchronization circuit. This results in a maximum count cycle error of $1/\phi$ (s). When the counter is operated in subactive mode or subsleep mode, either select $\phi w/4$ as the internal clock or select an external clock. The counter will not operate on any other internal clock. If $\phi w/4$ is selected as the internal clock for the counter when $\phi w/8$ has been selected as subclock ϕ_{SUB}, the lower 2 bits of the counter operate on the same cycle, and the operation of the least significant bit is unrelated to the operation of the counter.

Bits 7 and 6: Operating mode select 1 and 0 (SNC1, SNC0)

Bits 7 and 6 select the operating mode.

Bit 7 SNC1	Bit 6 SNC0	Description	
0	0	8-bit synchronous mode	(initial value)
0	1	16-bit synchronous mode	
1	0	Continuous clock output mode*1	
1	1	Reserved*2	

Notes: 1. Use pins SI_1 and SO_1 as ports.
2. Do not set bits SNC1 and SNC0 to 11.

Bit 5: TAIL MARK control (MRKON)

Bit 5 controls tail mark output after transfer of 8-bit or 16-bit data.

Bit 5 MRKON	Description	
0	TAIL MARK is not output (synchronous mode)	(initial value)
1	TAIL MARK is output (SSB mode)	

Bit 4: LATCH TAIL select (LTCH)

Bit 4 selects whether LATCH TAIL or HOLD TAIL is output as the tail mark when MRKON = 1 (i.e. in SSB mode).

Bit 4 LTCH	Description	
0	HOLD TAIL is output	(initial value)
1	LATCH TAIL is output	

Table 10.6 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (2)

	OSC					
	10 MHz			16 MHz		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)
110	2	88	–0.25	2	141	0.03
150	2	64	0.16	2	103	0.16
200	2	48	–0.35	2	77	0.16
250	2	38	0.16	2	62	–0.79
300	—	—	—	2	51	0.16
600	—	—	—	2	25	0.16
1200	0	129	0.16	0	207	0.16
2400	0	64	0.16	0	103	0.16
4800	—	—	—	0	51	0.16
9600	—	—	—	0	25	0.16
19200	—	—	—	0	12	0.16
31250	0	4	0	0	7	0
38400	—	—	—	—	—	—

Notes: 1. The setting should be made so that the error is not more than 1%.

2. The value set in BRR is given by the following equation:

$$N = \frac{OSC}{(64 \times 2^{2n} \times B)} - 1$$

where

B: Bit rate (bit/s)

N: Baud rate generator BRR setting ($0 \leq N \leq 255$)

OSC: Value of ϕ_{OSC} (Hz)

n: Baud rate generator input clock number (n = 0, 2, or 3)

(The relation between n and the clock is shown in table 10.7.)

Table 10.7 Relation between n and Clock

		SMR Setting	
n	Clock	CKS1	CKS0
0	ϕ	0	0
0	$\phi_W/2^{*1}/\phi_W{}^{*2}$	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

Notes: 1. $\phi_W/2$ clock is selected in active (medium- and high-speed) or sleep (medium- and high-speed) mode.

2. ϕ_W clock is selected in subactive or subsleep mode. SCI3 can be used only when the $\phi_W/2$ is selected as the CPU clock in subactive or subsleep mode.

3. The error in table 10.6 is the value obtained from the following equation, rounded to two decimal places.

$$\text{Error (\%)} = \frac{\text{B (rate obtained from n, N, OSC)} - \text{R (bit rate in left-hand column in table 10.6.)}}{\text{R (bit rate in left-hand column in table 10.6.)}} \times 100$$

Table 10.8 shows the maximum bit rate for each frequency. The values shown are for active (high-speed) mode.

Table 10.8 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

		Setting	
OSC (MHz)	**Maximum Bit Rate (bit/s)**	**n**	**N**
0.0384*	600	0	0
2	31250	0	0
2.4576	38400	0	0
4	62500	0	0
10	156250	0	0
16	250000	0	0

Note: * When SMR is set up to CKS1 = “0”, CKS0 = “1”.

Table 10.9 shows examples of BRR settings in synchronous mode. The values shown are for active (high-speed) mode.

a. Data transfer format

The general data transfer format in synchronous communication is shown in figure 10.15.

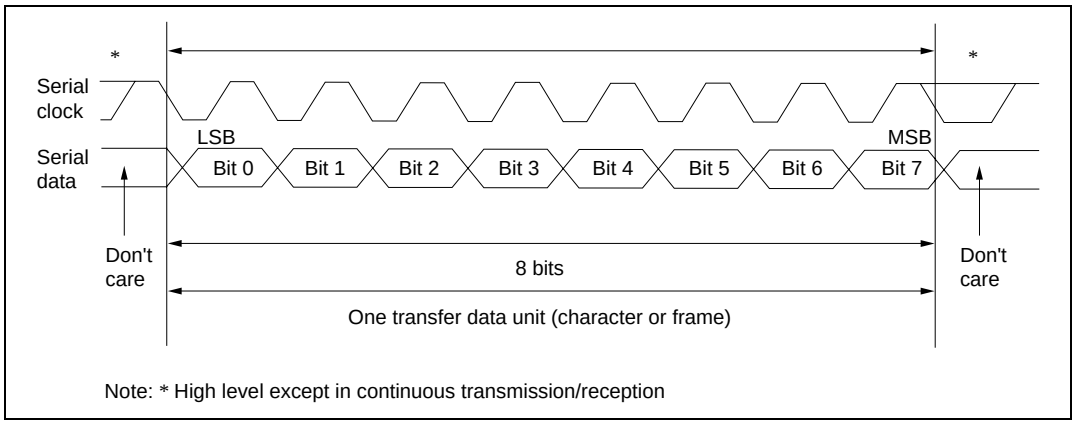


Figure 10.15 Data Format in Synchronous Communication

In synchronous communication, data on the communication line is output from one falling edge of the serial clock until the next falling edge. Data confirmation is guaranteed at the rising edge of the serial clock.

One transfer data character begins with the LSB and ends with the MSB. After output of the MSB, the communication line retains the MSB state.

When receiving in synchronous mode, SCI3 latches receive data at the rising edge of the serial clock.

The data transfer format uses a fixed 8-bit data length.

Parity and multiprocessor bits cannot be added.

b. Clock

Either an internal clock generated by the baud rate generator or an external clock input at the SCK_{3x} pin can be selected as the SCI3 serial clock. The selection is made by means of bit COM in SMR and bits CKE1 and CKE0 in SCR3. See table 10.12 for details on clock source selection.

When SCI3 operates on an internal clock, the serial clock is output at the SCK_{3x} pin. Eight pulses of the serial clock are output in transmission or reception of one character, and when SCI_3 is not transmitting or receiving, the clock is fixed at the high level.

SCI3 operates as follows when transmitting data.

SCI3 monitors bit TDRE in SSR, and when it is cleared to 0, recognizes that data has been written to TDR and transfers data from TDR to TSR. It then sets bit TDRE to 1 and starts transmitting. If bit TIE in SCR3 is set to 1 at this time, a TXI request is made.

When clock output mode is selected, SCI3 outputs 8 serial clock pulses. When an external clock is selected, data is output in synchronization with the input clock.

Serial data is transmitted from the TXD3x pin in order from the LSB (bit 0) to the MSB (bit 7). When the MSB (bit 7) is sent, checks bit TDRE. If bit TDRE is cleared to 0, SCI3 transfers data from TDR to TSR, and starts transmission of the next frame. If bit TDRE is set to 1, SCI3 sets bit TEND to 1 in SSR, and after sending the MSB (bit 7), retains the MSB state. If bit TEIE in SCR3 is set to 1 at this time, a TEI request is made.

After transmission ends, the SCK pin is fixed at the high level.

Note: Transmission is not possible if an error flag (OER, FER, or PER) that indicates the data reception status is set to 1. Check that these error flags are all cleared to 0 before a transmit operation.

Figure 10.17 shows an example of the operation when transmitting in synchronous mode.

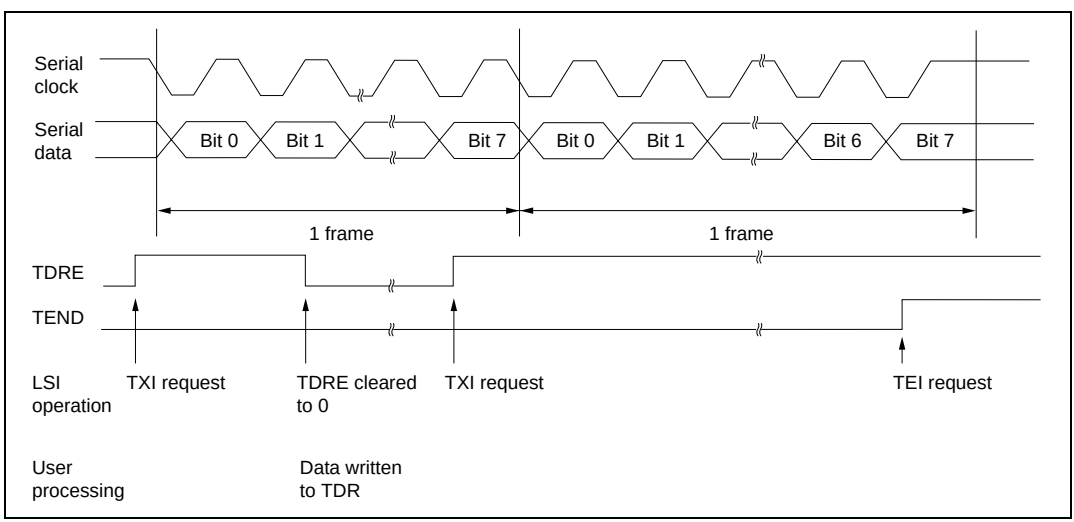


Figure 10.17 Example of Operation when Transmitting in Synchronous Mode

SCI3 operates as follows when transmitting data.

SCI3 monitors bit TDRE in SSR, and when it is cleared to 0, recognizes that data has been written to TDR and transfers data from TDR to TSR. It then sets bit TDRE to 1 and starts transmitting. If bit TIE in SCR3 is set to 1 at this time, a TXI request is made.

Serial data is transmitted from the TXD pin using the relevant data transfer format in table 10.14. When the stop bit is sent, SCI3 checks bit TDRE. If bit TDRE is cleared to 0, SCI3 transfers data from TDR to TSR, and when the stop bit has been sent, starts transmission of the next frame. If bit TDRE is set to 1 bit TEND in SSR bit is set to 1, the mark state, in which 1s are transmitted, is established after the stop bit has been sent. If bit TEIE in SCR3 is set to 1 at this time, a TEI request is made.

Figure 10.23 shows an example of the operation when transmitting using the multiprocessor format.

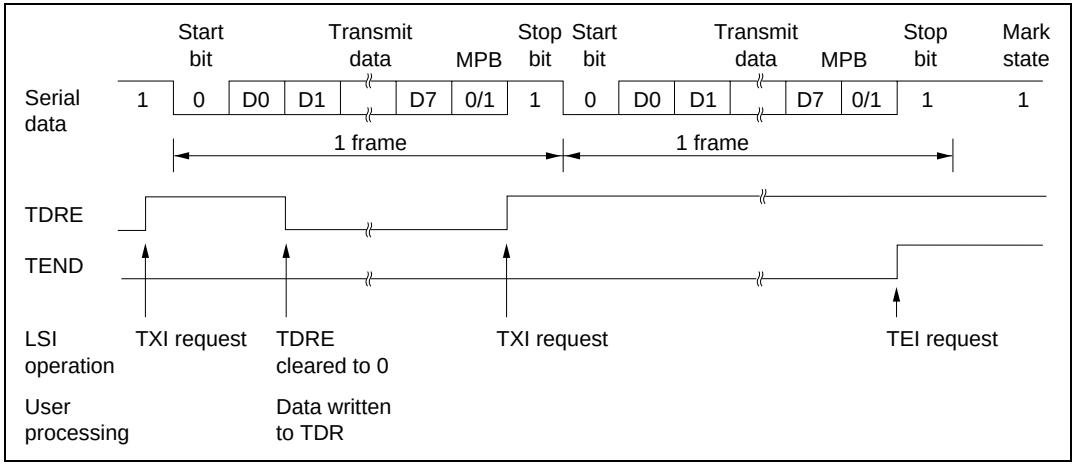


Figure 10.23 Example of Operation when Transmitting Using Multiprocessor Format (8-bit data, multiprocessor bit, 1 stop bit)

- Multiprocessor receiving

Figure 10.24 shows an example of a flowchart for multiprocessor data reception. This procedure should be followed for multiprocessor data reception after initializing SCI3.

12.3 Operation

12.3.1 A/D Conversion Operation

The A/D converter operates by successive approximations, and yields its conversion result as 10-bit data.

A/D conversion begins when software sets the A/D start flag (bit ADSF) to 1. Bit ADSF keeps a value of 1 during A/D conversion, and is cleared to 0 automatically when conversion is complete.

The completion of conversion also sets bit IRRAD in interrupt request register 2 (IRR2) to 1. An A/D conversion end interrupt is requested if bit IENAD in interrupt enable register 2 (IENR2) is set to 1.

If the conversion time or input channel needs to be changed in the A/D mode register (AMR) during A/D conversion, bit ADSF should first be cleared to 0, stopping the conversion operation, in order to avoid malfunction.

12.3.2 Start of A/D Conversion by External Trigger Input

The A/D converter can be made to start A/D conversion by input of an external trigger signal. External trigger input is enabled at pin $\overline{\text{ADTRG}}$ when bit IRQ4 in PMR1 is set to 1 and bit TRGE in AMR is set to 1. Then when the input signal edge designated in bit IEG4 of interrupt edge select register (IEGR) is detected at pin $\overline{\text{ADTRG}}$, bit ADSF in ADSR will be set to 1, starting A/D conversion.

Figure 12.2 shows the timing.

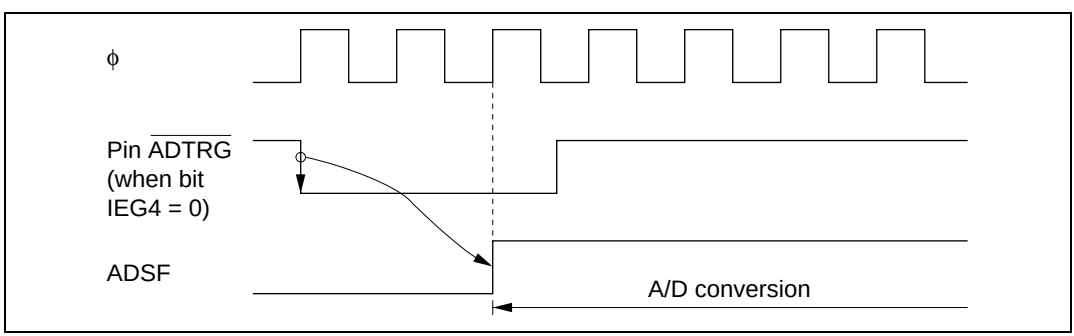
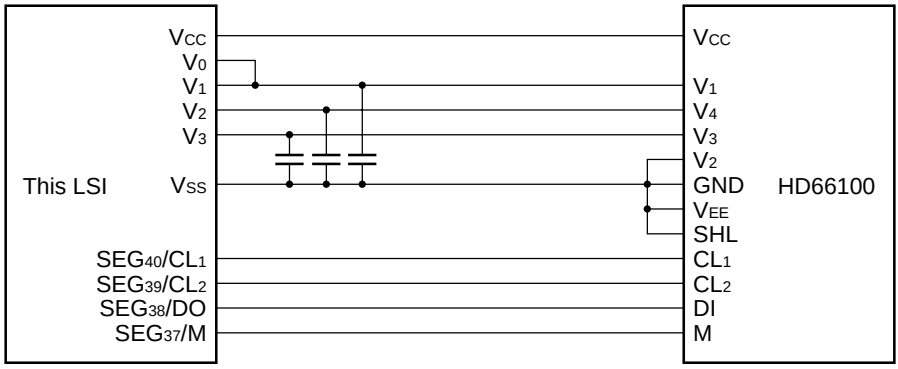
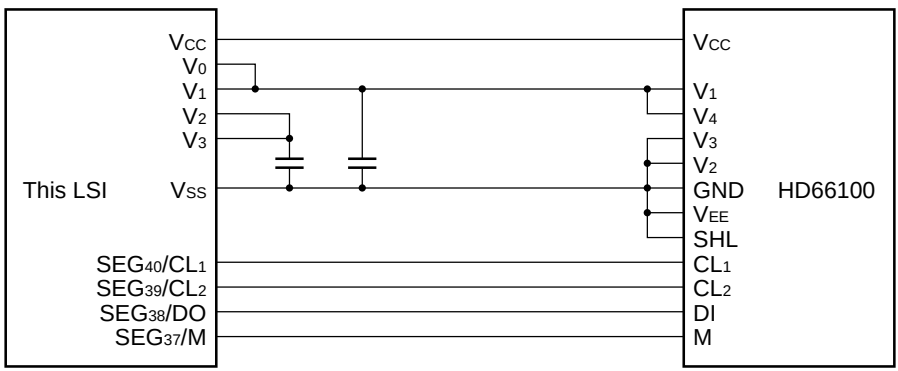


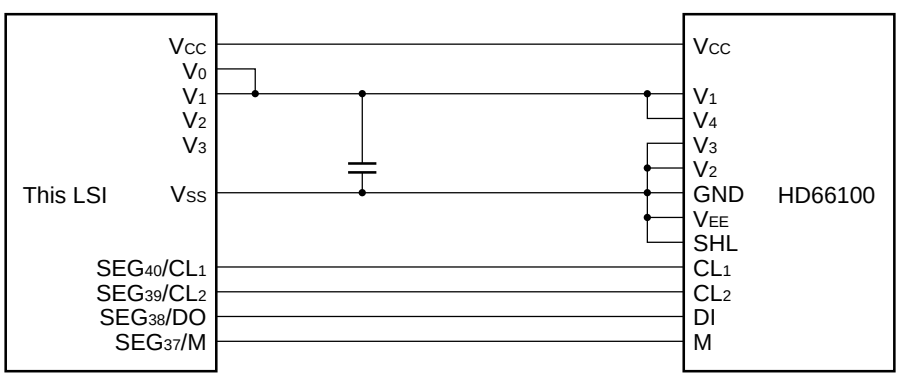
Figure 12.2 External Trigger Input Timing



(a) 1/3 bias, 1/4 duty or 1/3 duty



(b) 1/2 duty



(c) Static

Figure 13.18 Connection to HD66100

15.8.3 AC Characteristics

Table 15.27 lists the control signal timing and table 15.28 and 15.29 list the serial interface timing.

Table 15.27 Control Signal Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2.0	—	16.0	MHz		*3
			2.0	—	16.0		V_{CC} = 4.5 to 5.5 V	*4
			2.0	—	10.0		V_{CC} = 2.7 to 5.5 V	
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC_1, OSC_2	62.5	—	500 (1000)	ns		Figure 15.1 *2 *3
			62.5	—	500 (1000)		V_{CC} = 4.5 to 5.5 V	Figure 15.1 *2 *4
			100	—	500 (1000)		V_{CC} = 2.7 to 5.5 V	
System clock (ϕ) cycle time	t_{cyc}		2	—	128	t_{OSC}		
			—	—	128	µs		
Subclock oscillation frequency	f_W	X_1, X_2, EXCL	—	32.768 or 38.4	—	kHz		
Watch clock (ϕ_W) cycle time	t_W	X_1, X_2, EXCL	—	30.5 or 26.0	—	µs		Figure 15.1
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}		2	—	4	t_W		*1
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time	t_{rc}	OSC_1, OSC_2	—	20	45	µs	Ceramic resonator (V_{CC} = 3.0 to 5.5 V)	Figure 15.11
			—	80	—		Ceramic resonator other than above	
			—	0.8	2	ms	Crystal resonator	
			—	—	50		Other than above	
	t_{rc}	X_1, X_2	—	—	2.0	s		

15.8.6 Flash Memory Characteristics

Table 15.32 Flash Memory Characteristics

Condition: AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 2.7 V to 5.5 V (range of operating voltage when reading), V_{CC} = 3.0 V to 5.5 V (range of operating voltage when programming/erasing), T_a = –20°C to +75°C (range of operating temperature when programming/erasing: product with regular specifications, product with wide-range temperature specifications)

Item		Symbol	Values			Unit	Test Conditions
			Min	Typ	Max		
Programming time*1*2*4		t_P	—	7	200	ms/128 bytes	
Erase time*1*3*5		t_E	—	100	1200	ms/block	
Reprogramming count		N_{WEC}	1000*8	10000*9	—	times	
Data retain period		t_{DRP}	10*10	—	—	year	
Programming	Wait time after SWE-bit setting*1	x	1	—	—	µs	
	Wait time after PSU-bit setting*1	y	50	—	—	µs	
	Wait time after P-bit setting*1*4	z1	28	30	32	µs	1 ≤ n ≤ 6
		z2	198	200	202	µs	7 ≤ n ≤ 1000
		z3	8	10	12	µs	Additional programming
	Wait time after P-bit clear*1	α	5	—	—	µs	
	Wait time after PSU-bit clear*1	β	5	—	—	µs	
	Wait time after PV-bit setting*1	γ	4	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after PV-bit clear*1	η	2	—	—	µs	
	Wait time after SWE-bit clear*1	θ	100	—	—	µs	
	Maximum programming count*1*4*5	N	—	—	1000	times	

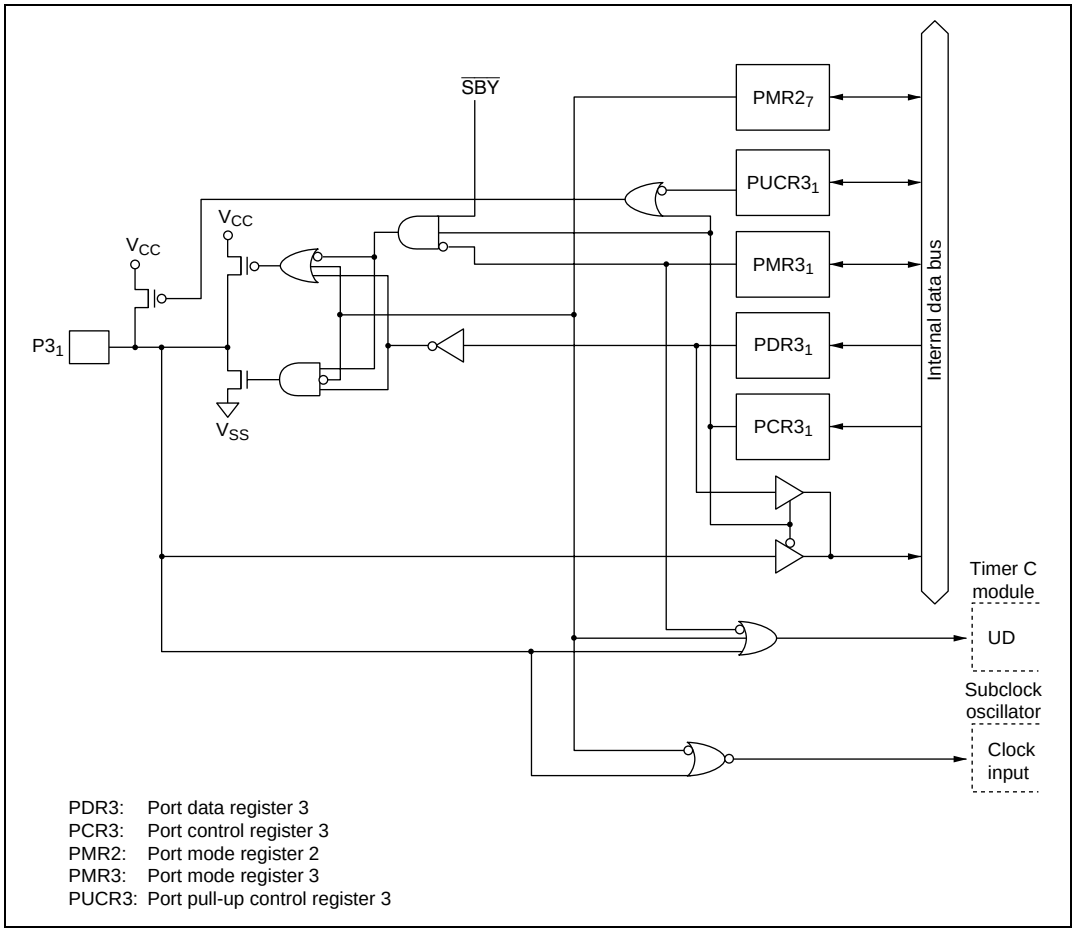


Figure C.3 (f-2) Port 3 Block Diagram (Pin P3$_1$, H8/38347 Group and H8/38447 Group)

Product Type				Product Code	Mark Code	Package (Package Code)
H8/38347 Group	H8/38342	Mask ROM versions	Regular products	HD64338342H	38342H	100-pin QFP (FP-100B)
				HD64338342W	38342W	100-pin TQFP (TFP-100G)
				HD64338342X	38342X	100-pin TQFP (TFP-100B)
				HCD64338342	—	Die
			Wide-range specification products	HD64338342HW	38342H	100-pin QFP (FP-100B)
				HD64338342WW	38342W	100-pin TQFP (TFP-100G)
				HD64338342XW	38342X	100-pin TQFP (TFP-100B)
	H8/38343	Mask ROM versions	Regular products	HD64338343H	38343H	100-pin QFP (FP-100B)
				HD64338343W	38343W	100-pin TQFP (TFP-100G)
				HD64338343X	38343X	100-pin TQFP (TFP-100B)
				HCD64338343	—	Die
			Wide-range specification products	HD64338343HW	38343H	100-pin QFP (FP-100B)
				HD64338343WW	38343W	100-pin TQFP (TFP-100G)
				HD64338343XW	38343X	100-pin TQFP (TFP-100B)
	H8/38344	Mask ROM versions	Regular products	HD64338344H	38344H	100-pin QFP (FP-100B)
				HD64338344W	38344W	100-pin TQFP (TFP-100G)
				HD64338344X	38344X	100-pin TQFP (TFP-100B)
				HCD64338344	—	Die
			Wide-range specification products	HD64338344HW	38344H	100-pin QFP (FP-100B)
				HD64338344WW	38344W	100-pin TQFP (TFP-100G)
				HD64338344XW	38344X	100-pin TQFP (TFP-100B)
		F-ZTAT versions	Regular products	HD64F38344H	F38344H	100-pin QFP (FP-100B)
				HD64F38344W	F38344W	100-pin TQFP (TFP-100G)
				HD64F38344X	F38344X	100-pin TQFP (TFP-100B)
			Wide-range specification products	HD64F38344HW	F38344H	100-pin QFP (FP-100B)
				HD64F38344WW	F38344W	100-pin TQFP (TFP-100G)
				HD64F38344XW	F38344X	100-pin TQFP (TFP-100B)