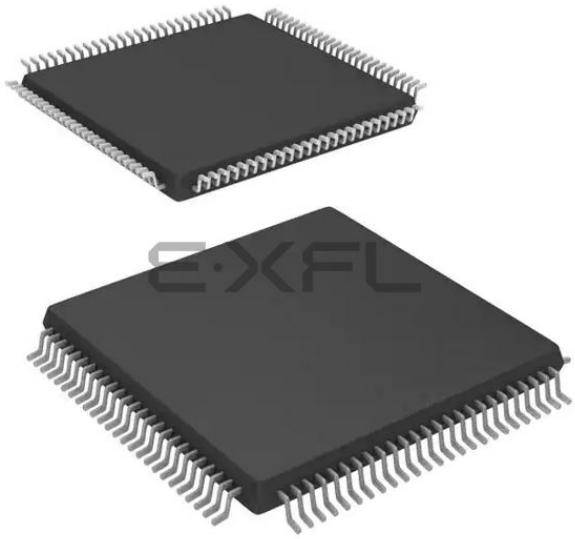

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38347xv

Tables

Item	Description				
Product lineup	**Mask ROM Version**	**ZTAT Version**	**F-ZTAT Version**	**Package**	**ROM/RAM Size (Byte)**
	HD6433847R HD6433847S HD64338347 HD64338447	HD6473847R	HD64F38347 HD64F38447	FP-100A (H8/3847R only) FP-100B TFP-100B TFP-100G Die	60 K/2 K
	HD6433846R HD6433846S HD64338346 HD64338446	—	—	FP-100A (H8/3846R only) FP-100B TFP-100B TFP-100G Die	48 K/2 K
	HD6433845R HD6433845S HD64338345 HD64338445	—	—	FP-100A (H8/3845R only) FP-100B TFP-100B TFP-100G Die	40 K/2 K
	HD6433844R HD6433844S HD64338344 HD64338444	—	HD64F38344 HD64F38444	FP-100A (H8/3844R only) FP-100B TFP-100B TFP-100G Die (Mask ROM version only)	32 K/2 K
	HD6433843R HD64338343 HD64338443	—	—	FP-100A (H8/3843R only) FP-100B TFP-100B TFP-100G Die	24 K/1 K
	HD6433842R HD64338342 HD64338442	—	—	FP-100A (H8/3842R only) FP-100B TFP-100B TFP-100G Die	16 K/1 K
	See appendix E for a list of product codes.				

Note: * See section 4, Clock Pulse Generators, for the definition of ϕ and ϕw.

		Coordinates*	
Pad No.	**Pad Name**	**X (µm)**	**Y (µm)**
95	PB_7/AN_7	-766	1767
96	PC_0/AN_8	-872	1767
97	PC_1/AN_9	-978	1767
98	PC_2/AN_{10}	-1084	1767
99	PC_3/AN_{11}	-1190	1767
100	AV_{SS}	-1629	1767

Note: * These values show the coordinates of the centers of pads. The accuracy is ±5 µm. The home-point position is the chip's center and the center is located at half the distance between the upper and lower pads and left and right pads. Pad numbers 11, 33, and 100 are power supply (V_{SS}) pads and must be connected. They should not be left open. Pad number 14 (TEST) must be connected to the Vss position. The device will not operate properly if the pads are not connected as indicated.

Type	Symbol	Pin No. FP-100B TFP-100B TFP-100G	Pin No. FP-100A	I/O	Name and Functions
I/O ports	$P8_7$ to $P8_0$	74 to 67	77 to 70	I/O	**Port 8:** This is an 8-bit I/O port. Input or output can be designated for each bit by means of port control register 8 (PCR8).
	$P9_7$ to $P9_0$	82 to 75	85 to 78	I/O	**Port 9:** This is an 8-bit I/O port. Input or output can be designated for each bit by means of port control register 9 (PCR9).
Serial communi-cation interface (SCI)	SI_1	17	20	Input	**SCI1 receive data input:** This is the SCI1 data input pin.
	SO_1	18	21	Output	**SCI1 transmit data output:** This is the SCI1 data output pin.
	SCK_1	16	19	I/O	**SCI1 clock I/O:** This is the SCI1 clock I/O pin.
	RXD_{31}	28	31	Input	**SCI3-1 receive data input:** This is the SCI31 data input pin.
	TXD_{31}	29	32	Output	**SCI3-1 transmit data output:** This is the SCI31 data output pin.
	SCK_{31}	27	30	I/O	**SCI3-1 clock I/O:** This is the SCI31 clock I/O pin.
	RXD_{32}	84	87	Input	**SCI3-2 receive data input:** This is the SCI32 data input pin.
	TXD_{32}	85	88	Output	**SCI3-2 transmit data output:** This is the SCI32 data output pin.
	SCK_{32}	83	86	I/O	**SCI3-2 clock I/O:** This is the SCI32 clock I/O pin.
A/D converter	AN_{11} to An_0	99 to 88	2,1 100 to 91	Input	**Analog input channels 11 to 0:** These are analog data input channels to the A/D converter
	$\overline{ADTRG}$	5	8	Input	**A/D converter trigger input:** This is the external trigger input pin to the A/D converter

Table 3.2 Interrupt Sources and Their Priorities

Interrupt Source	Interrupt	Vector Number	Vector Address	Priority
$\overline{RES}$	Reset	0	H'0000 to H'0001	High
Watchdog timer				▲
$\overline{IRQ_0}$	IRQ_0	4	H'0008 to H'0009	
$\overline{IRQ_1}$	IRQ_1	5	H'000A to H'000B	
$\overline{IRQ_2}$	IRQ_2	6	H'000C to H'000D	
$\overline{IRQ_3}$	IRQ_3	7	H'000E to H'000F	
$\overline{IRQ_4}$	IRQ_4	8	H'0010 to H'0011	
WKP_0	WKP_0	9	H'0012 to H'0013	
WKP_1	WKP_1			
WKP_2	WKP_2			
WKP_3	WKP_3			
WKP_4	WKP_4			
WKP_5	WKP_5			
WKP_6	WKP_6			
WKP_7	WKP_7			
SCI1	SCI1 transfer complete	10	H'0014 to H'0015	
Timer A	Timer A overflow	11	H'0016 to H'0017	
Asynchronous counter	Asynchronous counter overflow	12	H'0018 to H'0019	
Timer C	Timer C overflow or underflow	13	H'001A to H'001B	
Timer FL	Timer FL compare match Timer FL overflow	14	H'001C to H'001D	
Timer FH	Timer FH compare match Timer FH overflow	15	H'001E to H'001F	
Timer G	Timer G input capture Timer G overflow	16	H'0020 to H'0021	
SCI3-1	SCI3-1 transmit end SCI3-1 transmit data empty SCI3-1 receive data full SCI3-1 overrrun error SCI3-1 framing error SCI3-1 parity error	17	H'0022 to H'0023	
SCI3-2	SCI3-2 transmit end SCI3-2 transmit data empty SCI3-2 receive data full SCI3-2 overrun error SCI3-2 framing error SCI3-2 parity error	18	H'0024 to H'0025	
A/D	A/D conversion end	19	H'0026 to H'0027	
(SLEEP instruction executed)	Direct transfer	20	H'0028 to H'0029	▼ Low

Note: Vector addresses H'0002 to H'0007 are reserved and cannot be used.

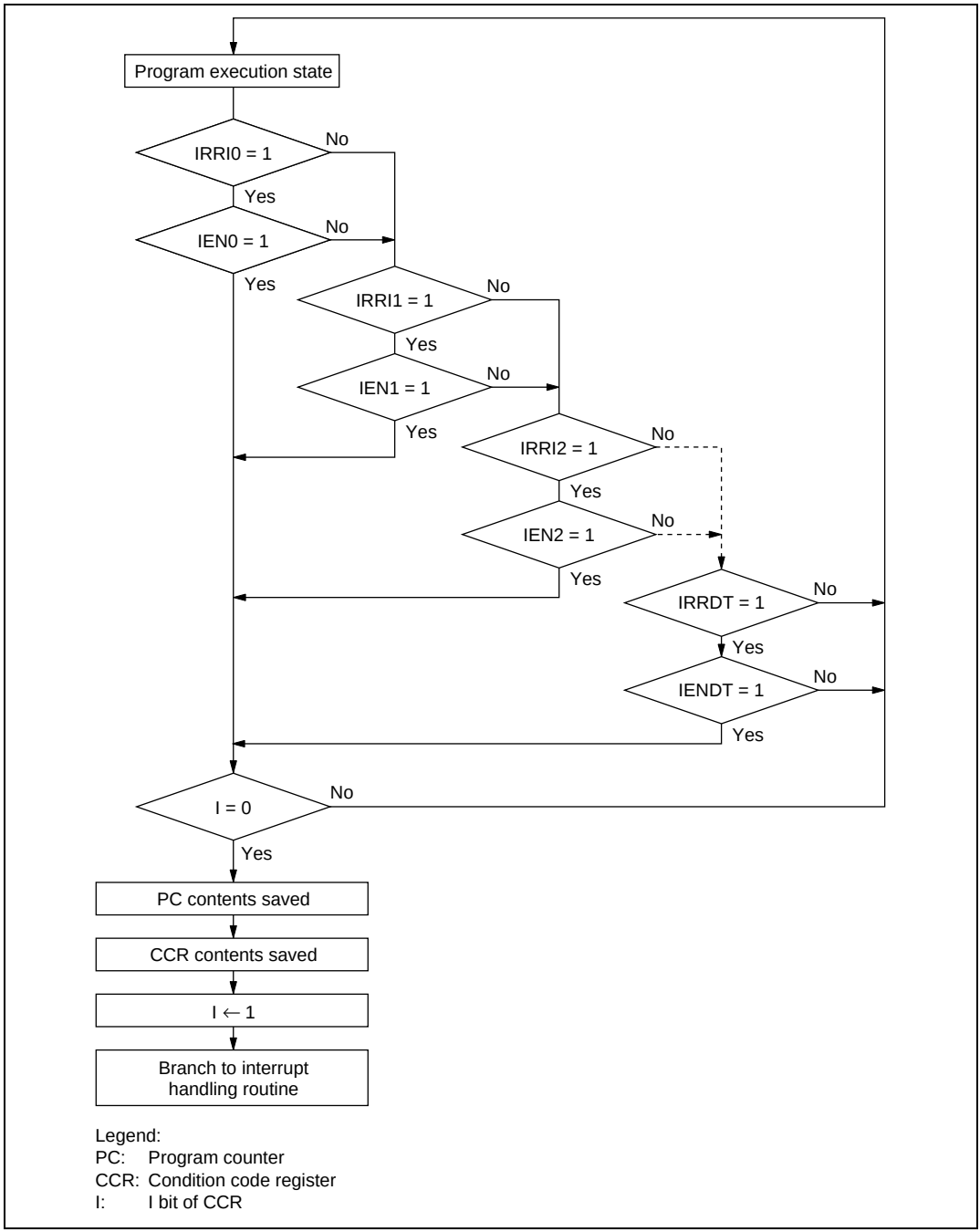

Figure 3.3 Flow Up to Interrupt Acceptance

6.5 Flash Memory Overview

6.5.1 Features

The features of the 60 Kbytes or 32 Kbytes of flash memory built into the F-ZTAT versions are summarized below.

- Programming/erase methods
  - The flash memory is programmed 128 bytes at a time. Erase is performed in single-block units. The 60-Kbyte flash memory is configured as follows: 1 Kbyte × 4 blocks, 28 Kbytes × 1 block, 16 Kbytes × 1 block, 8 Kbytes × 1 block and 4 Kbytes × 1 block. The 32-Kbyte flash memory is configured as follows: 1 Kbyte × 4 blocks, 28 Kbytes × 1 block. To erase the entire flash memory, each block must be erased in turn.
- Reprogramming capability
  - The flash memory can be reprogrammed up to 1,000 times.
- On-board programming
  - On-board programming/erasing can be done in boot mode, in which the boot program built into the chip is started to erase or program of the entire flash memory. In normal user program mode, individual blocks can be erased or programmed.
- Programmer mode
  - Flash memory can be programmed/erased in programmer mode using a PROM programmer, as well as in on-board programming mode.
- Automatic bit rate adjustment
  - For data transfer in boot mode, this LSI's bit rate can be automatically adjusted to match the transfer bit rate of the host.
- Programming/erasing protection
  - Sets software protection against flash memory programming/erasing.
- Power-down mode
  - The power supply circuit is partly halted in the subactive mode and can be read in the power-down mode.

Table 6.18 AC Characteristics in Auto-Program Mode

Conditions: V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V, T_a = 25°C ±5°C

Item	Symbol	Min	Max	Unit	Notes
Command write cycle	t_{nxtc}	20	—	µs	Figure 6.17
$\overline{CE}$ hold time	t_{ceh}	0	—	ns	
$\overline{CE}$ setup time	t_{ces}	0	—	ns	
Data hold time	t_{dh}	50	—	ns	
Data setup time	t_{ds}	50	—	ns	
Write pulse width	t_{wep}	70	—	ns	
Status polling start time	t_{wsts}	1	—	ms	
Status polling access time	t_{spa}	—	150	ns	
Address setup time	t_{as}	0	—	ns	
Address hold time	t_{ah}	60	—	ns	
Memory write time	t_{write}	1	3000	ms	
$\overline{WE}$ rise time	t_r	—	30	ns	
$\overline{WE}$ fall time	t_f	—	30	ns	

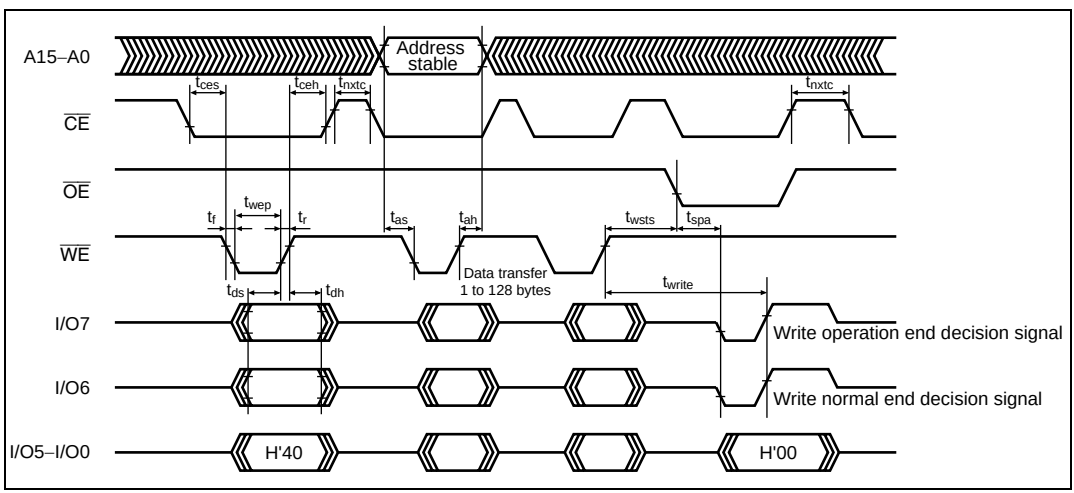

Figure 6.17 Auto-Program Mode Timing Waveforms

Bit 1: $P1_1$/TMOFL pin function switch (TMOFL)

This bit selects whether pin $P1_1$/TMOFL is used as $P1_1$ or as TMOFL.

Bit 1 TMOFL	Description	
0	Functions as $P1_1$ I/O pin	(initial value)
1	Functions as TMOFL output pin	

Bit 0: $P1_0$/TMOW pin function switch (TMOW)

This bit selects whether pin $P1_0$/TMOW is used as P10 or as TMOW.

Bit 0 TMOW	Description	
0	Functions as $P1_0$ I/O pin	(initial value)
1	Functions as TMOW output pin	

8.3.4 Pin States

Table 8.7 shows the port 2 pin states in each operating mode.

Table 8.7 Port 2 Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P2_7$ to $P2_5$	High-impedance	Retains previous state	Retains previous state	High-impedance	Retains previous state	Functional	Functional
$P2_4$*1	Pull-up MOS on						
$P2_4$*2 $P2_3$	High-impedance						
$P2_2/SO_1$ $P2_1/SI_1$ $P2_0/SCK_1$	High-impedance						

Notes: 1. Applies to the F-ZTAT version of the H8/38347 Group and H8/38447 Group.
2. Applies to H8/3847R Group and H8/3847S Group. Also applies to the mask ROM version of the H8/38347 Group and H8/38447 Group.

Bits 7 to 5: Clock output select (TMA7 to TMA5)

Bits 7 to 5 choose which of eight clock signals is output at the TMOW pin. The system clock divided by 32, 16, 8, or 4 can be output in active mode and sleep mode. A 32.768 kHz or 38.4 kHz signal divided by 32, 16, 8, or 4 can be output in active mode, sleep mode, and subactive mode. ϕ_w is output in all modes except the reset state.

CWOSR	TMA				
CWOS	Bit 7 TMA7	Bit 6 TMA6	Bit 5 TMA5	Clock Output	
0	0	0	0	ϕ/32	(initial value)
			1	ϕ/16	
		1	0	ϕ/8	
			1	ϕ/4	
	1	0	0	ϕ_W/32	
			1	ϕ_W/16	
		1	0	ϕ_W/8	
			1	ϕ_W/4	
1	*	*	*	ϕ_W	

*: Don't care

Bit 4: Reserved bit

Bit 4 is reserved; it is always read as 1, and cannot be modified.

2. Block Diagram

Figure 9.3 shows a block diagram of timer F.

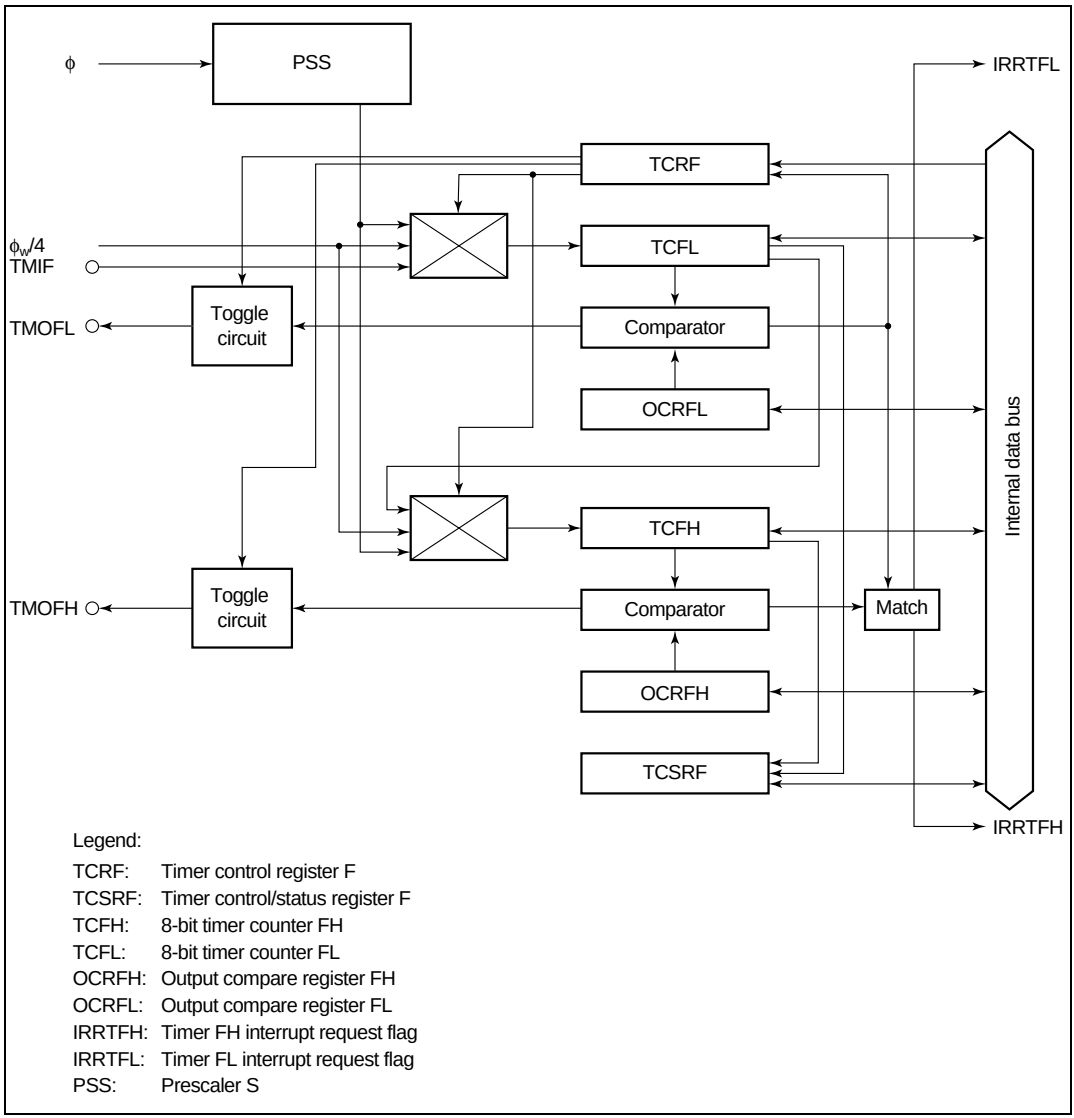

Figure 9.3 Block Diagram of Timer F

10.3 SCI3

10.3.1 Overview

In addition to SCI1, this LSI has two serial communication interfaces, SCI3-1 and SCI3-2, with identical functions. In this manual, the generic term SCI3 is used to refer to both of these SCIs.

Serial communication interface 3 (SCI3) can carry out serial data communication in either asynchronous or synchronous mode. It is also provided with a multiprocessor communication function that enables serial data to be transferred among processors.

1. Features

Features of SCI3 are listed below.

- Choice of asynchronous or synchronous mode for serial data communication
  - — Asynchronous mode

    Serial data communication is performed asynchronously, with synchronization provided character by character. In this mode, serial data can be exchanged with standard asynchronous communication LSIs such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). A multiprocessor communication function is also provided, enabling serial data communication among processors.

    There is a choice of 16 data transfer formats.

Data length	7, 8, 5 bits
Stop bit length	1 or 2 bits
Parity	Even, odd, or none
Multiprocessor bit	“1” or “0”
Receive error detection	Parity, overrun, and framing errors
Break detection	Break detected by reading the RXD_{3X} pin level directly when a framing error occurs

After setting bits CKE1 and CKE0, set the operating mode in the serial mode register (SMR).

For details on clock source selection, see table 10.12 in 10.3.3,1, Overview.

Bit 1	Bit 0	Description		
CKE1	**CKE0**	**Communication Mode**	**Clock Source**	**SCK_{3X} Pin Function**
0	0	Asynchronous	Internal clock	I/O port*1
		Synchronous	Internal clock	Serial clock output*1
0	1	Asynchronous	Internal clock	Clock output*2
		Synchronous	Reserved	
1	0	Asynchronous	External clock	Clock input*3
		Synchronous	External clock	Serial clock input
1	1	Asynchronous	Reserved	
		Synchronous	Reserved	

Notes: 1. Initial value
2. A clock with the same frequency as the bit rate is output.
3. Input a clock with a frequency 16 times the bit rate.

7. Serial Status Register (SSR)

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only a write of 0 for flag clearing is possible.

SSR is an 8-bit register containing status flags that indicate the operational status of SCI3, and multiprocessor bits.

SSR can be read or written by the CPU at any time, but only a write of 1 is possible to bits TDRE, RDRF, OER, PER, and FER. In order to clear these bits by writing 0, 1 must first be read.

Bits TEND and MPBR are read-only bits, and cannot be modified.

SSR is initialized to H'84 upon reset, and in standby, module standby, or watch mode.

Table 10.14 Data Transfer Formats (Asynchronous Mode)

SMR				Serial Data Transfer Format and Frame Length											
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S	8-bit data								STOP		
0	0	0	1	S	8-bit data								STOP	STOP	
0	0	1	0	S	8-bit data								MPB	STOP	
0	0	1	1	S	8-bit data								MPB	STOP	STOP
0	1	0	0	S	8-bit data								P	STOP	
0	1	0	1	S	8-bit data								P	STOP	STOP
0	1	1	0	S	5-bit data					STOP					
0	1	1	1	S	5-bit data					STOP	STOP				
1	0	0	0	S	7-bit data							STOP			
1	0	0	1	S	7-bit data							STOP	STOP		
1	0	1	0	S	7-bit data							MPB	STOP		
1	0	1	1	S	7-bit data							MPB	STOP	STOP	
1	1	0	0	S	7-bit data							P	STOP		
1	1	0	1	S	7-bit data							P	STOP	STOP	
1	1	1	0	S	5-bit data					P	STOP				
1	1	1	1	S	5-bit data					P	STOP	STOP			

Legend:
S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit

Bit 4: Expansion Signal Selection (SGX)

Bit 4 (SGX) selects whether the SEG_{40}/CL_1, SEG_{39}/CL_2, SEG_{38}/DO, and SEG_{37}/M pins are used as segment pins (SEG_{40} to SEG_{37}) or as segment external expansion signal pins (CL_1, CL_2, DO, and M). In the H8/38347 Group and H8/38447 Group this bit should be left at its initial value and not written to. Changing the value of this bit may prevent the SEG/COM signal from operating normally.

Bit 4 SGX	Description	
0	SEG_{40} to SEG_{37} pins*	(initial value)
1	CL_1, CL_2, DO, and M pins	

Note: * Functions as ports when SGS3 to SGS0 are set at “0000”.

Bits 3 to 0: Segment driver select 3 to 0 (SGS3 to SGS0)

Bits 3 to 0 select the segment drivers to be used. The SGX = 0 setting is selected on the H8/38347 and H8/38447.

					Function of Pins SEG_{40} to SEG_1					
Bit 4 SGX	Bit 3 SGS3	Bit 2 SGS2	Bit 1 SGS1	Bit 0 SGS0	SEG_{40} to SEG_{33}	SEG_{32} to SEG_{25}	SEG_{24} to SEG_{17}	SEG_{16} to SEG_9	SEG_8 to SEG_1	Notes
0	0	0	0	0	Port	Port	Port	Port	Port	(initial value)
0	0	0	0	1	SEG	Port	Port	Port	Port	
0	0	0	1	*	SEG	SEG	Port	Port	Port	
0	0	1	0	*	SEG	SEG	SEG	Port	Port	
0	0	1	1	*	SEG	SEG	SEG	SEG	Port	
0	1	*	*	*	SEG	SEG	SEG	SEG	SEG	
1	0	0	0	0	Port(*1)	Port	Port	Port	Port	
1	0	0	0	1	Do not use					
1	0	0	1	*						
1	0	1	*	*						
1	1	*	*	*						

*: Don’t care

Note: 1. SEG_{40} to SEG_{37} are external expansion pins.

Table 15.16 Segment External Expansion AC Characteristics

V_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, Ta = –40°C to +85°C (including subactive mode) unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Conditions	Reference Figure
Clock high width	t_{CWH}	CL_1, CL_2	800.0	—	—	ns	*	Figure 15.8
Clock low width	t_{CWL}	CL_2	800.0	—	—	ns	*	Figure 15.8
Clock setup time	t_{CSU}	CL_1, CL_2	500.0	—	—	ns	*	Figure 15.8
Data setup time	t_{SU}	DO	300.0	—	—	ns	*	Figure 15.8
Data retaining time	t_{DH}	DO	300.0	—	—	ns	*	Figure 15.8
M delay time	t_{DM}	M	–1000.0	—	1000.0	ns	*	Figure 15.8
Clock rise/fall time	t_{CT}	CL_1, CL_2	—	—	170.0	ns		Figure 15.8

Note: * When the frame frequency is set at 488 Hz to 30.5 Hz.

TMG—Timer Mode Register G H'BC Timer G

Bit	7	6	5	4	3	2	1	0
	OVFH	OVFL	OVIE	IIEGS	CCLR1	CCLR0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	W	W	W	W	W	W

Clock select

0	0	Internal clock: counting on ϕ/64
0	1	Internal clock: counting on ϕ/32
1	0	Internal clock: counting on ϕ/2
1	1	Internal clock: counting on ϕw/4

Counter clear

0	0	TCG clearing is disabled
0	1	TCG cleared by falling edge of input capture input signal
1	0	TCG cleared by rising edge of input capture input signal
1	1	TCG cleared by both edges of input capture input signal

Input capture interrupt edge select

0	Interrupt generated on rising edge of input capture input signal
1	Interrupt generated on falling edge of input capture input signal

Timer overflow interrupt enable

0	TCG overflow interrupt request is disabled
1	TCG overflow interrupt request is enabled

Timer overflow flag L

0	[Clearing condition] After reading OVFL = 1, cleared by writing 0 to OVFL
1	[Setting condition] Set when TCG overflows from H'FF to H'00

Timer overflow flag H

0	[Clearing condition] After reading OVFH = 1, cleared by writing 0 to OVFH
1	[Setting condition] Set when TCG overflows from H'FF to H'00

Note: * Bits 7 and 6 can only be written with 0, for flag clearing.

PDR5—Port Data Register 5 **H'D8** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 5 pins

PDR6—Port Data Register 6 **H'D9** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 6 pins

PDR7—Port Data Register 7 **H'DA** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 7 pins

PDR8—Port Data Register 8 **H'DB** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$P8_7$	$P8_6$	$P8_5$	$P8_4$	$P8_3$	$P8_2$	$P8_1$	$P8_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 8 pins

Product Type				Product Code	Mark Code	Package (Package Code)
H8/38347 Group	H8/38342	Mask ROM versions	Regular products	HD64338342H	38342H	100-pin QFP (FP-100B)
				HD64338342W	38342W	100-pin TQFP (TFP-100G)
				HD64338342X	38342X	100-pin TQFP (TFP-100B)
				HCD64338342	—	Die
			Wide-range specification products	HD64338342HW	38342H	100-pin QFP (FP-100B)
				HD64338342WW	38342W	100-pin TQFP (TFP-100G)
				HD64338342XW	38342X	100-pin TQFP (TFP-100B)
	H8/38343	Mask ROM versions	Regular products	HD64338343H	38343H	100-pin QFP (FP-100B)
				HD64338343W	38343W	100-pin TQFP (TFP-100G)
				HD64338343X	38343X	100-pin TQFP (TFP-100B)
				HCD64338343	—	Die
			Wide-range specification products	HD64338343HW	38343H	100-pin QFP (FP-100B)
				HD64338343WW	38343W	100-pin TQFP (TFP-100G)
				HD64338343XW	38343X	100-pin TQFP (TFP-100B)
	H8/38344	Mask ROM versions	Regular products	HD64338344H	38344H	100-pin QFP (FP-100B)
				HD64338344W	38344W	100-pin TQFP (TFP-100G)
				HD64338344X	38344X	100-pin TQFP (TFP-100B)
				HCD64338344	—	Die
			Wide-range specification products	HD64338344HW	38344H	100-pin QFP (FP-100B)
				HD64338344WW	38344W	100-pin TQFP (TFP-100G)
				HD64338344XW	38344X	100-pin TQFP (TFP-100B)
		F-ZTAT versions	Regular products	HD64F38344H	F38344H	100-pin QFP (FP-100B)
				HD64F38344W	F38344W	100-pin TQFP (TFP-100G)
				HD64F38344X	F38344X	100-pin TQFP (TFP-100B)
			Wide-range specification products	HD64F38344HW	F38344H	100-pin QFP (FP-100B)
				HD64F38344WW	F38344W	100-pin TQFP (TFP-100G)
				HD64F38344XW	F38344X	100-pin TQFP (TFP-100B)