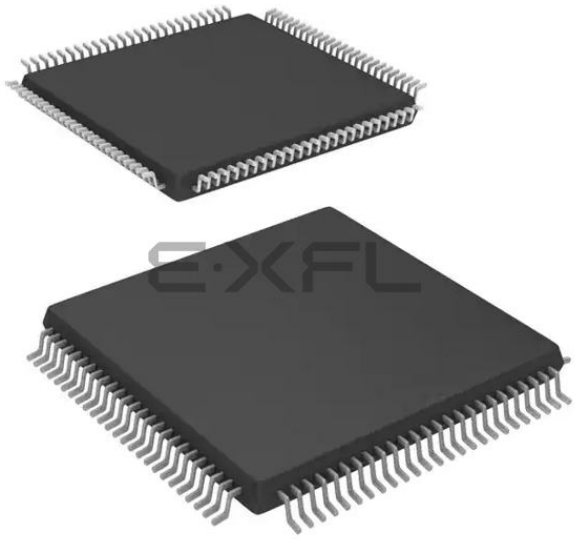

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	71
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38347xwv

Section 11 14-Bit PWM

Section 12 A/D Converter

Section 13 LCD Controller/Driver

[B: BCLR instruction executed]

```
BCLR    #0   ,   @RAM0
```

The BCLR instruction is executed designating the PCR3 work area (RAM0).

[C: After executing BCLR]

```
MOV. B  @RAM0,    R0L
MOV. B  R0L,      @PCR3
```

The work area (RAM0) value is written to PCR3.

	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR3	0	0	1	1	1	1	1	0
PDR3	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	0

Table 2.12 lists the pairs of registers that share identical addresses. Table 2.13 lists the registers that contain write-only bits.

Table 2.12 Registers with Shared Addresses

Register Name	Abbr.	Address
Timer counter and timer load register C	TCC/TLC	H'FFB5
Port data register 1*	PDR1	H'FFD4
Port data register 2*	PDR2	H'FFD5
Port data register 3*	PDR3	H'FFD6
Port data register 4*	PDR4	H'FFD7
Port data register 5*	PDR5	H'FFD8
Port data register 6*	PDR6	H'FFD9
Port data register 7*	PDR7	H'FFDA
Port data register 8*	PDR8	H'FFDB
Port data register 9*	PDR9	H'FFDC
Port data register A*	PDRA	H'FFDD

Note: * Port data registers have the same addresses as input pins.

2. Pin Connection when Not Using Subclock

When the subclock is not used, connect pin X_1 to GND and leave pin X_2 open, as shown in figure 4.8.

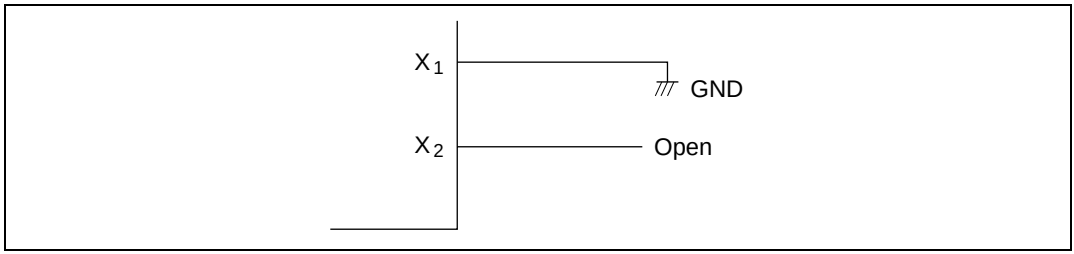


Figure 4.8 Pin Connection when not Using Subclock

3. External Clock Input

- H8/3847R Group and H8/3847S Group

Connect the external clock to the X_1 pin and leave the X_2 pin open, as shown in figure 4.9 (a).

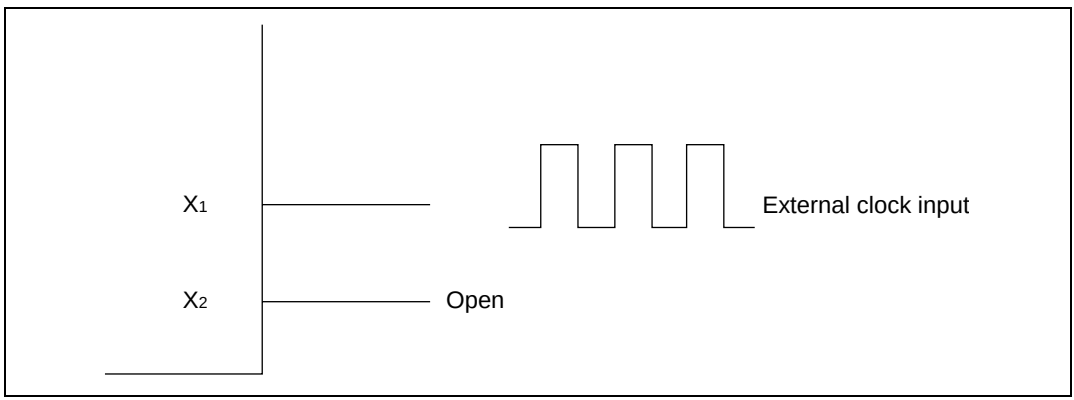


Figure 4.9 (a) Pin Connection when Inputting External Clock (H8/38347R Group and H8/3847S Group)

Frequency	Subclock (ϕw)
Duty	45% to 55%

Bit 3: Direct transfer on flag (DTON)

This bit designates whether or not to make direct transitions among active (high-speed), active (medium-speed) and subactive mode when a SLEEP instruction is executed. The mode to which the transition is made after the SLEEP instruction is executed depends on a combination of this and other control bits.

Bit 3 DTON	Description
0	• When a SLEEP instruction is executed in active mode, a transition is made to standby mode, watch mode, or sleep mode (initial value)
	• When a SLEEP instruction is executed in subactive mode, a transition is made to watch mode or subsleep mode
1	• When a SLEEP instruction is executed in active (high-speed) mode, a direct transition is made to active (medium-speed) mode if SSBY = 0, MSON = 1, and LSON = 0, or to subactive mode if SSBY = 1, TMA3 = 1, and LSON = 1 • When a SLEEP instruction is executed in active (medium-speed) mode, a direct transition is made to active (high-speed) mode if SSBY = 0, MSON = 0, and LSON = 0, or to subactive mode if SSBY = 1, TMA3 = 1, and LSON = 1 • When a SLEEP instruction is executed in subactive mode, a direct transition is made to active (high-speed) mode if SSBY = 1, TMA3 = 1, LSON = 0, and MSON = 0, or to active (medium-speed) mode if SSBY = 1, TMA3 = 1, LSON = 0, and MSON = 1

Bit 2: Medium speed on flag (MSON)

After standby, watch, or sleep mode is cleared, this bit selects active (high-speed) or active (medium-speed) mode.

Bit 2 MSON	Description
0	Operation in active (high-speed) mode (initial value)
1	Operation in active (medium-speed) mode

5.9.3 Usage Note

If, due to the timing with which a peripheral module issues interrupt requests, the module in question is set to module standby mode before an interrupt is processed, the module will stop with the interrupt request still pending. In this situation, interrupt processing will be repeated indefinitely unless interrupts are prohibited.

It is therefore necessary to ensure that no interrupts are generated when a module is set to module standby mode. The surest way to do this is to specify the module standby mode setting only when interrupts are prohibited (interrupts prohibited using the interrupt enable register or interrupts masked using bit CCR-I).

6.4 Reliability of Programmed Data

A highly effective way to improve data retention characteristics is to bake the programmed chips at 150°C, then screen them for data errors. This procedure quickly eliminates chips with PROM memory cells prone to early failure.

Figure 6.6 shows the recommended screening procedure.

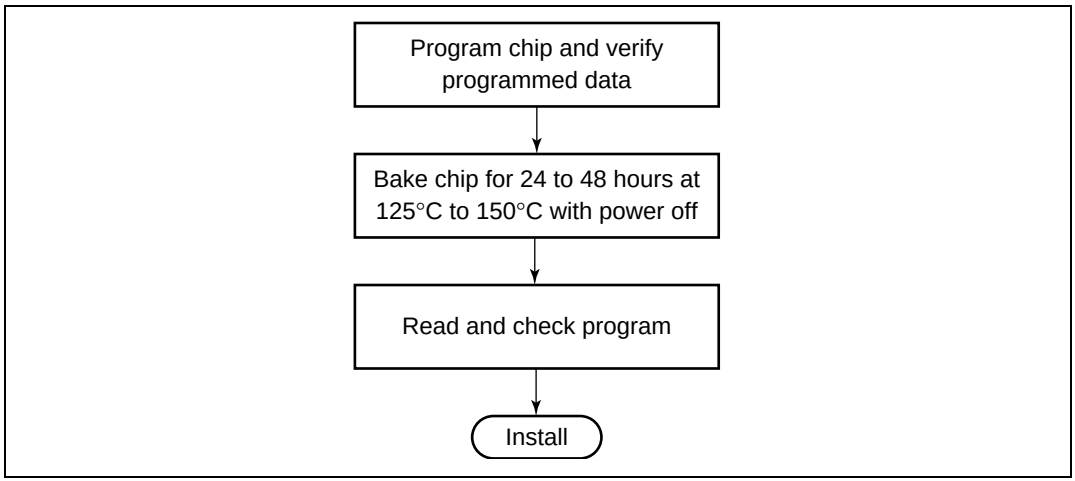


Figure 6.6 Recommended Screening Procedure

If a series of programming errors occurs while the same PROM programmer is in use, stop programming and check the PROM programmer and socket adapter for defects. Please inform Renesas Technology of any abnormal conditions noted during or after programming or in screening of program data after high-temperature baking.

Table 6.20 AC Characteristics in Status Read Mode

Conditions: V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V, T_a = 25°C ±5°C

Item	Symbol	Min	Max	Unit	Notes
Read time after command write	t_{nxtc}	20	—	µs	Figure 6.19
$\overline{CE}$ hold time	t_{ceh}	0	—	ns	
$\overline{CE}$ setup time	t_{ces}	0	—	ns	
Data hold time	t_{dh}	50	—	ns	
Data setup time	t_{ds}	50	—	ns	
Write pulse width	t_{wep}	70	—	ns	
$\overline{OE}$ output delay time	t_{oe}	—	150	ns	
Disable delay time	t_{df}	—	100	ns	
$\overline{CE}$ output delay time	t_{ce}	—	150	ns	
$\overline{WE}$ rise time	t_r	—	30	ns	
$\overline{WE}$ fall time	t_f	—	30	ns	

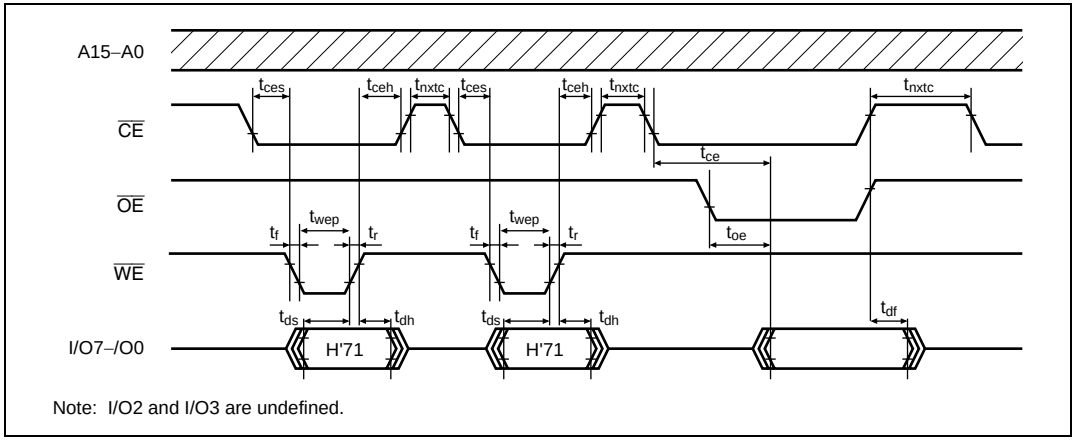


Figure 6.19 Status Read Mode Timing Waveforms

6.10.8 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup period. After the programmer mode setup time, a transition is made to memory read mode.

Table 6.23 Stipulated Transition Times to Command Wait State

Item	Symbol	Min	Max	Unit	Notes
Oscillation stabilization time(crystal oscillator)	T_{osc1}	10	—	ms	Figure 6.20
Oscillation stabilization time(ceramic oscillator)	T_{osc1}	5	—	ms	
Programmer mode setup time	T_{bmv}	10	—	ms	
Vcc hold time	T_{dwn}	0	—	ms	

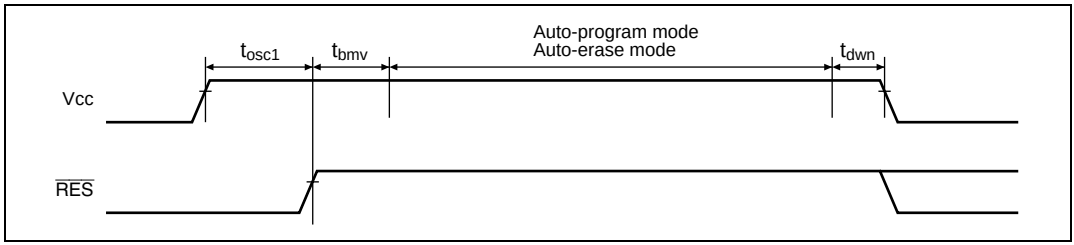


Figure 6.20 Oscillation Stabilization Time, Boot Program Transfer Time, and Power-Down Sequence

6.10.9 Notes on Memory Programming

1. When performing programming using programmer mode on a chip that has been programmed/erased in an on-board programming mode, auto-erasing is recommended before carrying out auto-programming.
2. The flash memory is initially in the erased state when the device is shipped by Renesas Technology. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.

8.9 Port 8

8.9.1 Overview

Port 8 is an 8-bit I/O port configured as shown in figure 8.8.

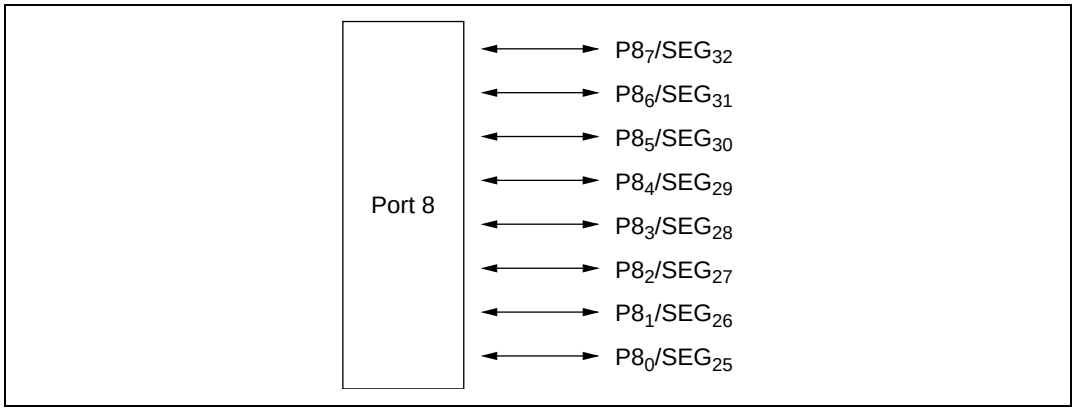


Figure 8.8 Port 8 Pin Configuration

8.9.2 Register Configuration and Description

Table 8.23 shows the port 8 register configuration.

Table 8.23 Port 8 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 8	PDR8	R/W	H'00	H'FFDB
Port control register 8	PCR8	W	H'00	H'FFEB

Bit 3: Multiprocessor interrupt enable (MPIE)

Bit 3 selects enabling or disabling of the multiprocessor interrupt request. The MPIE bit setting is only valid when asynchronous mode is selected and reception is carried out with bit MP in SMR set to 1. The MPIE bit setting is invalid when bit COM is set to 1 or bit MP is cleared to 0.

Bit 3 MPIE	Description	
0	Multiprocessor interrupt request disabled (normal receive operation) Clearing condition: When data is received in which the multiprocessor bit is set to 1	(initial value)
1	Multiprocessor interrupt request enabled*	

Note: * Receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and OER status flags in SSR is not performed. RXI, ERI, and setting of the RDRF, FER, and OER flags in SSR, are disabled until data with the multiprocessor bit set to 1 is received. When a receive character with the multiprocessor bit set to 1 is received, bit MPBR in SSR is set to 1, bit MPIE is automatically cleared to 0, and RXI and ERI requests (when bits TIE and RIE in serial control register 3 (SCR3) are set to 1) and setting of the RDRF, FER, and OER flags are enabled.

Bit 2: Transmit end interrupt enable (TEIE)

Bit 2 selects enabling or disabling of the transmit end interrupt request (TEI) if there is no valid transmit data in TDR when MSB data is to be sent.

Bit 2 TEIE	Description	
0	Transmit end interrupt request (TEI) disabled	(initial value)
1	Transmit end interrupt request (TEI) enabled*	

Note: * TEI can be released by clearing bit TDRE to 0 and clearing bit TEND to 0 in SSR, or by clearing bit TEIE to 0.

Bits 1 and 0: Clock enable 1 and 0 (CKE1, CKE0)

Bits 1 and 0 select the clock source and enabling or disabling of clock output from the SCK_{3X} pin. The combination of CKE1 and CKE0 determines whether the SCK_{3X} pin functions as an I/O port, a clock output pin, or a clock input pin.

The CKE0 bit setting is only valid in case of internal clock operation (CKE1 = 0) in asynchronous mode. In synchronous mode, or when external clock operation is used (CKE1 = 1), bit CKE0 should be cleared to 0.

Table 10.14 Data Transfer Formats (Asynchronous Mode)

SMR				Serial Data Transfer Format and Frame Length											
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S	8-bit data								STOP		
0	0	0	1	S	8-bit data								STOP	STOP	
0	0	1	0	S	8-bit data								MPB	STOP	
0	0	1	1	S	8-bit data								MPB	STOP	STOP
0	1	0	0	S	8-bit data								P	STOP	
0	1	0	1	S	8-bit data								P	STOP	STOP
0	1	1	0	S	5-bit data					STOP					
0	1	1	1	S	5-bit data					STOP	STOP				
1	0	0	0	S	7-bit data							STOP			
1	0	0	1	S	7-bit data							STOP	STOP		
1	0	1	0	S	7-bit data							MPB	STOP		
1	0	1	1	S	7-bit data							MPB	STOP	STOP	
1	1	0	0	S	7-bit data							P	STOP		
1	1	0	1	S	7-bit data							P	STOP	STOP	
1	1	1	0	S	5-bit data					P	STOP				
1	1	1	1	S	5-bit data					P	STOP	STOP			

Legend:
S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input/ output leak- age current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$	—	—	20.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	*2
			—	—	1.0			*1
		OSC_1, X_1, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, PA_0 to PA_3	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7, PC_0 to PC_3	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_0$ to $P1_7$, $P3_0$ to $P3_7$,	50.0	—	300.0	µA	V_{CC} = 5 V, V_{IN} = 0 V	
		$P5_0$ to $P5_7$, $P6_0$ to $P6_7$	—	35.0	—		V_{CC} = 2.7 V, V_{IN} = 0 V	Refer- ence value
Input capaci- tance	C_{IN}	All input pins except power supply, $\overline{RES}$, $P4_3$, PB_0 to PB_7	—	—	15.0	pF	f = 1 MHz, V_{IN} =0 V, Ta = 25°C	
		$\overline{RES}$	—	—	80.0			*2
			—	—	15.0			*1
		$P4_3$	—	—	50.0			*2
			—	—	15.0			*1
		PB_0 to PB_7	—	—	15.0			
Active mode current dissi- pation	I_{OPE1}	V_{CC}	—	4.5	6.5	mA	Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	*3 *5 *6
	I_{OPE2}	V_{CC}	—	1.3	2.0	mA	Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz, ϕ_{OSC}/128	*3 *5 *6
Sleep mode current dissi- pation	I_{SLEEP}	V_{CC}	—	2.5	4.0	mA	V_{CC} = 5 V, f_{OSC} = 10 MHz	*3 *5 *6

LCR—LCD Control Register H'C1 LCD controller/driver

Bit	7	6	5	4	3	2	1	0
	—	PSW	ACT	DISP	CKS3	CKS2	CKS1	CKS0
Initial value	1	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Frame frequency select

Bit 3	Bit 2	Bit 1	Bit 1	Operating Clock
CKS3	CKS2	CKS1	CKS0	
0	*	0	0	ϕw
0	*	0	1	ϕw/2
0	*	1	*	ϕw/4
1	0	0	0	ϕ/2
1	0	0	1	ϕ/4
1	0	1	0	ϕ/8
1	0	1	1	ϕ/16
1	1	0	0	ϕ/32
1	1	0	1	ϕ/64
1	1	1	0	ϕ/128
1	1	1	1	ϕ/256

* Don't care

Display data control

0	Blank data is displayed
1	LCD RAM data is displayed

Display function activate

0	LCD controller/driver operation halted
1	LCD controller/driver operates

LCD drive power supply on/off control

0	LCD drive power supply off
1	LCD drive power supply on

AMR—A/D Mode Register **H'C6** **A/D converter**

Bit	7	6	5	4	3	2	1	0
	CKS	TRGE	—	—	CH3	CH2	CH1	CH0
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

Channel select

Bit 3	Bit 2	Bit 1	Bit 0	
CH3	CH2	CH1	CH0	Analog Input Channel
0	0	*	*	No channel selected
0	1	0	0	AN_0
0	1	0	1	AN_1
0	1	1	0	AN_2
0	1	1	1	AN_3
1	0	0	0	AN_4
1	0	0	1	AN_5
1	0	1	0	AN_6
1	0	1	1	AN_7
1	1	0	0	AN_8
1	1	0	1	AN_9
1	1	1	0	AN_{10}
1	1	1	1	AN_{11}

* Don't care

External trigger select

0	Disables start of A/D conversion by external trigger
1	Enables start of A/D conversion by rising or falling edge of external trigger at pin $\overline{\text{ADTRG}}$

Clock select

Bit 7		Conversion Time	
CKS	Conversion Period	ϕ = 1 MHz	ϕ = 5 MHz
0	62/ϕ	62 µs	12.4 µs
1	31/ϕ	31 µs	—

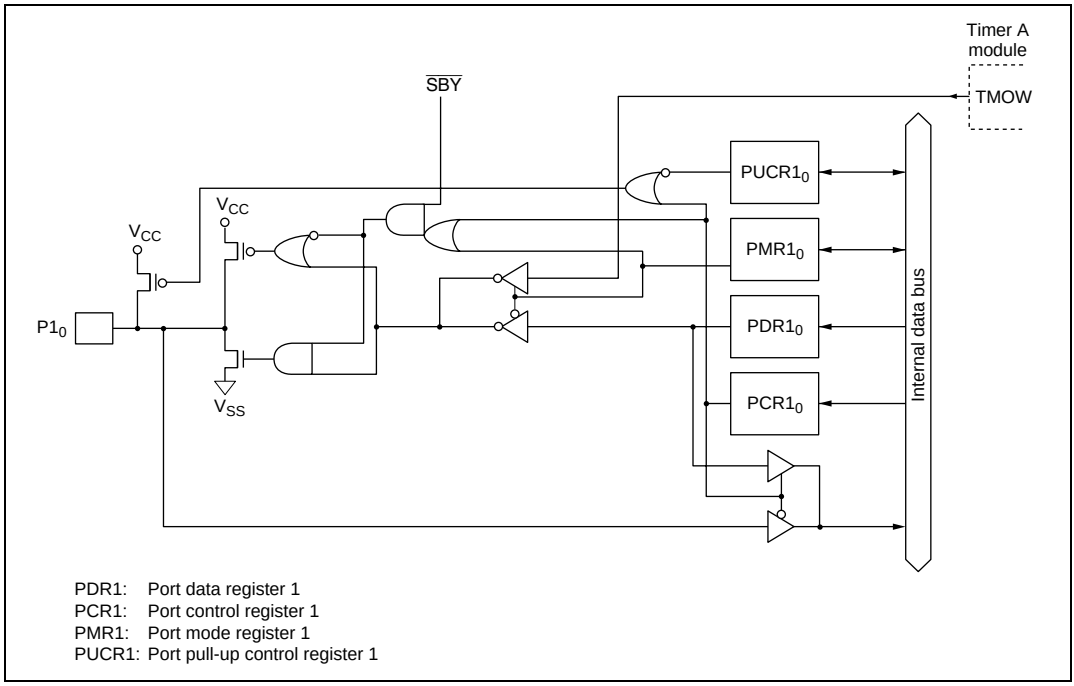


Figure C.1 (d) Port 1 Block Diagram (Pin $P1_0$)

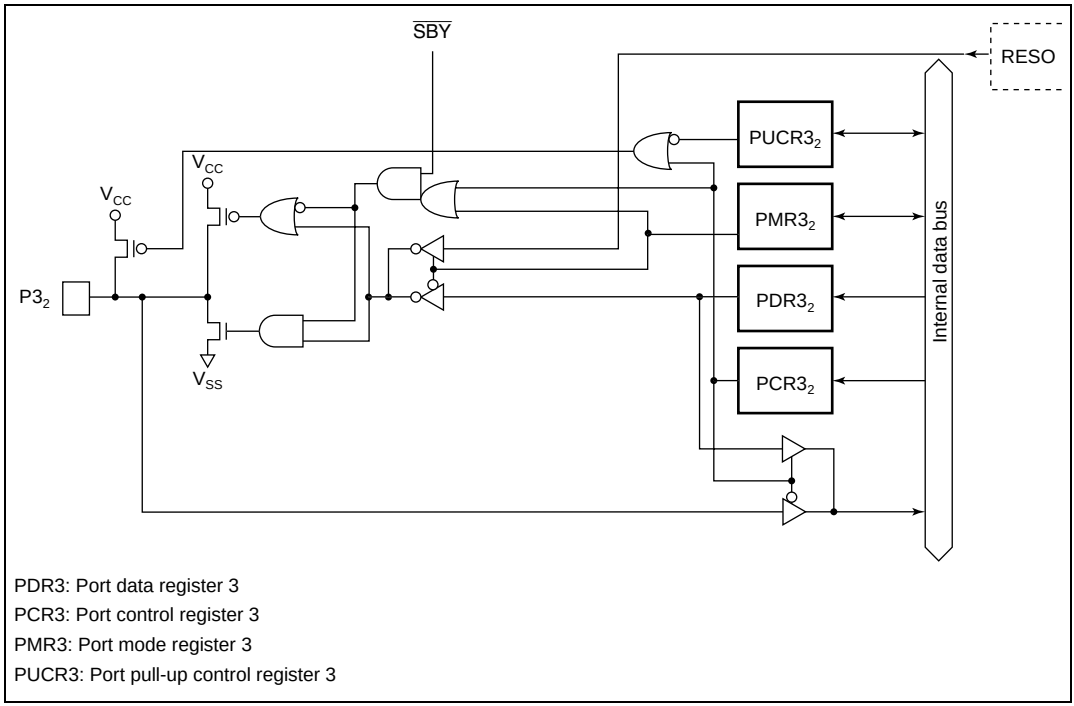


Figure C.3 (e-1) Port 3 Block Diagram (Pin $P3_2$, H8/3847R Group and H8/3847S Group)

C.11 Block Diagram of Port B

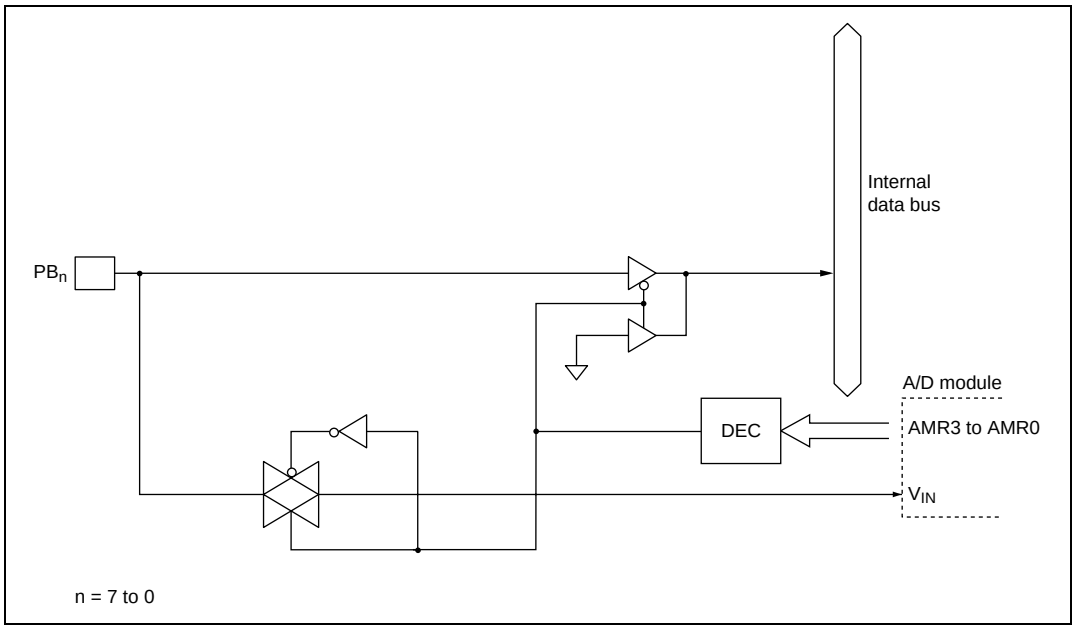


Figure C.11 Port B Block Diagram

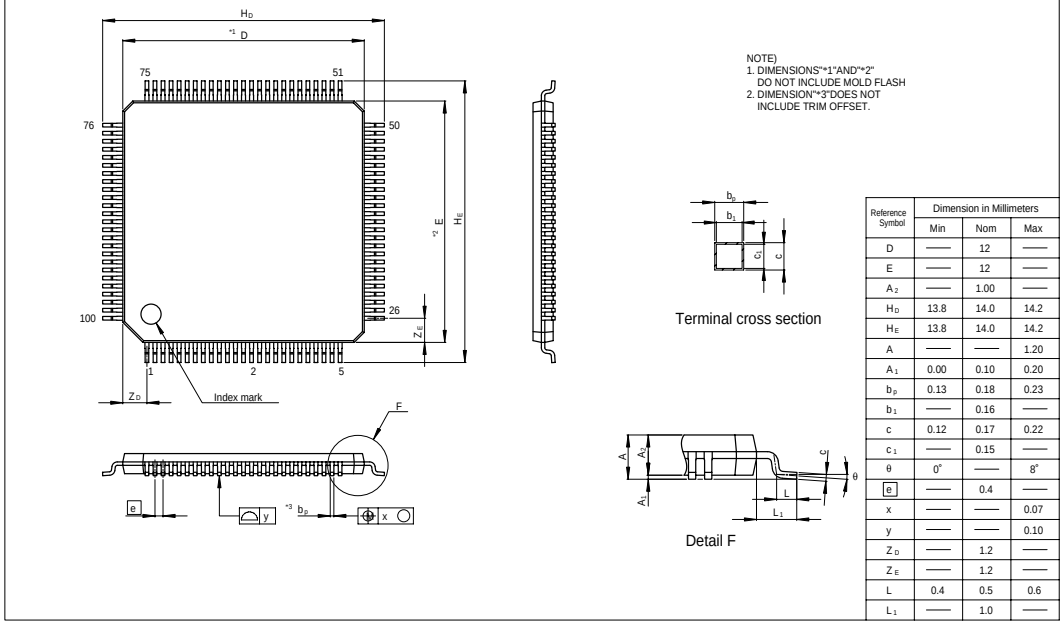
Appendix D Port States in the Different Processing States

Table D.1 Port States Overview

Port	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P1_7$ to $P1_0$	High-impedance	Retained	Retained	High-impedance*1	Retained	Functions	Functions
$P2_7$ to $P2_0$	High-impedance*3	Retained	Retained	High-impedance	Retained	Functions	Functions
$P3_7$ to $P3_0$	High-impedance*2	Retained	Retained	High-impedance*1	Retained	Functions	Functions
$P4_3$ to $P4_0$	High-impedance	Retained	Retained	High-impedance	Retained	Functions	Functions
$P5_7$ to $P5_0$	High-impedance	Retained	Retained	High-impedance*1	Retained	Functions	Functions
$P6_7$ to $P6_0$	High-impedance	Retained	Retained	High-impedance	Retained	Functions	Functions
$P7_7$ to $P7_0$	High-impedance	Retained	Retained	High-impedance	Retained	Functions	Functions
$P8_7$ to $P8_0$	High-impedance	Retained	Retained	High-impedance	Retained	Functions	Functions
$P9_7$ to $P9_0$	High-impedance	Retained	Retained	High-impedance	Retained	Functions	Functions
PA_3 to PA_0	High-impedance	Retained	Retained	High-impedance	Retained	Functions	Functions
PB_7 to PB_0	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance
PC_3 to PC_0	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance	High-impedance

Notes: 1. High level output when MOS pull-up is in on state.
2. Reset output from $P3_2$ pin only (H8/3847R Group and H8/3847S Group).
3. On-chip pull-up MOS turns on for pin $P2_4$ only (F-ZTAT Version of the H8/38347 Group and H8/38447 Group).

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TQFP100-12x12-0.40	PTQP0100LC-A	TFP-100G/TFP-100GV	0.4g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	12	——
E	——	12	——
A_2	——	1.00	——
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	——	——	1.20
A_1	0.00	0.10	0.20
b_p	0.13	0.18	0.23
b_1	——	0.16	——
c	0.12	0.17	0.22
c_1	——	0.15	——
θ	0°	——	8°
e	——	0.4	——
x	——	——	0.07
y	——	——	0.10
Z_D	——	1.2	——
Z_E	——	1.2	——
L	0.4	0.5	0.6
L_1	——	1.0	——

Figure F.4 TFP-100G Package Dimension