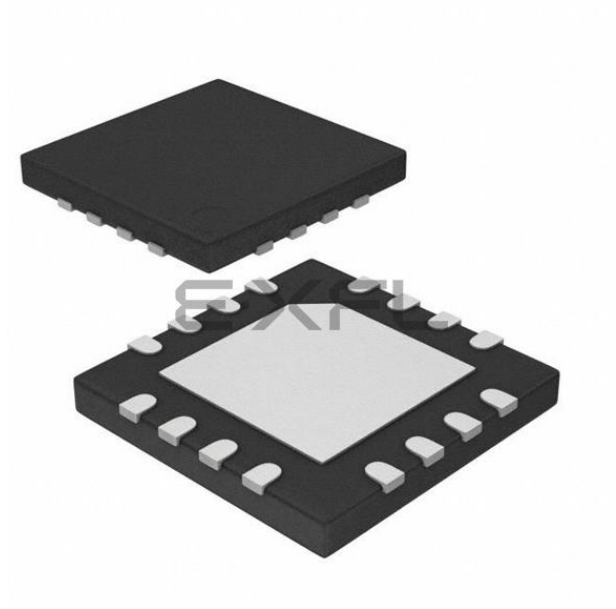

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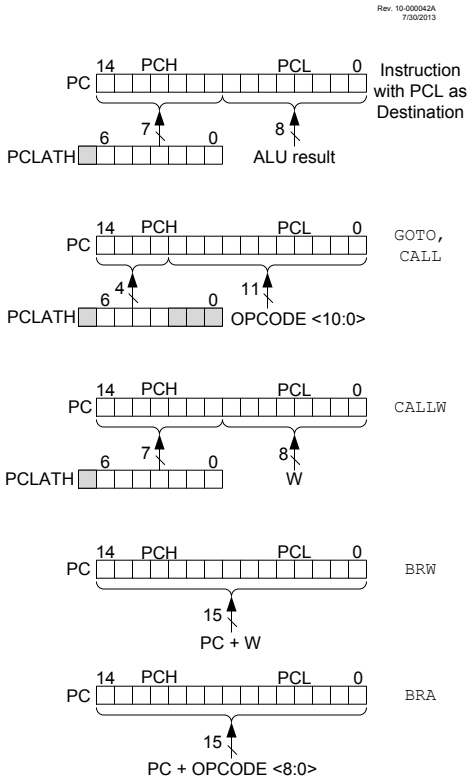
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18426-e-jq

Figure 7-3. Loading of PC in Different Situations



7.4.1 Modifying PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

7.4.2 Computed GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

7.4.3 Computed Function Calls

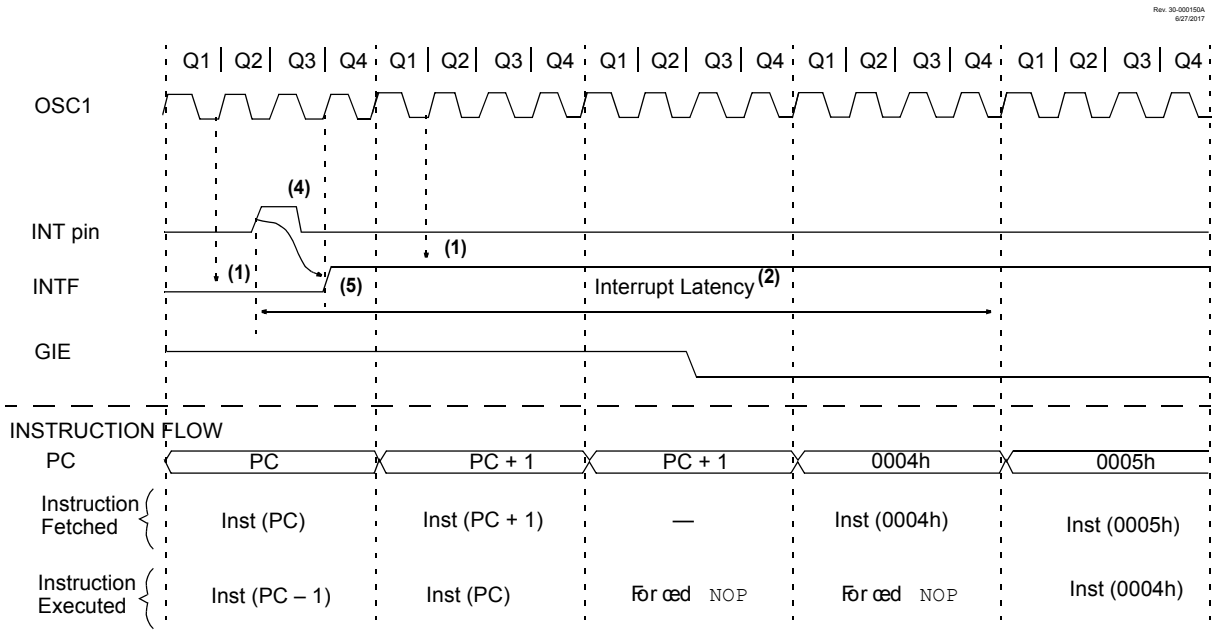
A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

Value	Description
1	The PLL is ready to be used
0	The PLL is not enabled, the required input source is not ready, or the PLL is not locked.

1. An interrupt may occur at any time during the interrupt window.
2. Since an interrupt may occur any time during the interrupt window, the actual latency can vary.

Figure 10-3. INT Pin Interrupt Timing



Note:

1. INTF flag is sampled here (every Q1).
2. Asynchronous interrupt latency = 3-5 T_{CY}. Synchronous latency = 3-4 T_{CY}, where T_{CY} = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. For minimum width of INT pulse, refer to AC specifications in the *"Electrical Specifications"* section.
4. INTF may be set any time during the Q4-Q1 cycles.

10.3 Interrupts During Sleep

Interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the `SLEEP` instruction. The instruction directly after the `SLEEP` instruction will always be executed before branching to the ISR.

Related Links

Power-Saving Operation Modes

10.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. Refer to Figure 10-3. This interrupt is enabled by setting the INTE bit of the PIE0 register. The INTEDG bit of the INTCON register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF

10.7.8 PIE6

Name: PIE6
Address: 0x71C

Peripheral Interrupt Enable Register 6

Bit	7	6	5	4	3	2	1	0
					CCP4IE	CCP3IE	CCP2IE	CCP1IE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – CCP4IE CCP4 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 2 – CCP3IE CCP3 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 1 – CCP2IE CCP2 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 0 – CCP1IE CCP1 Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

10.7.12 PIR1

Name: PIR1
Address: 0x70D

Peripheral Interrupt Request (Flag) Register 1

Bit	7	6	5	4	3	2	1	0
	OSFIF	CSWIF					ADTIF	ADIF
Access	R/W/HS	R/W/HS					R/W/HS	R/W/HS
Reset	0	0					0	0

Bit 7 – OSFIF Oscillator Fail Interrupt Flag bit

Value	Description
1	Oscillator fail-safe interrupt has occurred (must be cleared in software)
0	No oscillator fail-safe interrupt

Bit 6 – CSWIF Clock-Switch Complete Interrupt Flag bit

Value	Description
1	The clock switch module indicates an interrupt condition and is ready to complete the clock switch operation (must be cleared in software)
0	The clock switch does not indicate an interrupt condition

Bit 1 – ADTIF ADC Threshold Interrupt Flag bit

Value	Description
1	An A/D conversion or complex operation has completed (must be cleared in software)
0	An A/D conversion or complex operation is not complete

Bit 0 – ADIF ADC Interrupt Flag bit

Value	Description
1	An A/D conversion or complex operation has completed (must be cleared in software)
0	An A/D conversion or complex operation is not complete

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON appropriate interrupt flag bits are clear prior to enabling an interrupt.

2. When WDTCPS in CONFIG3 = 11111, the Reset value (q) of WDTPS is '01011'. Otherwise, the Reset value of WDTPS is equal to WDTCPS in CONFIG3.
3. When WDTCPS in CONFIG3L ≠ 11111, these bits are read-only.

13.5 Register Summary: NVM Control

Offset	Name	Bit Pos.								
0x081A	NVMADR	7:0	NVMADRL[7:0]							
		15:8		NVMADRH[6:0]						
0x081C	NVMDAT	7:0	NVMDATL[7:0]							
		15:8			NVMDATH[5:0]					
0x081E	NVMCON1	7:0		NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD
0x081F	NVMCON2	7:0	NVMCON2[7:0]							

13.6 Register Definitions: Nonvolatile Memory

Offset	Name	Bit Pos.									
0x1EBF ... 0x1EC2	Reserved										
0x1EC3	ADACTPPS	7:0				PORT[1:0]		PIN[2:0]			
0x1EC4	Reserved										
0x1EC5	SSP1CLKPPS	7:0				PORT[1:0]		PIN[2:0]			
0x1EC6	SSP1DATPPS	7:0				PORT[1:0]		PIN[2:0]			
0x1EC7	SSP1SSPPS	7:0				PORT[1:0]		PIN[2:0]			
0x1EC8	SSP2CLKPPS	7:0				PORT[1:0]		PIN[2:0]			
0x1EC9	SSP2DATPPS	7:0				PORT[1:0]		PIN[2:0]			
0x1ECA	SSP2SSPPS	7:0				PORT[1:0]		PIN[2:0]			
0x1ECB	RX1PPS	7:0				PORT[1:0]		PIN[2:0]			
0x1ECC	CK1PPS	7:0				PORT[1:0]		PIN[2:0]			
0x1ECD ... 0x1F0F	Reserved										
0x1F10	RA0PPS	7:0			PPS[5:0]						
0x1F11	RA1PPS	7:0			PPS[5:0]						
0x1F12	RA2PPS	7:0			PPS[5:0]						
0x1F13	Reserved										
0x1F14	RA4PPS	7:0			PPS[5:0]						
0x1F15	RA5PPS	7:0			PPS[5:0]						
0x1F16 ... 0x1F1B	Reserved										
0x1F1C	RB4PPS	7:0			PPS[5:0]						
0x1F1D	RB5PPS	7:0			PPS[5:0]						
0x1F1E	RB6PPS	7:0			PPS[5:0]						
0x1F1F	RB7PPS	7:0			PPS[5:0]						
0x1F20	RC0PPS	7:0			PPS[5:0]						
0x1F21	RC1PPS	7:0			PPS[5:0]						
0x1F22	RC2PPS	7:0			PPS[5:0]						
0x1F23	RC3PPS	7:0			PPS[5:0]						
0x1F24	RC4PPS	7:0			PPS[5:0]						
0x1F25	RC5PPS	7:0			PPS[5:0]						
0x1F26	RC6PPS	7:0			PPS[5:0]						
0x1F27	RC7PPS	7:0			PPS[5:0]						

15.9 Register Definitions: PPS Input and Output Selection

25.6.1 T0CON0

Name: T0CON0
Address: 0x59E

Timer0 Control Register 0

Bit	7	6	5	4	3	2	1	0
	T0EN		T0OUT	T016BIT	T0OUTPS[3:0]			
Access	R/W		R	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 – T0EN TMR0 Enable bit

Value	Description
1	The module is enabled and operating
0	The module is disabled

Bit 5 – T0OUT TMR0 Output bit

Bit 4 – T016BIT TMR0 Operating as 16-Bit Timer Select bit

Value	Description
1	TMR0 is a 16-bit timer
0	TMR0 is an 8-bit timer

Bits 3:0 – T0OUTPS[3:0] TMR0 Output Postscaler (Divider) Select bits

Value	Description
1111	1:16 Postscaler
1110	1:15 Postscaler
1101	1:14 Postscaler
1100	1:13 Postscaler
1011	1:12 Postscaler
1010	1:11 Postscaler
1001	1:10 Postscaler
1000	1:9 Postscaler
0111	1:8 Postscaler
0110	1:7 Postscaler
0101	1:6 Postscaler
0100	1:5 Postscaler
0011	1:4 Postscaler
0010	1:3 Postscaler
0001	1:2 Postscaler
0000	1:1 Postscaler

Value	Description
0001	1:2 Postscaler
0000	1:1 Postscaler

Note:

1. In certain modes, the ON bit will be auto-cleared by hardware. See Table 27-3.

28. CCP/PWM Timer Resource Selection

Each CCP/PWM module has an independent timer selection which can be accessed using the CxTSEL or PxTSEL bits in the CCPTMRS0 and/or CCPTMRS1 registers. The default timer selection is TMR1 when using Capture/Compare mode and T2TMR when using PWM mode in the CCPx module. The default timer selection for the PWM module is always T2TMR.

31.15.6 CWGxAS0

Name: CWGxAS0
Address: 0x612,0x61C

CWG Auto-Shutdown Control Register 0

Bit	7	6	5	4	3	2	1	0
	SHUTDOWN	REN	LSBD[1:0]		LSAC[1:0]			
Access	R/W/HS/HC	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	1	0	1		

Bit 7 – SHUTDOWN Auto-Shutdown Event Status bit(1,2)

Value	Description
1	An auto-shutdown state is in effect
0	No auto-shutdown event has occurred

Bit 6 – REN Auto-Restart Enable bit

Value	Description
1	Auto-restart is enabled
0	Auto-restart is disabled

Bits 5:4 – LSBD[1:0] CWGxB and CWGxD Auto-Shutdown State Control bits

Value	Description
11	A logic '1' is placed on CWGxB/D when an auto-shutdown event occurs.
10	A logic '0' is placed on CWGxB/D when an auto-shutdown event occurs.
01	Pin is tri-stated on CWGxB/D when an auto-shutdown event occurs.
00	The inactive state of the pin, including polarity, is placed on CWGxB/D after the required dead-band interval when an auto-shutdown event occurs.

Bits 3:2 – LSAC[1:0] CWGxA and CWGxC Auto-Shutdown State Control bits

Value	Description
11	A logic '1' is placed on CWGxA/C when an auto-shutdown event occurs.
10	A logic '0' is placed on CWGxA/C when an auto-shutdown event occurs.
01	Pin is tri-stated on CWGxA/C when an auto-shutdown event occurs.
00	The inactive state of the pin, including polarity, is placed on CWGxA/C after the required dead-band interval when an auto-shutdown event occurs.

Note:

1. This bit may be written while EN = 0 (CWGxCON0), to place the outputs into the shutdown configuration.
2. The outputs will remain in auto-shutdown state until the next rising edge of the CWG data input after this bit is cleared.

33.8.8 CLCxGLS1

Name: CLCxGLS1
Address: 0x1E17,0x1E21,0x1E2B,0x1E35

CLCx Gate2 Logic Select Register

Bit	7	6	5	4	3	2	1	0
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 – G2DyT
dyT: Gate2 Data 'y' True (non-inverted) bit
Reset States: Default = xxxx
POR/BOR = x
All Other Resets = u

Value	Description
1	dyT is gated into g2
0	dyT is not gated into g2

Bits 0, 2, 4, 6 – G2DyN
dyN: Gate2 Data 'y' Negated (inverted) bit
Reset States: Default = xxxx
POR/BOR = x
All Other Resets = u

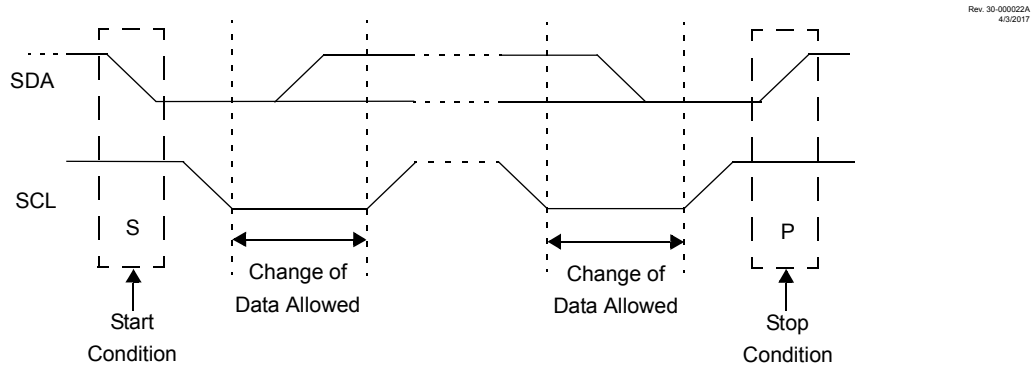
Value	Description
1	dyN is gated into g2
0	dyN is not gated into g2

35.4.8 Stop Condition

A Stop condition is a transition of the SDA line from low-to-high state while the SCL line is high.

Important: At least one SCL low time must appear before a Stop is valid, therefore, if the SDA line goes low then high again while the SCL line stays high, only the Start condition is detected.

Figure 35-12. I²C Start and Stop Conditions



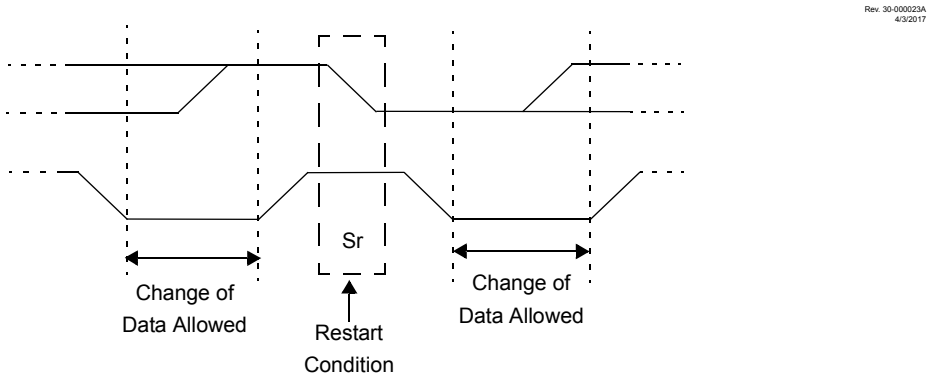
35.4.9 Restart Condition

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 35-13 shows the wave form for a Restart condition.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/$\overline{W}$ bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/$\overline{W}$ clear in 10-bit mode, a prior match flag is set and maintained until a Stop condition, a high address with R/$\overline{W}$ clear, or high address match fails.

Figure 35-13. I²C Restart Condition



SSEL<4:0>	SMT1 Signal Source
01000	CCP1OUT
00111	TMR6 postscaled output
00110	TMR5 overflow
00101	TMR4 postscaled output
00100	TMR3 overflow
00011	TMR2 postscaled output
00010	TMR1 overflow
00001	TMR0 overflow
00000	Pin Selected by SMT1SIGPPS

Table 37-3. SMT Window Selection

WSEL<4:0>	SMT1 Window Source
11111-11000	Reserved
10111	NCO1OUT
10110	Reserved
10101	CLKREFOUT
10100	CLC4OUT
10011	CLC3OUT
10010	CLC2OUT
10001	CLC1OUT
10000	ZCDOUT
01111	C2OUT
01110	C1OUT
01101	PWM7OUT
01100	PWM6OUT
01011	CCP4OUT
01010	CCP3OUT
01001	CCP2OUT
01000	CCP1OUT
00111	TMR6_postscaled_out
00110	TMR4_postscaled_out
00101	TMR2_postscaled_out

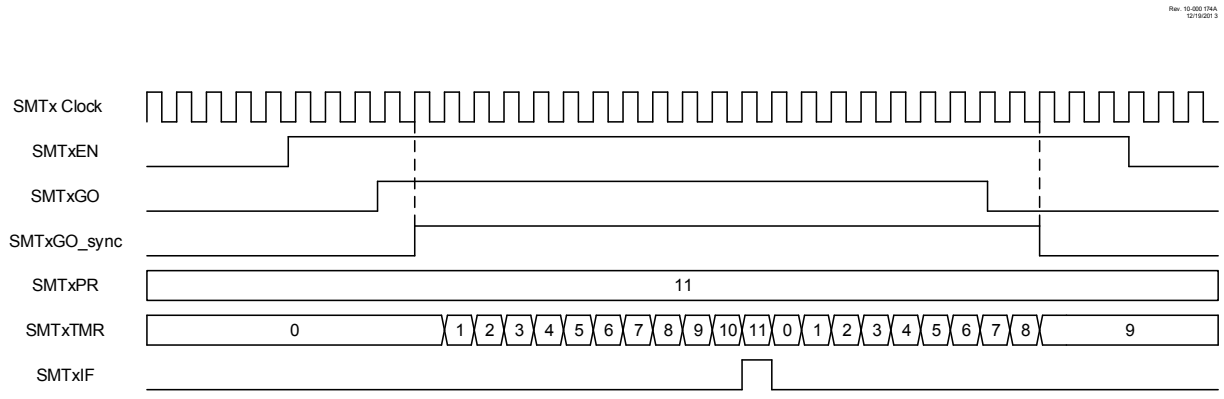
Table 37-4. Modes of Operation

MODE	Mode of operation	Synchronous operation
0000	Timer	Yes
0001	Gated Timer	Yes
0010	Period and Duty Cycle Measurement	Yes
0011	High and low time Measurement	Yes
0100	Windowed Measurement	Yes
0101	Gated Windowed Measurement	Yes
0110	Time of Flight Measurement	Yes
0111	Capture	Yes
1000	Counter	No
1001	Gated Counter	No
1010	Windowed Counter	No
1011-1111	Reserved	-

37.1.6.1 Timer Mode

Timer mode is the basic mode of operation where the SMTxTMR is used as a 24-bit timer. No data acquisition takes place in this mode. The timer increments as long as the SMTxGO bit has been set by software. No SMT window or SMT signal events affect the SMTxGO bit. Everything is synchronized to the SMT clock source. When the timer experiences a period match (SMTxTMR = SMTxPR), SMTxTMR is reset and the period match interrupt trips. See figure below.

Figure 37-2. Timer Mode Timing Diagram



37.1.6.2 Gated Timer Mode

Gated Timer mode uses the signal input (SSEL) to control whether or not the SMTxTMR will increment. Upon a falling edge of the signal, the SMTxCPW register will update to the current value of the SMTxTMR. Example waveforms for both repeated and single acquisitions are provided in figures below.

Offset	Name	Bit Pos.								
0x028E	T2CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x028F	T2HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x0290	T2CLKCON	7:0					CS[3:0]			
0x0291	T2RST	7:0					RSEL[3:0]			
0x0292	T4TMR	7:0	TxTMR[7:0]							
0x0293	T4PR	7:0	TxPR[7:0]							
0x0294	T4CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x0295	T4HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x0296	T4CLKCON	7:0					CS[3:0]			
0x0297	T4RST	7:0					RSEL[3:0]			
0x0298	T6TMR	7:0	TxTMR[7:0]							
0x0299	T6PR	7:0	TxPR[7:0]							
0x029A	T6CON	7:0	ON		CKPS[2:0]		OUTPS[3:0]			
0x029B	T6HLT	7:0	PSYNC	CPOL	CSYNC	MODE[4:0]				
0x029C	T6CLKCON	7:0					CS[3:0]			
0x029D	T6RST	7:0					RSEL[3:0]			
0x029E	Reserved									
0x029F	ADCPCON0	7:0	CPON							CPRDY
0x02A0 ... 0x02FF	Reserved									
0x0300	INDF0	7:0	INDF0[7:0]							
0x0301	INDF1	7:0	INDF1[7:0]							
0x0302	PCL	7:0	PCL[7:0]							
0x0303	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0304	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0306	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0308	BSR	7:0			BSR[5:0]					
0x0309	WREG	7:0	WREG[7:0]							
0x030A	PCLATH	7:0		PCLATH[6:0]						
0x030B	INTCON	7:0	GIE	PEIE						INTEDG
0x030C	CCPR1	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x030E	CCP1CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x030F	CCP1CAP	7:0						CTS[2:0]		
0x0310	CCPR2	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x0312	CCP2CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x0313	CCP2CAP	7:0						CTS[2:0]		
0x0314	CCPR3	7:0	CCPRL[7:0]							
		15:8	CCPRH[7:0]							
0x0316	CCP3CON	7:0	EN		OUT	FMT	MODE[3:0]			
0x0317	CCP3CAP	7:0						CTS[2:0]		
0x0318	CCPR4	7:0	CCPRL[7:0]							

Offset	Name	Bit Pos.								
0x1E10	CLC1CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E11	CLC1POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E12	CLC1SEL0	7:0			D1S[5:0]					
0x1E13	CLC1SEL1	7:0			D2S[5:0]					
0x1E14	CLC1SEL2	7:0			D3S[5:0]					
0x1E15	CLC1SEL3	7:0			D4S[5:0]					
0x1E16	CLC1GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E17	CLC1GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E18	CLC1GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E19	CLC1GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E1A	CLC2CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E1B	CLC2POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E1C	CLC2SEL0	7:0			D1S[5:0]					
0x1E1D	CLC2SEL1	7:0			D2S[5:0]					
0x1E1E	CLC2SEL2	7:0			D3S[5:0]					
0x1E1F	CLC2SEL3	7:0			D4S[5:0]					
0x1E20	CLC2GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E21	CLC2GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E22	CLC2GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E23	CLC2GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E24	CLC3CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E25	CLC3POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E26	CLC3SEL0	7:0			D1S[5:0]					
0x1E27	CLC3SEL1	7:0			D2S[5:0]					
0x1E28	CLC3SEL2	7:0			D3S[5:0]					
0x1E29	CLC3SEL3	7:0			D4S[5:0]					
0x1E2A	CLC3GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E2B	CLC3GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E2C	CLC3GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E2D	CLC3GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E2E	CLC4CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E2F	CLC4POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E30	CLC4SEL0	7:0			D1S[5:0]					
0x1E31	CLC4SEL1	7:0			D2S[5:0]					
0x1E32	CLC4SEL2	7:0			D3S[5:0]					
0x1E33	CLC4SEL3	7:0			D4S[5:0]					
0x1E34	CLC4GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E35	CLC4GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E36	CLC4GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E37	CLC4GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E38 ... 0x1E7F	Reserved									
0x1E80	INDF0	7:0	INDF0[7:0]							
0x1E81	INDF1	7:0	INDF1[7:0]							
0x1E82	PCL	7:0	PCL[7:0]							

PIC16F18426/46 only								
Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**	
							V_{DD}	**Note**
D102	$I_{DD_{HFOPLL}}$	HFINTOSC = 32 MHz	—	3.7	5.6	mA	3.0V	
D103	$I_{DD_{HSPLL32}}$	HS+PLL = 32 MHz	—	3.7	5.7	mA	3.0V	
D104	$I_{DD_{IDLE}}$	IDLE mode, HFINTOSC = 16 MHz	—	1.8	2.1	mA	3.0V	
D105	$I_{DD_{DOZE}}$ (3)	DOZE mode, HFINTOSC = 16 MHz, Doze Ratio = 16	—	1.6	—	mA	3.0V	

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins are outputs driven low; $\overline{MCLR}$ = V_{DD}; WDT disabled.
2. The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
3. $I_{DD_{DOZE}}$ = [$I_{DD_{IDLE}}$*(N-1)/N] + $I_{DD_{HFO}}$16/N where N = DOZE Ratio (see *CPUDOZE* register).
4. PMD bits are all in the default state, no modules are disabled.

Related Links

CPUDOZE

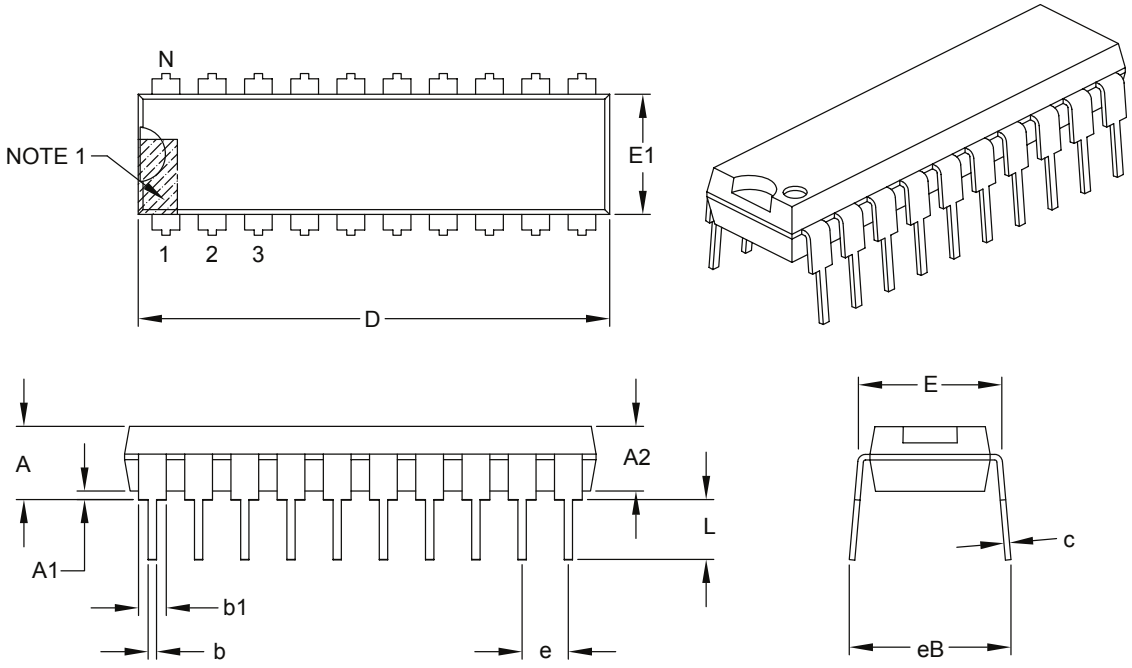
42.3.3 Power-Down Current (I_{PD})(1,2)

Table 42-3.

PIC16LF18426/46 only									
Standard Operating Conditions (unless otherwise stated)									
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
								V_{DD}	**Note**
D200	I_{PD}	I_{PD} Base	—	0.06	2	9	µA	3.0V	
D201	I_{PD_WDT}	Low-Frequency Internal Oscillator/WDT	—	0.8	4.0	11	µA	3.0V	

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B