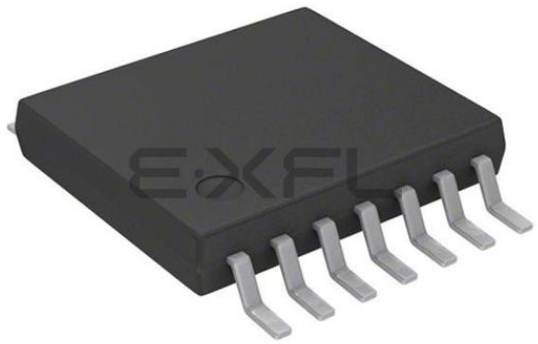

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18426-e-st

7.10.3 BSR_SHAD

Name: BSR_SHAD
Address: 0x1FE6

Shadow of Bank Select Register

The BSR indicates the data memory bank by writing the bank number into the register. All data memory can be accessed directly via instructions, or indirectly via FSRs.

Bit	7	6	5	4	3	2	1	0
			BSR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 5:0 – BSR[5:0]
Six Most Significant bits of the data memory address
Reset States: POR/BOR = xxxxxx
All Other Resets = uuuuuu

9.6.5 OSCEN

Name: OSCEN
Address: 0x891

Oscillator Manual Enable Register

Bit	7	6	5	4	3	2	1	0
	EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit 7 – EXTOEN External Oscillator Manual Request Enable bit

Value	Description
1	EXTOSC is explicitly enabled, operating as specified by CONFIG1[FEXTOSC]
0	EXTOSC is only enabled if requested by a peripheral

Bit 6 – HFOEN HFINTOSC Oscillator Manual Request Enable bit

Value	Description
1	HFINTOSC is explicitly enabled, operating as specified by OSCFRQ
0	HFINTOSC is only enabled if requested by a peripheral

Bit 5 – MFOEN MFINTOSC (500 kHz/31.25 kHz) Oscillator Manual Request Enable bit (Derived from HFINTOSC)

Value	Description
1	MFINTOSC is explicitly enabled
0	MFINTOSC is only enabled if requested by a peripheral

Bit 4 – LFOEN LFINTOSC (31 kHz) Oscillator Manual Request Enable bit

Value	Description
1	LFINTOSC is explicitly enabled
0	LFINTOSC is only enabled if requested by a peripheral

Bit 3 – SOSCEN Secondary Oscillator Manual Request Enable bit

Value	Description
1	Secondary Oscillator is explicitly enabled, operating as specified by SOSCPWR
0	Secondary Oscillator is only enabled if requested by a peripheral

Bit 2 – ADOEN ADC Oscillator Manual Request Enable bit

Value	Description
1	ADC oscillator is explicitly enabled
0	ADC oscillator is only enabled if requested by a peripheral

Related Links

CONFIG1

11.4 Register Summary - Power Savings Control

Offset	Name	Bit Pos.								
0x0812	VREGCON	7:0							VREGPM	
0x0813 ... 0x088B	Reserved									
0x088C	CPUDOZE	7:0	IDLEN	DOZEN	ROI	DOE		DOZE[2:0]		

11.5 Register Definitions: Power Savings Control

14.6.8 LATB

Name: LATB
Address: 0x019

Output Latch Register

Bit	7	6	5	4	3	2	1	0
	LATB7	LATB6	LATB5	LATB4				
Access	R/W	R/W	R/W	R/W				
Reset	x	x	x	x				

Bits 4, 5, 6, 7 – LATBn Output Latch B Value bits
Reset States: POR/BOR = xxxx
All Other Resets = uuuuu

Note: Writes to LATB are equivalent with writes to the corresponding PORTB register. Reads from LATB register return register values, not I/O pin values.

14.6.10 ANSELA

Name: ANSELA
Address: 0x1F38

Analog Select Register

Bit	7	6	5	4	3	2	1	0
			ANSELA5	ANSELA4		ANSELA2	ANSELA1	ANSELA0
Access			R/W	R/W		R/W	R/W	R/W
Reset			1	1		1	1	1

Bits 4, 5 – ANSELAn Analog Select on RA Pins

Value	Description
1	Analog input. Pin is assigned as analog input. Digital input buffer disabled.
0	Digital I/O. Pin is assigned to port or digital special function.

Bits 0, 1, 2 – ANSELAn Analog Select on RA Pins

Value	Description
1	Analog input. Pin is assigned as analog input. Digital input buffer disabled.
0	Digital I/O. Pin is assigned to port or digital special function.

Note: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

20.6.1 Digital Filter/Average

The digital filter/average module consists of an accumulator with data feedback options, and control logic to determine when threshold tests need to be applied. The accumulator is a 16-bit wide register which can be accessed through the ADACCH:ADACCL register pair.

Upon each trigger event (the GO bit set or external event trigger), the ADC conversion result is added to the accumulator. If the accumulated result exceeds $2^{(accumulator\_width)}$-1, the OV Accumulator overflow bit is set.

The number of samples to be accumulated is determined by the ADRPT (A/D Repeat Setting) register. Each time a sample is added to the accumulator, the ADCNT register is incremented. Once ADRPT samples are accumulated (ADCNT = ADRPT), an accumulator clear command can be issued by the software by setting the ACLR bit. Setting the ACLR bit will also clear the OV bit, as well as the ADCNT register. The ACLR bit is cleared by the hardware when accumulator clearing action is complete.

Important: When ADC is operating from FRC, five FRC clock cycles are required to execute the ADACC clearing operation.

The CRS bits control the data shift on the accumulator result, which effectively divides the value in accumulator (ADACCU:ADACCH:ADACCL) register pair. For the Accumulate mode of the digital filter, the shift provides a simple scaling operation. For the Average/Burst Average mode, the shift bits are used to determine the number of logical right shifts to be performed on the accumulated result. For the Low-pass Filter mode, the shift is an integral part of the filter, and determines the cut-off frequency of the filter. The table below shows the -3 dB cut-off frequency in ωT (radians) and the highest signal attenuation obtained by this filter at nyquist frequency (ωT = π).

Table 20-5. Low-pass Filter -3 dB Cut-off Frequency

CRS	ωT (radians) @ -3 dB Frequency	dB @ $F_{nyquist}$=1/(2T)
1	0.72	-9.5
2	0.284	-16.9
3	0.134	-23.5
4	0.065	-29.8
5	0.032	-36.0
6	0.016	-42.0
7	0.0078	-48.1

20.6.2 Basic Mode

Basic mode (MD = 000) disables all additional computation features. In this mode, no accumulation occurs but threshold error comparison is performed. Double sampling, Continuous mode, and all CVD features are still available, but no features involving the digital filter/average features are used.

20.6.3 Accumulate Mode

In Accumulate mode (MD = 001), after every conversion, the ADC result is added to the ADACC register. The ADACC register is right-shifted by the value of the CRS bits. This right-shifted value is copied into the ADFLT register. The Formatting mode does not affect the right-justification of the ADFLT value. Upon

20.8.5 ADSTAT

Name: ADSTAT
Address: 0x115

ADC Status Register

Bit	7	6	5	4	3	2	1	0
	OV	UTHR	LTHR	MATH		STAT[2:0]		
Access	RO	RO	RO	R/HS/HC		RO	RO	RO
Reset	0	0	0	0		0	0	0

Bit 7 – OV ADC Accumulator Overflow bit

Value	Description
1	ADC accumulator or ERR calculation have overflowed
0	ADC accumulator and ERR calculation have not overflowed

Bit 6 – UTHR ADC Module Greater-than Upper Threshold Flag bit

Value	Description
1	ERR >UTH
0	ERR≤UTH

Bit 5 – LTHR ADC Module Less-than Lower Threshold Flag bit

Value	Description
1	ERR<LTH
0	ERR≥LTH

Bit 4 – MATH ADC Module Computation Status bit

Value	Description
1	Registers ADACC, ADFLTR, ADUTH, ADLTH and the OV bit are updating or have already updated
0	Associated registers/bits have not changed since this bit was last cleared

Bits 2:0 – STAT[2:0] ADC Module Cycle Multistage Status bits(1)

Value	Description
111	ADC module is in 2nd conversion stage
110	ADC module is in 2nd acquisition stage
101	ADC module is in 2nd precharge stage
100	Not used
011	ADC module is in 1st conversion stage
010	ADC module is in 1st acquisition stage
001	ADC module is in 1st precharge stage
000	ADC module is not converting

Note:

1. If CS = 1, and F_{OSC}<FRC, these bits may be invalid.

26.14.2 TxGCON

Name: TxGCON
Address: 0x20F,0x215,0x21B

Timer Gate Control Register

Bit	7	6	5	4	3	2	1	0
	GE	GPOL	GTM	GSPM	GGO/DONE	GVAL		
Access	R/W	R/W	R/W	R/W	R/W	RO		
Reset	0	0	0	0	0	x		

Bit 7 – GE Timer Gate Enable bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Condition	Description
1	ON = 1	Timer counting is controlled by the Timer gate function
0	ON = 1	Timer is always counting
X	ON = 0	This bit is ignored

Bit 6 – GPOL Timer Gate Polarity bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer gate is active-high (Timer counts when gate is high)
0	Timer gate is active-low (Timer counts when gate is low)

Bit 5 – GTM Timer Gate Toggle Mode bit
Timer Gate Flip-Flop Toggles on every rising edge

Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer Gate Toggle mode is enabled
0	Timer Gate Toggle mode is disabled and Toggle flip-flop is cleared

Bit 4 – GSPM Timer Gate Single Pulse Mode bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	Timer Gate Single Pulse mode is enabled and is controlling Timer gate)
0	Timer Gate Single Pulse mode is disabled

Bit 3 – GGO/DONE Timer Gate Single Pulse Acquisition Status bit
This bit is automatically cleared when TxGSPM is cleared.

Reset States: POR/BOR = 0
All Other Resets = u

27.9.2 TxPR

Name: TxPR
Address: 0x28D,0x293,0x299

Timer Period Register

Bit	7	6	5	4	3	2	1	0
	TxPR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – TxPR[7:0] Timer Period Register bits

Value	Description
0 - 255	The timer restarts at ‘0’ when TxTMR reaches TxPR value

Table 29-4. Example PWM Frequencies and Resolutions (F_{OSC} = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	16	4	1	1	1	1
T2PR Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

29.4.7 Operation in Sleep Mode

In Sleep mode, the T2TMR register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, T2TMR will continue from the previous state.

29.4.8 Changes in System Clock Frequency

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See the *"Oscillator Module (with Fail-Safe Clock Monitor)"* section for additional details.

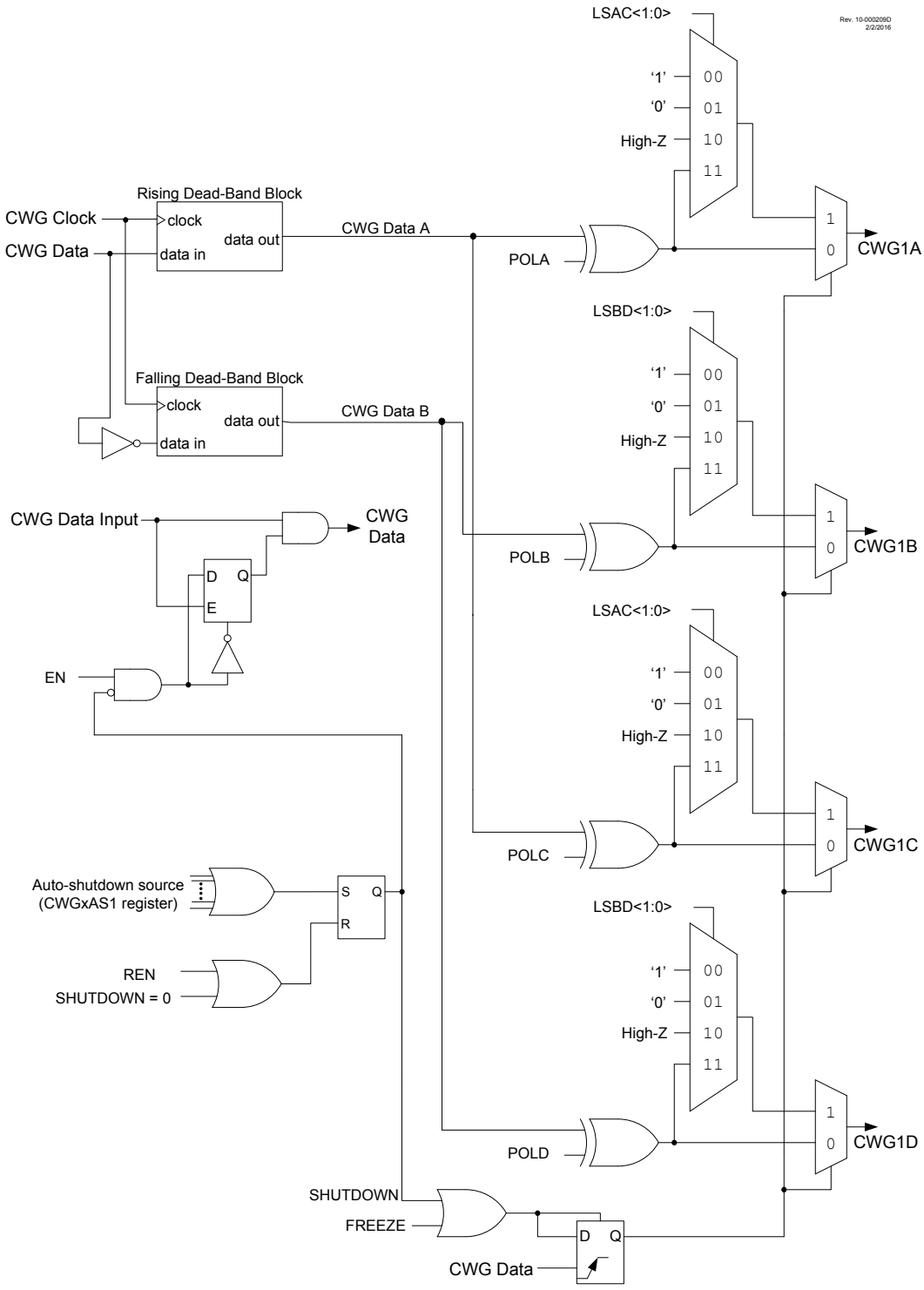
Related Links

Oscillator Module (with Fail-Safe Clock Monitor)

29.4.9 Effects of Reset

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

Figure 31-2. Simplified CWG Block Diagram (Half-Bridge Mode, MODE<2:0> = 100)



31.2.2 Push-Pull Mode

In Push-Pull mode, two output signals are generated, alternating copies of the input as illustrated in Figure 31-3. This alternation creates the push-pull effect required for driving some transformer-based

32.11 Register Summary - DSM

Offset	Name	Bit Pos.								
0x0897	MD1CON0	7:0	EN		OUT	OPOL				BIT
0x0898	MD1CON1	7:0			CHPOL	CHSYNC			CLPOL	CLSYNC
0x0899	MD1SRC	7:0				SRCS[4:0]				
0x089A	MD1CARL	7:0					CLS[3:0]			
0x089B	MD1CARH	7:0					CHS[3:0]			

32.12 Register Definitions: Modulation Control

Long bit name prefixes for the Modulation Control peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 32-4. Modulation Control Long Bit Name Prefixes

Peripheral	Bit Name Prefix
MD	MD

Related Links

Long Bit Names

34.1 Clock Source

The clock source of the reference clock peripheral is selected with the CLK bits. The available clock sources are listed in the following table:

Table 34-1. CLKR Clock Sources

CLK	Clock Source
1111-1011	Reserved
1010	CLC4 OUT
1001	CLC3 OUT
1000	CLC2 OUT
0111	CLC1 OUT
0110	NCO1 OUT
0101	SOSC
0100	MFINTOSC (32 kHz)
0011	MFINTOSC (500 kHz)
0010	LFINTOSC
0001	HFINTOSC (32 MHz)
0000	F_{OSC}

34.1.1 Clock Synchronization

The CLKR output signal is ensured to be glitch-free when the EN bit is set to start the module and enable the CLKR output.

When the reference clock output is disabled, the output signal will be disabled immediately.

Clock dividers and clock duty cycles can be changed while the module is enabled but doing so may cause glitches to occur on the output. To avoid possible glitches, clock dividers and clock duty cycles should be changed only when the EN bit is clear.

34.2 Programmable Clock Divider

The module takes the clock input and divides it based on the value of the DIV bits.

The following configurations are available:

- Base Fosc value
- F_{OSC} divided by 2
- F_{OSC} divided by 4
- F_{OSC} divided by 8
- F_{OSC} divided by 16
- F_{OSC} divided by 32
- F_{OSC} divided by 64
- F_{OSC} divided by 128

35.5.6 Clock Stretching

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

35.5.6.1 Normal Clock Stretching

Following an $\overline{ACK}$ if the R/W bit is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit is set, the slave hardware will always stretch the clock after the $\overline{ACK}$ sequence. Once the slave is ready; CKP is set by software and communication resumes.

Important:

1. The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPxBUF was read before the ninth falling edge of SCL.
2. Previous versions of the module did not stretch the clock for a transmission if SSPxBUF was loaded before the ninth falling edge of SCL. It is now always cleared for read requests.

35.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPxADD.

Important: Previous versions of the module did not stretch the clock if the second address byte did not match.

35.5.6.3 Byte NACKing

When the AHEN bit is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When the DHEN bit is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

35.5.7 Clock Synchronization and the CKP bit

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see the following figure).

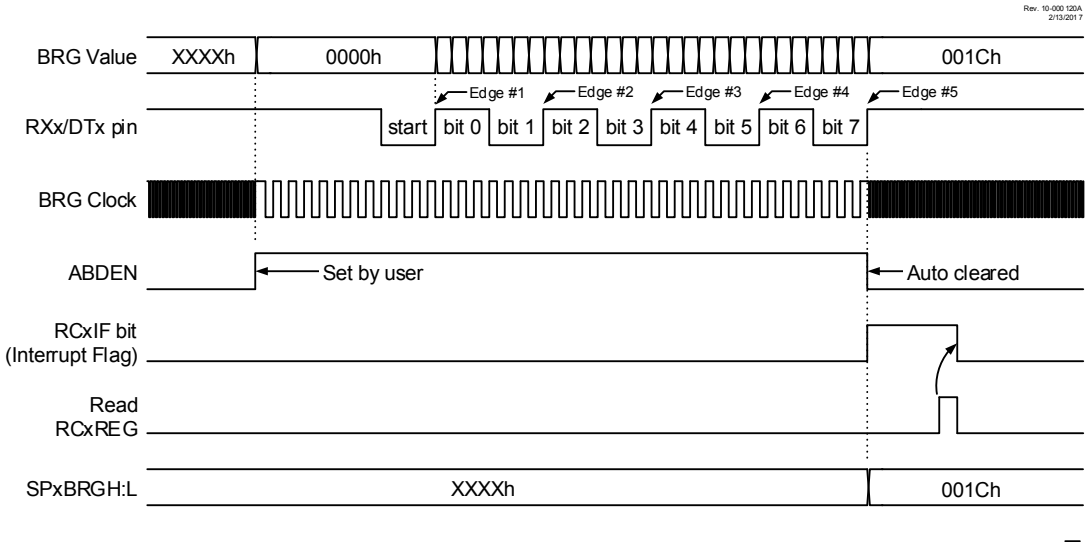
1. If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see Auto-Wake-up on Break).
2. It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.
3. During the auto-baud process, the auto-baud counter starts counting at one. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPxBRGH:SPxBRGL register pair.

Table 36-3. BRG Counter Clock Rates

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
1	1	$F_{OSC}/4$	$F_{OSC}/32$
1	0	$F_{OSC}/16$	$F_{OSC}/128$
0	1	$F_{OSC}/16$	$F_{OSC}/128$
0	0	$F_{OSC}/64$	$F_{OSC}/512$

Note: During the ABD sequence, SPxBRGL and SPxBRGH registers are both used as a 16-bit counter, independent of the BRG16 setting.

Figure 36-7. Automatic Baud Rate Calibration



36.2.2 Auto-Baud Overflow

During the course of automatic baud detection, the ABDOVF bit of the BAUDxCON register will be set if the baud rate counter overflows before the 5th rising edge is detected on the RXx pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPxBRGH:SPxBRGL register pair. After the ABDOVF bit has been set, the counter continues to count until the 5th rising edge is detected on the RXx pin. Upon detecting the 5th RX edge, the hardware will set the RCxIF interrupt flag and clear the ABDEN bit of the BAUDxCON register. The RCxIF flag can be subsequently cleared by reading the RCxREG register. The ABDOVF flag of the BAUDxCON register can be cleared by software directly.

37.3.1 SMTxCON0

Name: SMTxCON0
Address: 0x0498

SMT Control Register 0

Bit	7	6	5	4	3	2	1	0
	EN		STP	WPOL	SPOL	CPOL	PS[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 7 – EN SMT Enable Bit

Value	Description
1	SMT is enabled
0	SMT is disabled; internal states are reset, clock requests are disabled

Bit 5 – STP SMT Counter Halt Enable bit

Value	Condition	Description
1	When SMTxTMR = SMTxPR	Counter remains SMTxPR; period match interrupt occurs when clocked
0	When SMTxTMR = SMTxPR	Counter resets to 0x000000; period match interrupt occurs when clocked

Bit 4 – WPOL SMTxWIN Input Polarity Control bit

Value	Description
1	Window signal is active-low/falling edge enabled
0	Window signal is active-high/rising edge enabled

Bit 3 – SPOL SMTxSIG Input Polarity Control bit

Value	Description
1	SMT Signal is active-low/falling edge enabled
0	SMT Signal is active-high/rising edge enabled

Bit 2 – CPOL SMT Clock Input Polarity Control bit

Value	Description
1	SMTxTMR increments on the falling edge of the selected clock signal
0	SMTxTMR increments on the rising edge of the selected clock signal

Bits 1:0 – PS[1:0] SMT Prescale Select bits

Value	Description
11	Prescaler = 1:8
10	Prescaler = 1:4
01	Prescaler = 1:2
00	Prescaler = 1:1

Offset	Name	Bit Pos.								
0x150A	PCLATH	7:0		PCLATH[6:0]						
0x150B	INTCON	7:0	GIE	PEIE						INTEDG
0x150C ... 0x157F	Reserved									
0x1580	INDF0	7:0	INDF0[7:0]							
0x1581	INDF1	7:0	INDF1[7:0]							
0x1582	PCL	7:0	PCL[7:0]							
0x1583	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1584	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1586	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1588	BSR	7:0			BSR[5:0]					
0x1589	WREG	7:0	WREG[7:0]							
0x158A	PCLATH	7:0		PCLATH[6:0]						
0x158B	INTCON	7:0	GIE	PEIE						INTEDG
0x158C ... 0x15FF	Reserved									
0x1600	INDF0	7:0	INDF0[7:0]							
0x1601	INDF1	7:0	INDF1[7:0]							
0x1602	PCL	7:0	PCL[7:0]							
0x1603	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1604	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1606	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1608	BSR	7:0			BSR[5:0]					
0x1609	WREG	7:0	WREG[7:0]							
0x160A	PCLATH	7:0		PCLATH[6:0]						
0x160B	INTCON	7:0	GIE	PEIE						INTEDG
0x160C ... 0x167F	Reserved									
0x1680	INDF0	7:0	INDF0[7:0]							
0x1681	INDF1	7:0	INDF1[7:0]							
0x1682	PCL	7:0	PCL[7:0]							
0x1683	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1684	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1686	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1688	BSR	7:0			BSR[5:0]					
0x1689	WREG	7:0	WREG[7:0]							
0x168A	PCLATH	7:0		PCLATH[6:0]						

Offset	Name	Bit Pos.								
0x1B7F										
0x1B80	INDF0	7:0	INDF0[7:0]							
0x1B81	INDF1	7:0	INDF1[7:0]							
0x1B82	PCL	7:0	PCL[7:0]							
0x1B83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1B84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B88	BSR	7:0			BSR[5:0]					
0x1B89	WREG	7:0	WREG[7:0]							
0x1B8A	PCLATH	7:0		PCLATH[6:0]						
0x1B8B	INTCON	7:0	GIE	PEIE						INTEDG
0x1B8C ... 0x1BFF	Reserved									
0x1C00	INDF0	7:0	INDF0[7:0]							
0x1C01	INDF1	7:0	INDF1[7:0]							
0x1C02	PCL	7:0	PCL[7:0]							
0x1C03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1C04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1C06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1C08	BSR	7:0			BSR[5:0]					
0x1C09	WREG	7:0	WREG[7:0]							
0x1C0A	PCLATH	7:0		PCLATH[6:0]						
0x1C0B	INTCON	7:0	GIE	PEIE						INTEDG
0x1C0C ... 0x1C7F	Reserved									
0x1C80	INDF0	7:0	INDF0[7:0]							
0x1C81	INDF1	7:0	INDF1[7:0]							
0x1C82	PCL	7:0	PCL[7:0]							
0x1C83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1C84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1C86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1C88	BSR	7:0			BSR[5:0]					
0x1C89	WREG	7:0	WREG[7:0]							
0x1C8A	PCLATH	7:0		PCLATH[6:0]						
0x1C8B	INTCON	7:0	GIE	PEIE						INTEDG
0x1C8C ... 0x1CFF	Reserved									

40. Instruction Set Summary

PIC16(L)F18426/46 devices incorporate the standard set of 50 PIC16 core instructions. Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories:

- Byte Oriented
- Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 37-3 lists the instructions recognized by the MPASM™ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine entry takes two cycles (`CALL`, `CALLW`)
- Returns from interrupts or subroutines take two cycles (`RETURN`, `RETLW`, `RETFIE`)
- Program branching takes two cycles (`GOTO`, `BRA`, `BRW`, `BTFSS`, `BTFSC`, `DECFSZ`, `INCSFZ`)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format ‘`0xhh`’ to represent a hexadecimal number, where ‘`h`’ signifies a hexadecimal digit.

40.1 Read-Modify-Write Operations

Any write instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the working (W) register, or the originating file register, depending on the state of the destination designator 'd' (see the table below for more information). A read operation is performed on a register even if the instruction writes to that register.

Table 40-1. Opcode Field Descriptions

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don’t care location (= `0` or `1`). The assembler will generate code with x = `0`. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = `0`: store result in W, d = `1`: store result in file register f.

PIC16F18426/46 only									
Standard Operating Conditions (unless otherwise stated), VREGPM = 1									
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
								V_{DD}	**Note**
D202	I_{PD_SOSC}	Secondary Oscillator (S_{OSC})	—	0.8	5.5	13	µA	3.0V	
D203	I_{PD_FVR}	FVR	—	28	70	75	µA	3.0V	
D204	I_{PD_BOR}	Brown-out Reset (BOR)	—	14	18	20	µA	3.0V	
D207	I_{PD_ADCA}	ADC - Non-converting	—	0.4	4	12	µA	3.0V	ADC not converting (4)
D208	I_{PD_CMP}	Comparator	—	33	49	57	µA	3.0V	

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. The peripheral current is the sum of the base I_{DD} and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base I_{DD} or I_{PD}current from this limit. Max. values should be used when calculating total current consumption.
2. The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to V_{SS}.
3. All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.
4. ADC clock source is FRC.

42.3.4 I/O Ports

Table 42-4.

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
Input Low Voltage							
	V_{IL}	I/O PORT:					
D300		• with TTL buffer	—	—	0.8	V	$4.5V \le V_{DD} \le 5.5V$
D301			—	—	0.15 V_{DD}	V	$1.8V \le V_{DD} \le 4.5V$
D302		• with Schmitt Trigger buffer	—	—	0.2 V_{DD}	V	$2.0V \le V_{DD} \le 5.5V$
D303		• with I^2C levels	—	—	0.3 V_{DD}	V	
D304		• with SMBus levels	—	—	0.8	V	$2.7V \le V_{DD} \le 5.5V$