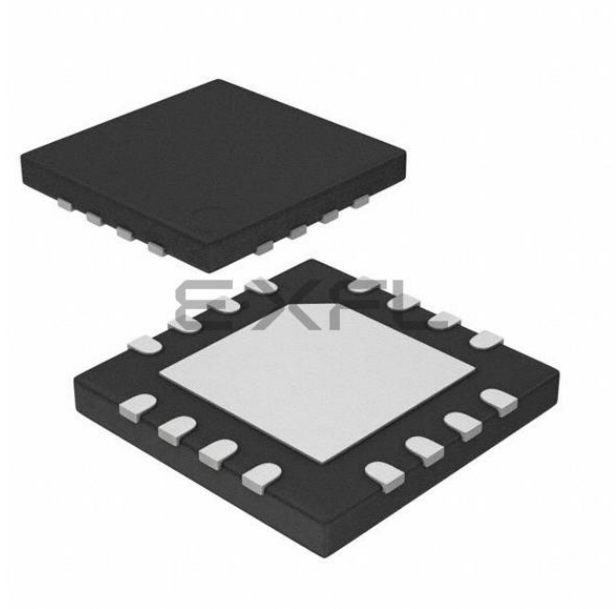

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 12 |
| Program Memory Size | 28KB (16K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 11x12b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 16-UQFN Exposed Pad |
| Supplier Device Package | 16-UQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f18426-i-jq |

### 7.8.2 INDF1

**Name:** INDF1
**Address:** 0x01 + n*0x80 [n=0..63]

Indirect Data Register. This is a virtual register. The GPR/SFR register addressed by the FSR1 register is the target for all operations involving the INDF1 register.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | INDF1[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7:0 – INDF1[7:0]**
Indirect data pointed to by the FSR1 register
**Related Links**
Core Registers

## 8.14 Register Summary - BOR Control and Power Control

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0811 | BORCON | 7:0 | SBOREN | | | | | | | BORRDY |
| 0x0812 | Reserved | | | | | | | | | |
| 0x0813 | PCON0 | 7:0 | STKOVF | STKUNF | $\overline{\text{WDTWV}}$ | $\overline{\text{RWDT}}$ | $\overline{\text{RMCLR}}$ | $\overline{\text{RI}}$ | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ |
| 0x0814 | PCON1 | 7:0 | | | | | | | $\overline{\text{MEMV}}$ | |

## 8.15 Register Definitions: Power Control

```
loaded in ADDRH:ADDRL
   ; 4. ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)
   ; 5. NVM interrupts are not taken into account

     BANKSEL    NVMADRH
     MOVF       ADDRH,W
     MOVWF      NVMADRH          ; Load initial address
     MOVF       ADDRL,W
     MOVWF      NVMADRL
     MOVLW      LOW DATA_ADDR    ; Load initial data address
     MOVWF      FSR0L
     MOVLW      HIGH DATA_ADDR
     MOVWF      FSR0H
     BCF        NVMCON1,NVMREGS  ; Set Program Flash Memory as write location
     BSF        NVMCON1,WREN     ; Enable writes
     BSF        NVMCON1,LWLO     ; Load only write latches

   LOOP

     MOVIW      FSR0++
     MOVWF      NVMDATL          ; Load first data byte
     MOVIW      FSR0++
     MOVWF      NVMDATH          ; Load second data byte

     MOVF       NVMADRL,W
     XORLW      0x1F             ; Check if lower bits of address are 00000
     ANDLW      0x1F             ; and if on last of 32 addresses
     BTFSC      STATUS,Z         ; Last of 32 words?
     GOTO       START_WRITE      ; If so, go write latches into memory

     CALL       UNLOCK_SEQ       ; If not, go load latch
     INCF       NVMADRL,F        ; Increment address
     GOTO       LOOP

   START_WRITE

     BCF        NVMCON1,LWLO     ; Latch writes complete, now write memory
     CALL       UNLOCK_SEQ       ; Perform required unlock sequence
     BCF        NVMCON1,WREN     ; Disable writes

   UNLOCK_SEQ

     MOVLW      55h
     BCF        INTCON,GIE       ; Disable interrupts
     MOVWF      NVMCON2          ; Begin unlock sequence
     MOVLW      AAh
     MOVWF      NVMCON2
     BSF        NVMCON1,WR
     BSF        INTCON,GIE       ; Unlock sequence complete, re-enable
interrupts
     return
```

### 13.4.6 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

1. Load the starting address of the row to be modified.
2. Read the existing data from the row into a RAM image.
3. Modify the RAM image to contain the new data to be written into program memory.
4. Load the starting address of the row to be rewritten.
5. Erase the program memory row.
6. Load the write latches with data from the RAM image.
7. Initiate a programming operation.

### 14.6.18 ODCONC

**Name:** ODCONC
**Address:** 0x1F50

Open-Drain Control Register

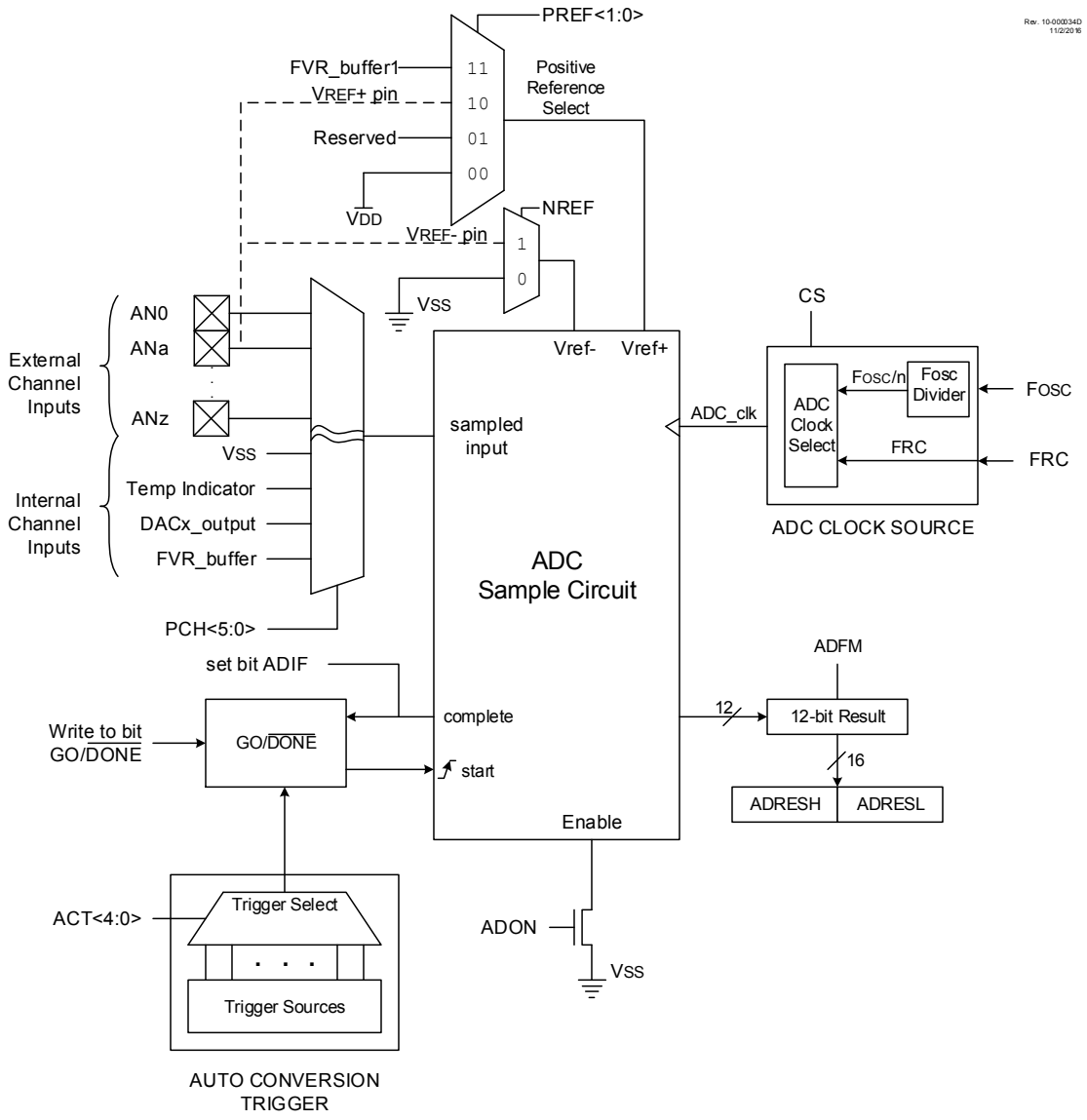
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ODCC7 | ODCC6 | ODCC5 | ODCC4 | ODCC3 | ODCC2 | ODCC1 | ODCC0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 0, 1, 2, 3, 4, 5, 6, 7 – ODCCn** Open-Drain Configuration on RC Pins

| Value | Description |
|---|---|
| 1 | Port pin operates as open-drain drive (sink current only) |
| 0 | Port pin operates as standard push-pull drive (source and sink current) |

**Note:** Bits ODCC6 and ODCC7 available on 20-pin or higher pin-count devices only; Bits unimplemented for lower pin-count devices.

**Figure 20-1. ADC$^2$ Block Diagram**




## 20.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port Configuration
- Channel Selection
- ADC Voltage Reference Selection
- ADC Conversion Clock Source
- Interrupt Control
- Result Formatting
- Conversion Trigger Selection
- ADC Acquisition Time

### 20.8.1 ADCON0

**Name:** ADCON0
**Address:** 0x111

ADC Control Register 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ON | CONT | | CS | | FRM | | GO |
| Access | R/W | R/W | | R/W | | R/W | | R/W/HC |
| Reset | 0 | 0 | | 0 | | 0 | | 0 |

**Bit 7 – ON** ADC Enable bit

| Value | Description |
|---|---|
| 1 | ADC is enabled |
| 0 | ADC is disabled |

**Bit 6 – CONT** ADC Continuous Operation Enable bit

| Value | Description |
|---|---|
| 1 | GO is retriggered upon completion of each conversion trigger until TIF is set (if SOI is set) or until GO is cleared (regardless of the value of SOI) |
| 0 | GO is cleared upon completion of each conversion trigger |

**Bit 4 – CS** ADC Clock Selection bit

| Value | Description |
|---|---|
| 1 | Clock supplied from FRC dedicated oscillator |
| 0 | Clock supplied by $F_{OSC}$, divided according to ADCLK register |

**Bit 2 – FRM** ADC results Format/alignment Selection

| Value | Description |
|---|---|
| 1 | ADRES and ADPREV data are right-justified |
| 0 | ADRES and ADPREV data are left-justified, zero-filled |

**Bit 0 – GO** ADC Conversion Status bit(1,2)

| Value | Description |
|---|---|
| 1 | ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle. The bit is cleared by hardware as determined by the CONT bit |
| 0 | ADC conversion completed/not in progress |

**Note:**

1. This bit requires ON bit to be set.
2. If cleared by software while a conversion is in progress, the results of the conversion up to this point will be transferred to ADRES and the state machine will be reset, but the ADIF interrupt flag bit will not be set; filter and threshold operations will not be performed.

# 22. Numerically Controlled Oscillator (NCO) Module

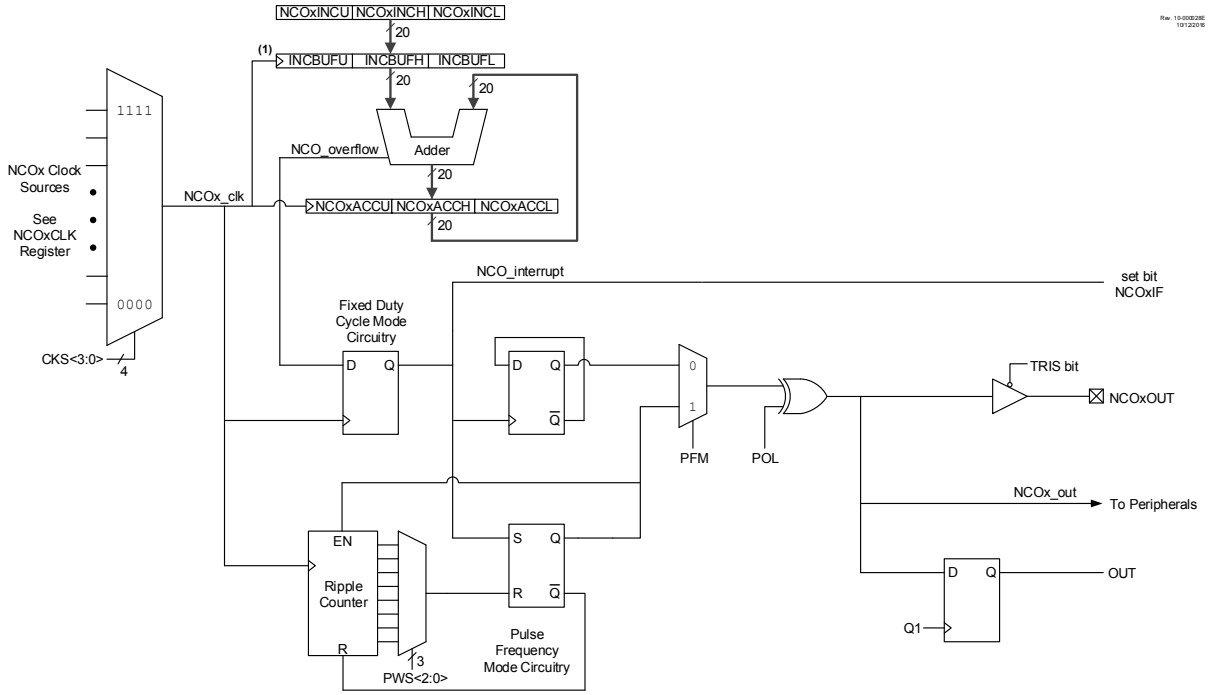
The Numerically Controlled Oscillator (NCO) module is a timer that uses overflow from the addition of an increment value to divide the input frequency. The advantage of the addition method over simple counter driven timer is that the output frequency resolution does not vary with the divider value. The NCO is most useful for application that requires frequency accuracy and fine resolution at a fixed duty cycle.

Features of the NCO include:

- 20-bit Increment Function
- Fixed Duty Cycle mode (FDC) mode
- Pulse Frequency (PF) mode
- Output Pulse Width Control
- Multiple Clock Input Sources
- Output polarity Control
- Interrupt Capability

The following figure is a simplified block diagram of the NCO module.

**Figure 22-1. Numerically Controlled Oscillator Module Simplified Block Diagram**




**Note:**

1. The increment registers are double-buffered to allow for value changes to be made without first disabling the NCO module. The full increment value is loaded into the buffer registers on the second rising edge of the NCOx_clk signal that occurs immediately after a write to NCOxINCL register. The buffers are not user-accessible and are shown here for reference.

## 22.1 NCO Operation

The NCO operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCO output (NCO_overflow). This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See the following equation.

**Equation 22-1. NCO Overflow Frequency**

$$F_{OVERFLOW} = \frac{NCO\ Clock\ Frequency \times Increment\ Value}{2^{20}}$$

### 22.1.1 NCO Clock Sources

Clock sources available to the NCO are shown in the following table:

**Table 22-1. NCO Clock Sources**

| CKS | Clock Source |
|---|---|
| 1111-1011 | Reserved |
| 1010 | CLC4_out |
| 1001 | CLC3_out |
| 1000 | CLC2_out |
| 0111 | CLC1_out |
| 0110 | CLKR |
| 0101 | SOSC |
| 0100 | MFINTOSC (32 kHz) |
| 0011 | MFINTOSC (500 kHz) |
| 0010 | LFINTOSC |
| 0001 | HFINTOSC |
| 0000 | $F_{OSC}$ |

The NCO clock source is selected by configuring the CKS bits.

**Related Links**

NCOxCLK

### 22.1.2 Accumulator

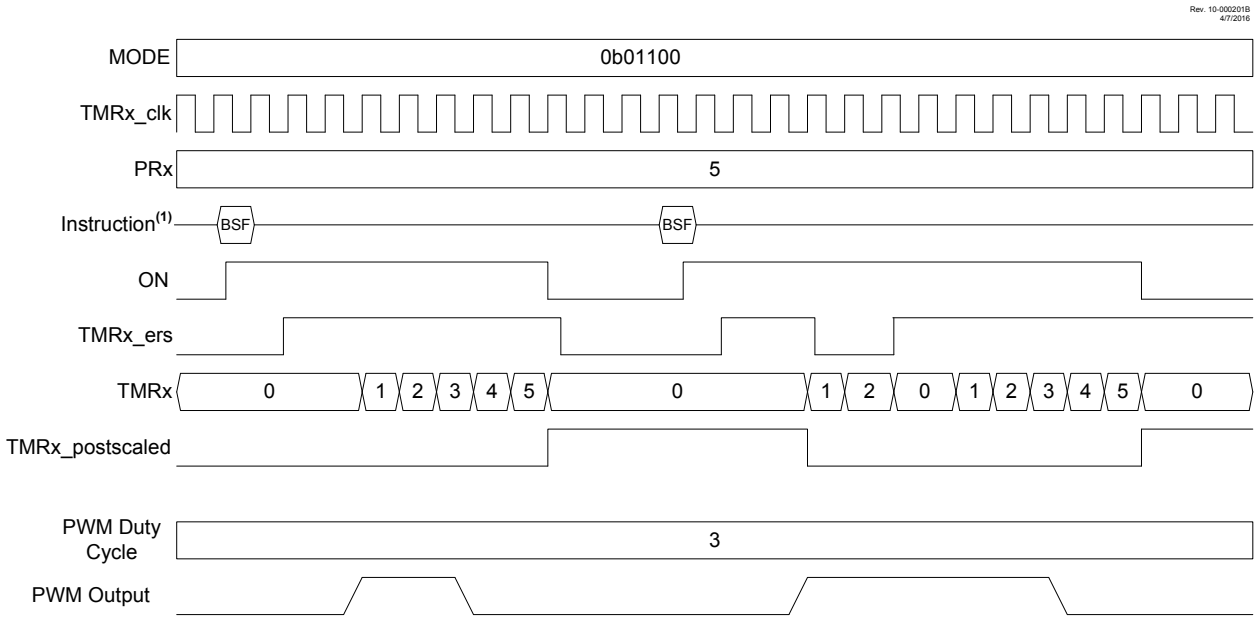
The accumulator is a 20-bit register. Read and write access to the accumulator is available through three registers:

- NCOxACCL
- NCOxACCH
- NCOxACCU

**Related Links**

NCOxACC

**Figure 27-9. Edge-Triggered Hardware Limit One-Shot Mode Timing Diagram (MODE = 01100)**




**Note:**

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

**Related Links**

PWM Overview

(PWM) Pulse-Width Modulation

### 27.6.8 Level Reset, Edge-Triggered Hardware Limit One-Shot Modes

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = 01110)
- High Reset level (MODE<4:0> = 01111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control, a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation, the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

## 31.14 Register Summary - CWG Control

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x060C | CWG1CLK | 7:0 | | | | | | | | CS |
| 0x060D | CWG1ISM | 7:0 | | | | | ISM[3:0] | | | |
| 0x060E | CWG1DBR | 7:0 | | | DBR[5:0] | | | | | |
| 0x060F | CWG1DBF | 7:0 | | | DBF[5:0] | | | | | |
| 0x0610 | CWG1CON0 | 7:0 | EN | LD | | | | MODE[2:0] | | |
| 0x0611 | CWG1CON1 | 7:0 | | | IN | | POLD | POLC | POLB | POLA |
| 0x0612 | CWG1AS0 | 7:0 | SHUTDOWN | REN | LSBD[1:0] | | LSAC[1:0] | | | |
| 0x0613 | CWG1AS1 | 7:0 | | | AS5E | AS4E | AS3E | AS2E | AS1E | AS0E |
| 0x0614 | CWG1STR | 7:0 | OVRD | OVRC | OVRB | OVRA | STRD | STRC | STRB | STRA |
| 0x0615 | Reserved | | | | | | | | | |
| 0x0616 | CWG2CLK | 7:0 | | | | | | | | CS |
| 0x0617 | CWG2ISM | 7:0 | | | | | ISM[3:0] | | | |
| 0x0618 | CWG2DBR | 7:0 | | | DBR[5:0] | | | | | |
| 0x0619 | CWG2DBF | 7:0 | | | DBF[5:0] | | | | | |
| 0x061A | CWG2CON0 | 7:0 | EN | LD | | | | MODE[2:0] | | |
| 0x061B | CWG2CON1 | 7:0 | | | IN | | POLD | POLC | POLB | POLA |
| 0x061C | CWG2AS0 | 7:0 | SHUTDOWN | REN | LSBD[1:0] | | LSAC[1:0] | | | |
| 0x061D | CWG2AS1 | 7:0 | | | AS5E | AS4E | AS3E | AS2E | AS1E | AS0E |
| 0x061E | CWG2STR | 7:0 | OVRD | OVRC | OVRB | OVRA | STRD | STRC | STRB | STRA |

## 31.15 Register Definitions: CWG Control

Long bit name prefixes for the CWG peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

**Table 31-3. CWG Bit Name Prefixes**

| Peripheral | Bit Name Prefix |
|---|---|
| CWG1 | CWG1 |
| CWG2 | CWG2 |

**Related Links**

Long Bit Names

| MDCARH | |
|---|---|
| CHS<3:0> | Connection |
| 1010 | NCO1 OUT |
| 1001 | PWM7 OUT |
| 1000 | PWM6 OUT |
| 0111 | CCP4 OUT |
| 0110 | CCP3 OUT |
| 0101 | CCP2 OUT |
| 0100 | CCP1 OUT |
| 0011 | CLKREF output |
| 0010 | HFINTOSC |
| 0001 | $F_{OSC}$ (system clock) |
| 0000 | Pin selected by MDCARHPPS |

The carrier low signal is selected by configuring the CLS bits.

**Table 32-3. MDCARL Source Selections**

| MDCARL | |
|---|---|
| CLS<3:0> | Connection |
| 1111 | Reserved |
| 1110 | CLC4 OUT |
| 1101 | CLC3 OUT |
| 1100 | CLC2 OUT |
| 1011 | CLC1 OUT |
| 1010 | NCO1 OUT |
| 1001 | PWM7 OUT |
| 1000 | PWM6 OUT |
| 0111 | CCP4 OUT |
| 0110 | CCP3 OUT |
| 0101 | CCP2 OUT |
| 0100 | CCP1 OUT |
| 0011 | CLKREF output |
| 0010 | HFINTOSC |

### 32.12.2 MDxCON1

**Name:** MDxCON1
**Address:** 0x0898

Modulation Control Register 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | CHPOL | CHSYNC | | | CLPOL | CLSYNC |
| Access | | | R/W | R/W | | | R/W | R/W |
| Reset | | | 0 | 0 | | | 0 | 0 |

**Bit 5 – CHPOL** Modulator High Carrier Polarity Select bit

| Value | Description |
|---|---|
| 1 | Selected high carrier signal is inverted |
| 0 | Selected high carrier signal is not inverted |

**Bit 4 – CHSYNC** Modulator High Carrier Synchronization Enable bit

| Value | Description |
|---|---|
| 1 | Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier |
| 0 | Modulator output is not synchronized to the high time carrier signal |

**Bit 1 – CLPOL** Modulator Low Carrier Polarity Select bit

| Value | Description |
|---|---|
| 1 | Selected low carrier signal is inverted |
| 0 | Selected low carrier signal is not inverted |

**Bit 0 – CLSYNC** Modulator Low Carrier Synchronization Enable bit

| Value | Description |
|---|---|
| 1 | Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier |
| 0 | Modulator output is not synchronized to the low time carrier signal |

**Note:**

1. Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

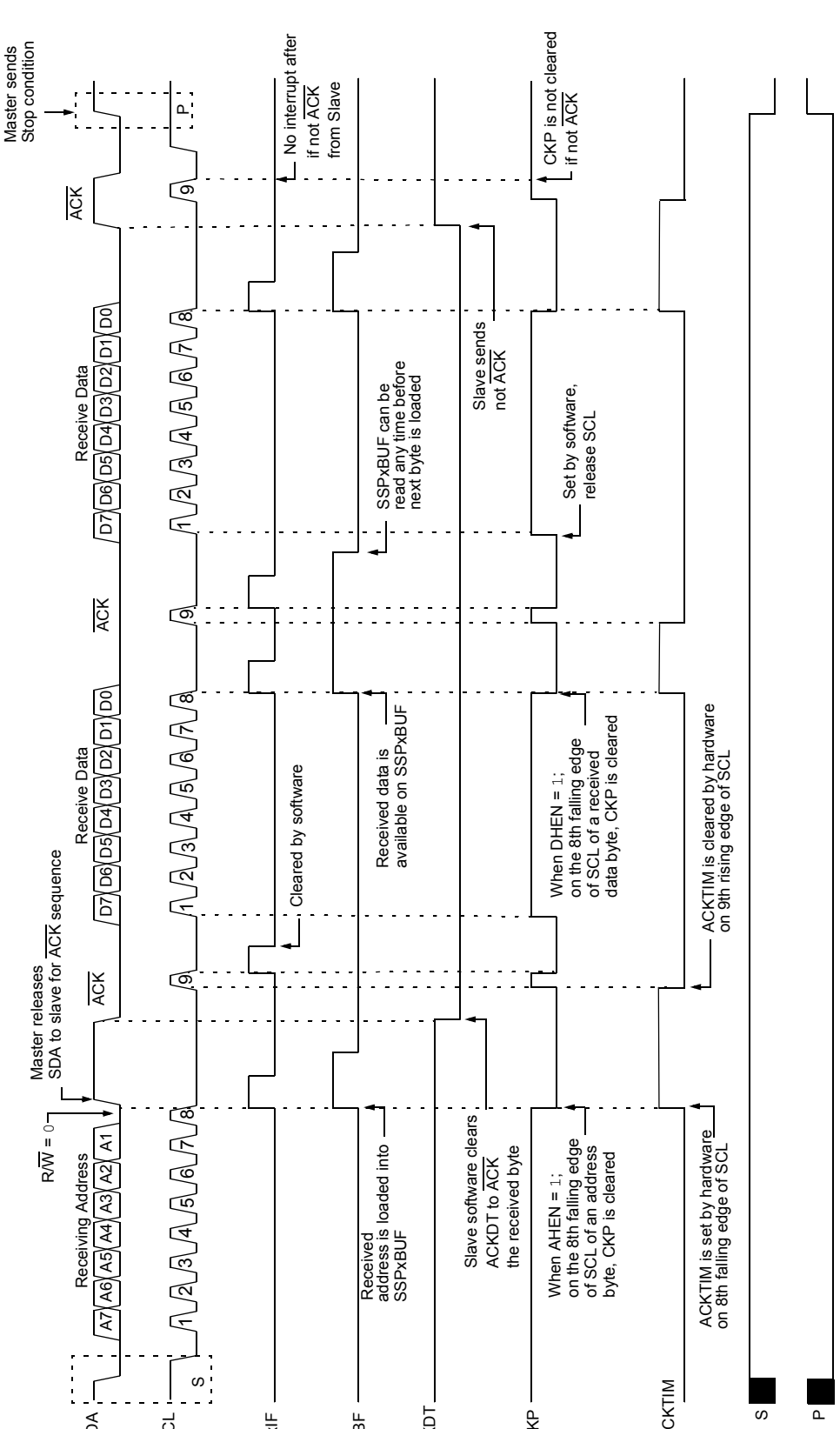



**Figure 35-17. I²C Slave, 7-bit Address, Reception (SEN = 1, AHEN = 1, DHEN = 1)**

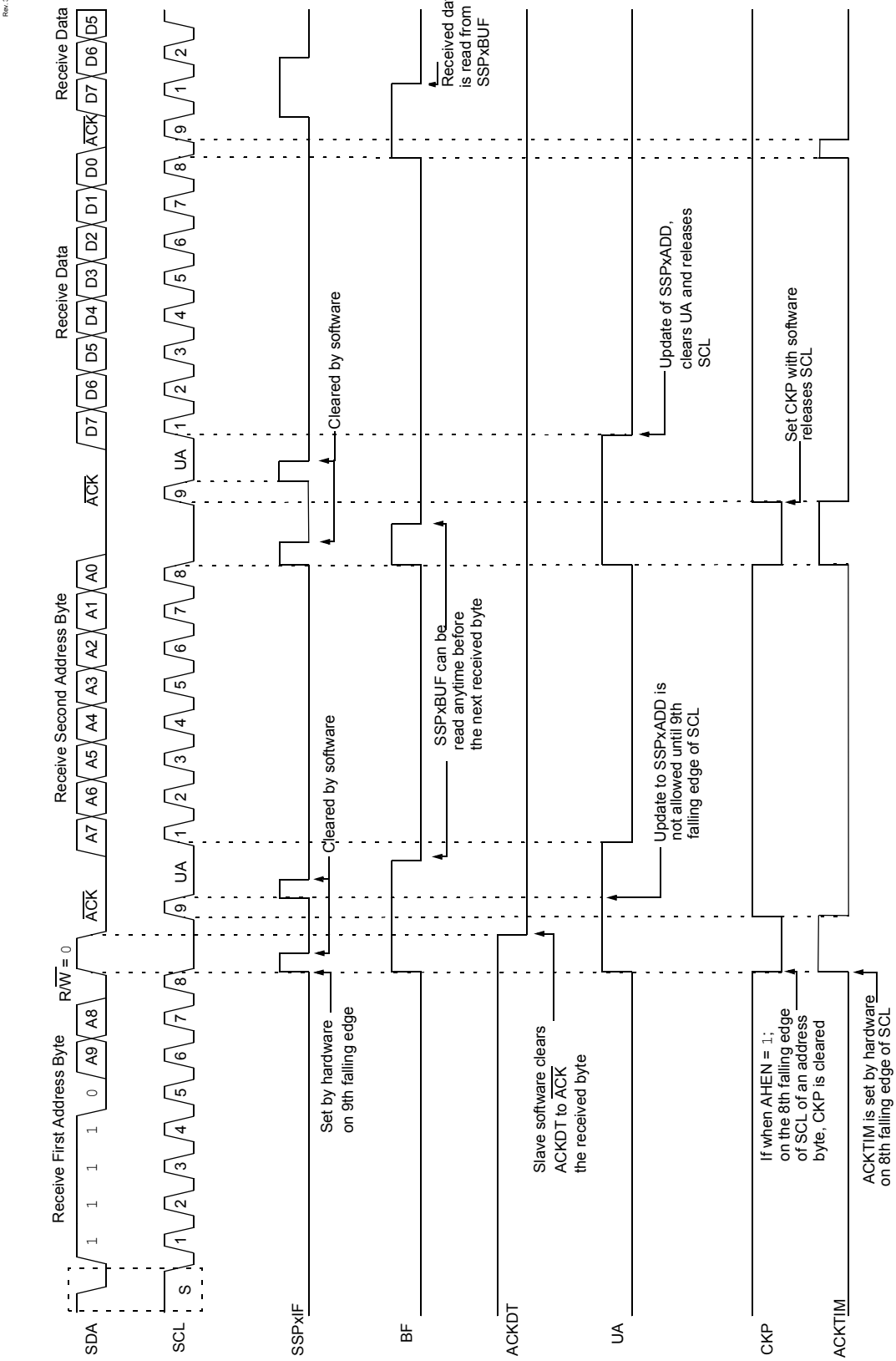


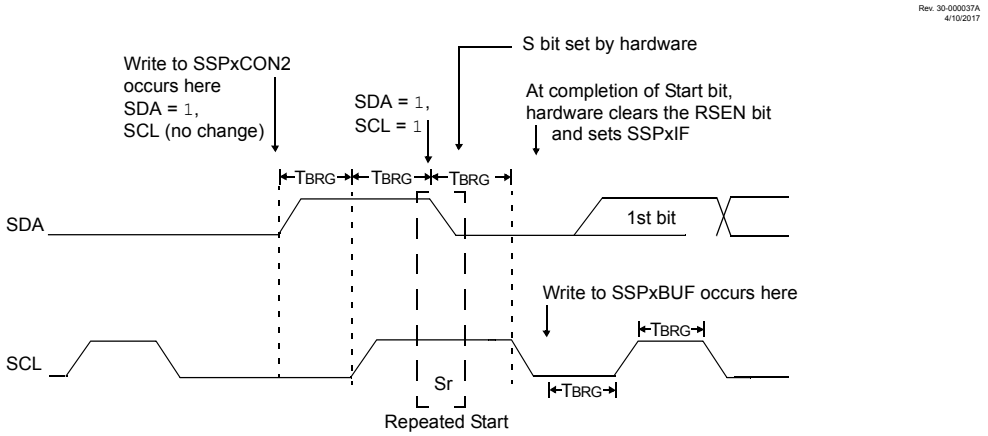

**Figure 35-21. I²C Slave, 10-bit Address, Reception (SEN = 0, AHEN = 1, DHEN = 0)**

the SDA and SCL pins, the S bit will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

**Important:**

1. If RSEN is programmed while any other event is in progress, it will not take effect.
2. A bus collision during the Repeated Start condition occurs if:
   – SDA is sampled low when SCL goes from low-to-high.
   – SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

**Figure 35-27. Repeated Start Condition Waveform**




### 35.6.6 I²C Master Mode Transmission

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count ($T_{BRG}$). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for $T_{BRG}$. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an $\overline{ACK}$ bit during the ninth bit time if an address match occurred, or if data was received properly. The status of $\overline{ACK}$ is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCL low and SDA unchanged (Figure 35-28).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/$\overline{W}$ bit are completed. On the falling edge of the eighth clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the $\overline{ACK}$ bit is loaded into the ACKSTAT Status bit of the SSPxCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSPxIF is set, the BF flag is cleared and

### 35.9.3 SSPxCON2

**Name:** SSPxCON2
**Address:** 0x191,0x19B

Control Register for I²C Operation Only

MSSP Control Register 2

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | GCEN | ACKSTAT | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |
| Access | R/W | R/W/HC | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7 – GCEN**
General Call Enable bit (Slave mode only)

| Value | Mode | Description |
|---|---|---|
| x | Master mode | Don't care |
| 1 | Slave mode | General call is enabled |
| 0 | Slave mode | General call is not enabled |

**Bit 6 – ACKSTAT** Acknowledge Status bit (Master Transmit mode only)

| Value | Description |
|---|---|
| 1 | Acknowledge was not received from slave |
| 0 | Acknowledge was received from slave |

**Bit 5 – ACKDT**
Acknowledge Data bit (Master Receive mode only)**(1)**

| Value | Description |
|---|---|
| 1 | Not Acknowledge |
| 0 | Acknowledge |

**Bit 4 – ACKEN**
Acknowledge Sequence Enable bit**(2)**

| Value | Description |
|---|---|
| 1 | Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; automatically cleared by hardware |
| 0 | Acknowledge sequence is Idle |

**Bit 3 – RCEN**
Receive Enable bit (Master Receive mode only)**(2)**

| Value | Description |
|---|---|
| 1 | Enables Receive mode for I²C |
| 0 | Receive is Idle |

**Bit 2 – PEN**
Stop Condition Enable bit (Master mode only)**(2)**

### 37.3.7 SMTxTMR

**Name:** SMTxTMR
**Address:** 0x048C

SMT Timer Register

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | TMRU[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | TMRH[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TMRL[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 23:16 – TMRU[7:0]** Upper byte of the SMT timer register

**Bits 15:8 – TMRH[7:0]** High byte of the SMT timer register

**Bits 7:0 – TMRL[7:0]** Lower byte of the SMT timer register

| ASRF | Arithmetic Right Shift |
|---|---|
| Status Affected: | C, Z |
| Description: | The contents of register ‘f’ are shifted one bit to the right through the Carry flag.<br>The MSb remains unchanged.<br>If ‘d’ is ‘0’, the result is placed in W.<br>If ‘d’ is ‘1’, the result is stored back in register ‘f’.<br>**Register f → C** |

| BCF | Bit Clear f |
|---|---|
| Syntax: | [ *label* ] BCF f, b |
| Operands: | 0 ≤ f ≤ 127<br>0 ≤ b ≤ 7 |
| Operation: | 0 → f<b> |
| Status Affected: | None |
| Description: | Bit ‘b’ in register ‘f’ is cleared. |

| BRA | Relative Branch |
|---|---|
| Syntax: | [ *label* ] BRA label<br>[ *label* ] BRA $+k |
| Operands: | -256 ≤ label - PC + ≤ 255<br>-256 ≤ k ≤ 255 |
| Operation: | (PC) + 1 + k → PC |
| Status Affected: | None |
| Description: | Add the signed 9-bit literal ‘k’ to the PC.<br>Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + k.<br>This instruction is a 2-cycle instruction. This branch has a limited range. |

| BRW | Relative Branch with W |
|---|---|
| Syntax: | [ *label* ] BRW |
| Operands: | None |
| Operation: | (PC) + (W) → PC |

| PIC16F18426/46 only | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | | |
| **Param. No.** | **Sym.** | **Device Characteristics** | **Min.** | **Typ.†** | **Max.** | **Units** | **Conditions** | |
| | | | | | | | **$V_{DD}$** | **Note** |
| D102 | $I_{DD_{HFOPLL}}$ | HFINTOSC = 32 MHz | — | 3.7 | 5.6 | mA | 3.0V | |
| D103 | $I_{DD_{HSPLL32}}$ | HS+PLL = 32 MHz | — | 3.7 | 5.7 | mA | 3.0V | |
| D104 | $I_{DD_{IDLE}}$ | IDLE mode, HFINTOSC = 16 MHz | — | 1.8 | 2.1 | mA | 3.0V | |
| D105 | $I_{DD_{DOZE}}$ (3) | DOZE mode, HFINTOSC = 16 MHz, Doze Ratio = 16 | — | 1.6 | — | mA | 3.0V | |

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note:**

1. The test conditions for all $I_{DD}$ measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins are outputs driven low; $\overline{MCLR}$ = $V_{DD}$; WDT disabled.
2. The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
3. $I_{DD_{DOZE}}$ = [$I_{DD_{IDLE}}$*(N-1)/N] + $I_{DD_{HFO}}$16/N where N = DOZE Ratio (see *CPUDOZE* register).
4. PMD bits are all in the default state, no modules are disabled.

**Related Links**

CPUDOZE

### 42.3.3 Power-Down Current ($I_{PD}$)(1,2)

**Table 42-3.**

| PIC16LF18426/46 only | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | | | |
| **Param. No.** | **Sym.** | **Device Characteristics** | **Min.** | **Typ.†** | **Max. +85°C** | **Max. +125°C** | **Units** | **Conditions** | |
| | | | | | | | | **$V_{DD}$** | **Note** |
| D200 | $I_{PD}$ | $I_{PD}$ Base | — | 0.06 | 2 | 9 | µA | 3.0V | |
| D201 | $I_{PD\_WDT}$ | Low-Frequency Internal Oscillator/WDT | — | 0.8 | 4.0 | 11 | µA | 3.0V | |

| PIC16LF18426/46 only | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | | | |
| **Param. No.** | **Sym.** | **Device Characteristics** | **Min.** | **Typ.†** | **Max. +85°C** | **Max. +125°C** | **Units** | **Conditions** | |
| | | | | | | | | **$V_{DD}$** | **Note** |
| D202 | $I_{PD\_SOSC}$ | Secondary Oscillator ($S_{OSC}$) | — | 0.6 | 5 | 11 | µA | 3.0V | |
| D203 | $I_{PD\_FVR}$ | FVR | — | 33 | 74 | 76 | µA | 3.0V | |
| D204 | $I_{PD\_BOR}$ | Brown-out Reset (BOR) | — | 10 | 17 | 19 | µA | 3.0V | |
| D205 | $I_{PD\_LPBOR}$ | Low-Power Brown-out Reset (LPBOR) | — | 0.5 | 3.0 | 10 | µA | 3.0V | |
| D207 | $I_{PD\_ADCA}$ | ADC - Non-converting | — | 0.06 | 2 | 9 | µA | 3.0V | ADC not converting (4) |
| D208 | $I_{PD\_CMP}$ | Comparator | — | 30 | 48 | 56 | µA | 3.0V | |

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note:**

1. The peripheral current is the sum of the base $I_{DD}$ and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base $I_{DD}$ or $I_{PD}$current from this limit. Max. values should be used when calculating total current consumption.
2. The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to $V_{SS}$.
3. All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.
4. ADC clock source is FRC.

| PIC16F18426/46 only | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Standard Operating Conditions (unless otherwise stated), VREGPM = 1** | | | | | | | | | |
| **Param. No.** | **Sym.** | **Device Characteristics** | **Min.** | **Typ.†** | **Max. +85°C** | **Max. +125°C** | **Units** | **Conditions** | |
| | | | | | | | | **$V_{DD}$** | **Note** |
| D200 | $I_{PD}$ | $I_{PD}$ Base | — | 0.4 | 4 | 12 | µA | 3.0V | |
| D200A | | | — | 18 | 22 | 27 | µA | 3.0V | VREGPM = 0 |
| D201 | $I_{PD\_WDT}$ | Low-Frequency Internal Oscillator/WDT | — | 0.9 | 6 | 14 | µA | 3.0V | |