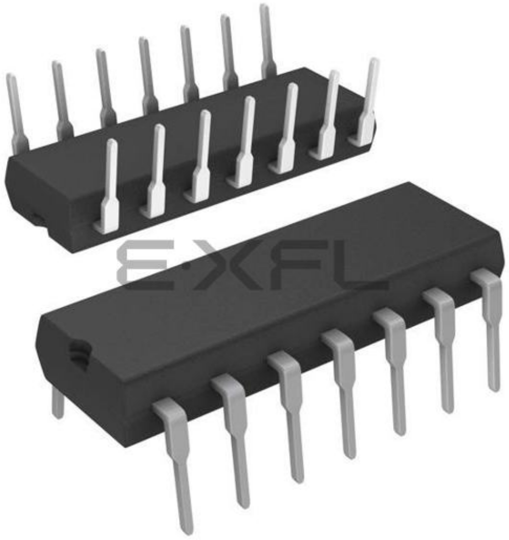
Microchip Technology - PIC16F18426-I/P Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18426-i-p

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1kΩ to 10 kΩ resistor to V_{SS} on unused pins to drive the output to logic low.

5.3 Analog-to-Digital Conversion Data of the Temperature Sensor

The purpose of the temperature indicator module is to provide a temperature-dependent voltage that can be measured by an analog module. The *"Temperature Indicator Module"* chapter explains the operation of the Temperature Indicator module and defines terms such as the low range and high range settings of the sensor. The DIA table contains the internal ADC measurement values of the temperature sensor for low and high range at fixed points of reference. The values are measured during test and are unique to each device. The right-justified ADC readings are stored in the DIA memory region. The calibration data can be used to plot the approximate sensor output voltage, V_{TSENSE} vs. Temperature curve.

- TSLR: Address 8112h to 8114h store the measurements for the low range setting of the temperature sensor at V_{DD} = 3V.
- TSHR: Address 8115h to 8117h store the measurements for the high range setting of the temperature sensor at V_{DD} = 3V.

The stored measurements are made by the device ADC using the internal V_{REF} = 2.048V.

Related Links

Temperature Indicator Module

5.4 Fixed Voltage Reference Data

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of V_{DD}, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- ADC positive reference
- Comparator positive input
- Digital-to-Analog Converter

For more information on the FVR, refer to the *"Fixed Voltage Reference (FVR)"* chapter (see related links).

The DIA stores measured FVR voltages for this device in mV for the different buffer settings of 1x, 2x or 4x at program memory locations 8118h to 811Dh.

- FVRA1X stores the value of ADC FVR1 Output voltage for 1x setting (in mV)
- FVRA2X stores the value of ADC FVR1 Output Voltage for 2x setting (in mV)
- FVRA4X stores the value of ADC FVR1 Output Voltage for 4x setting (in mV)
- FVRC1X stores the value of Comparator FVR2 output voltage for 1x setting (in mV)
- FVRC2X stores the value of Comparator FVR2 output voltage for 2x setting (in mV)
- FVRC4X stores the value of Comparator FVR2 output voltage for 4x setting (in mV)

Related Links

(FVR) Fixed Voltage Reference

CONFIG4

7.2.1 Application Block

Default settings of the Configuration bits ($\overline{\text{BBEN}}$ = 1 and $\overline{\text{SAFEN}}$ = 1) assign all memory in the user Flash area to the Application Block.

7.2.2 Boot Block

If $\overline{\text{BBEN}}$ = 1, the Boot Block is enabled and a specific address range is allotted as the Boot Block based on the value of the BBSIZE bits and the sizes provided in Configuration Word 4.

Related Links

CONFIG4

7.2.3 Storage Area Flash

Storage Area Flash (SAF) is enabled by clearing the $\overline{\text{SAFEN}}$ bit of the Configuration Word. If enabled, the SAF block is placed at the end of memory and spans 128 words. If the Storage Area Flash (SAF) is enabled, the SAF area is not available for program execution.

Related Links

CONFIG4

7.2.4 Memory Write Protection

All the memory blocks have corresponding write protection fuses $\overline{\text{WRTAPP}}$, $\overline{\text{WRTB}}$ and $\overline{\text{WRTC}}$ bits in the Configuration Word 4. If write-protected locations are written from NVMCON registers, memory is not changed and the WRERR bit defined in NVMCON1 register is set as explained in the *“WRERR Bit”* section.

Related Links

CONFIG4
NVMCON1
WRERR Bit

7.2.5 Memory Violation

A Memory Execution Violation Reset occurs while executing an instruction that has been fetched from outside a valid execution area, clearing the $\overline{\text{MEMV}}$ bit. Refer to the *“Memory Execution Violation”* section for the available valid program execution areas and the PCON1 register definition for $\overline{\text{MEMV}}$ bit conditions.

Table 7-2. Memory Access Partition

REG	Address	Partition			
		$\overline{\text{BBEN}}$ = 1 $\overline{\text{SAFEN}}$ = 1	$\overline{\text{BBEN}}$ = 1 $\overline{\text{SAFEN}}$ = 0	$\overline{\text{BBEN}}$ = 0 $\overline{\text{SAFEN}}$ = 1	$\overline{\text{BBEN}}$ = 0 $\overline{\text{SAFEN}}$ = 0
PFM	00 0000h ... Last Block	APPLICATION BLOCK[(4)]	APPLICATION BLOCK[(4)]	BOOT BLOCK[(4)]	BOOT BLOCK[(4)]

10.7.17 PIR6

Name: PIR6
Address: 0x712

PIR6 Peripheral Interrupt Request (Flag) Register 6

Bit	7	6	5	4	3	2	1	0
					CCP4IF	CCP3IF	CCP2IF	CCP1IF
Access					R/W/HS	R/W/HS	R/W/HS	R/W/HS
Reset					0	0	0	0

Bit 3 – CCP4IF CCP4 Interrupt Flag bit

Value	Condition	Description
1	Capture mode	Capture occurred (must be cleared in software)
0	Capture mode	Capture did not occur
1	Compare mode	Compare match occurred (must be cleared in software)
0	Compare mode	Compare match did not occur
1	PWM mode	Output trailing edge occurred (must be cleared in software)
0	PWM mode	Output trailing edge did not occur

Bit 2 – CCP3IF CCP3 Interrupt Flag bit

Value	Condition	Description
1	Capture mode	Capture occurred (must be cleared in software)
0	Capture mode	Capture did not occur
1	Compare mode	Compare match occurred (must be cleared in software)
0	Compare mode	Compare match did not occur
1	PWM mode	Output trailing edge occurred (must be cleared in software)
0	PWM mode	Output trailing edge did not occur

Bit 1 – CCP2IF CCP2 Interrupt Flag bit

Value	Condition	Description
1	Capture mode	Capture occurred (must be cleared in software)
0	Capture mode	Capture did not occur
1	Compare mode	Compare match occurred (must be cleared in software)
0	Compare mode	Compare match did not occur
1	PWM mode	Output trailing edge occurred (must be cleared in software)
0	PWM mode	Output trailing edge did not occur

Bit 0 – CCP1IF CCP1 Interrupt Flag bit

Value	Condition	Description
1	Capture mode	Capture occurred (must be cleared in software)
0	Capture mode	Capture did not occur
1	Compare mode	Compare match occurred (must be cleared in software)
0	Compare mode	Compare match did not occur

Table 11-1. Interrupts During DOZE

DOZEN	ROI	Code Flow			
		Main	ISR(1)	Return to Main	
0	0	Normal Operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)	If DOE = 1 when return from interrupt: DOZE operation and DOZEN = 1 (in hardware)	If DOE = 0 when return from interrupt: Normal operation and DOZEN = 0 (in hardware)
0	1	Normal Operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)		
1	0	DOZE operation	DOZE operation and DOE = DOZEN (in hardware) DOZEN = 1 (unchanged)		
1	1	DOZE operation	Normal operation and DOE = DOZEN (in hardware) DOZEN = 0 (unchanged)		

Note:

1. User software can change DOE bit in the ISR.

11.2 Sleep Mode

Sleep mode is entered by executing the `SLEEP` instruction, while the Idle Enable (IDLEN) bit of the CPUDOZE register is clear (IDLEN = 0).

Upon entering Sleep mode, the following conditions exist:

1. WDT will be cleared but keeps running if enabled for operation during Sleep
2. The $\overline{\text{PD}}$ bit of the STATUS register is cleared
3. The $\overline{\text{TO}}$ bit of the STATUS register is set
4. The CPU clock is disabled
5. LFINTOSC, SOSC, HFINTOSC and ADCRC are unaffected and peripherals using them may continue operation in Sleep.
6. I/O ports maintain the status they had before Sleep was executed (driving high, low, or high-impedance)
7. Resets other than WDT are not affected by Sleep mode

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins

13.3.1 FSR Read

With the intended address loaded into an FSR register a `MOVIW` instruction or read of INDF will read data from the program memory or EEPROM.

Reading from NVM requires one instruction cycle. The CPU operation is suspended during the read, and resumes immediately after. Read operations return a single byte of memory.

13.3.2 FSR Write

Writing/erasing the NVM through the FSR registers (ex. `MOVWI` instruction) is not supported in the PIC16(L)F184XX devices.

13.4 NVMREG Access

The NVMREG interface allows read/write access to all the locations accessible by FSRs, and also read/write access to the User ID locations and EEPROM, and read-only access to the device identification, revision, and Configuration data.

Writing or erasing of NVM via the NVMREG interface is prevented when the device is write-protected.

13.4.1 NVMREG Read Operation

To read a NVM location using the NVMREG interface, the user must:

1. Clear the NVMREGS bit of the NVMCON1 register if the user intends to access program memory locations, or set NMVREGS if the user intends to access User ID, EEPROM, or Configuration locations.
2. Write the desired address into the NVMADRH:NVMADRL register pair.
3. Set the RD bit of the NVMCON1 register to initiate the read.

Once the read control bit is set, the CPU operation is suspended during the read, and resumes immediately after. The data is available in the very next cycle, in the NVMDATH:NVMDATL register pair; therefore, it can be read as two bytes in the following instructions.

NVMDATH:NVMDATL register pair will hold this value until another read or until it is written to by the user.

Upon completion, the RD bit is cleared by hardware.

20. (ADC^2) Analog-to-Digital Converter with Computation Module

The Analog-to-Digital Converter with Computation (ADC^2) allows conversion of an analog input signal to a 12-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 12-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair).

Additionally, the following features are provided within the ADC module:

- 13-bit Acquisition Timer
- Hardware Capacitive Voltage Divider (CVD) support:
  - 13-bit precharge timer
  - Adjustable sample and hold capacitor array
  - Guard ring digital output drive
- Automatic repeat and sequencing:
  - Automated double sample conversion for CVD
  - Two sets of result registers (Result and Previous result)
  - Auto-conversion trigger
  - Internal retrigger
- Computation features:
  - Averaging and low-pass filter functions
  - Reference comparison
  - 2-level threshold comparison
  - Selectable interrupts

The figure below shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion and upon threshold comparison. These interrupts can be used to wake-up the device from Sleep.

20.8.1 ADCON0

Name: ADCON0
Address: 0x111

ADC Control Register 0

Bit	7	6	5	4	3	2	1	0
	ON	CONT		CS		FRM		GO
Access	R/W	R/W		R/W		R/W		R/W/HC
Reset	0	0		0		0		0

Bit 7 – ON ADC Enable bit

Value	Description
1	ADC is enabled
0	ADC is disabled

Bit 6 – CONT ADC Continuous Operation Enable bit

Value	Description
1	GO is retriggered upon completion of each conversion trigger until TIF is set (if SOI is set) or until GO is cleared (regardless of the value of SOI)
0	GO is cleared upon completion of each conversion trigger

Bit 4 – CS ADC Clock Selection bit

Value	Description
1	Clock supplied from FRC dedicated oscillator
0	Clock supplied by F_{OSC}, divided according to ADCLK register

Bit 2 – FRM ADC results Format/alignment Selection

Value	Description
1	ADRES and ADPREV data are right-justified
0	ADRES and ADPREV data are left-justified, zero-filled

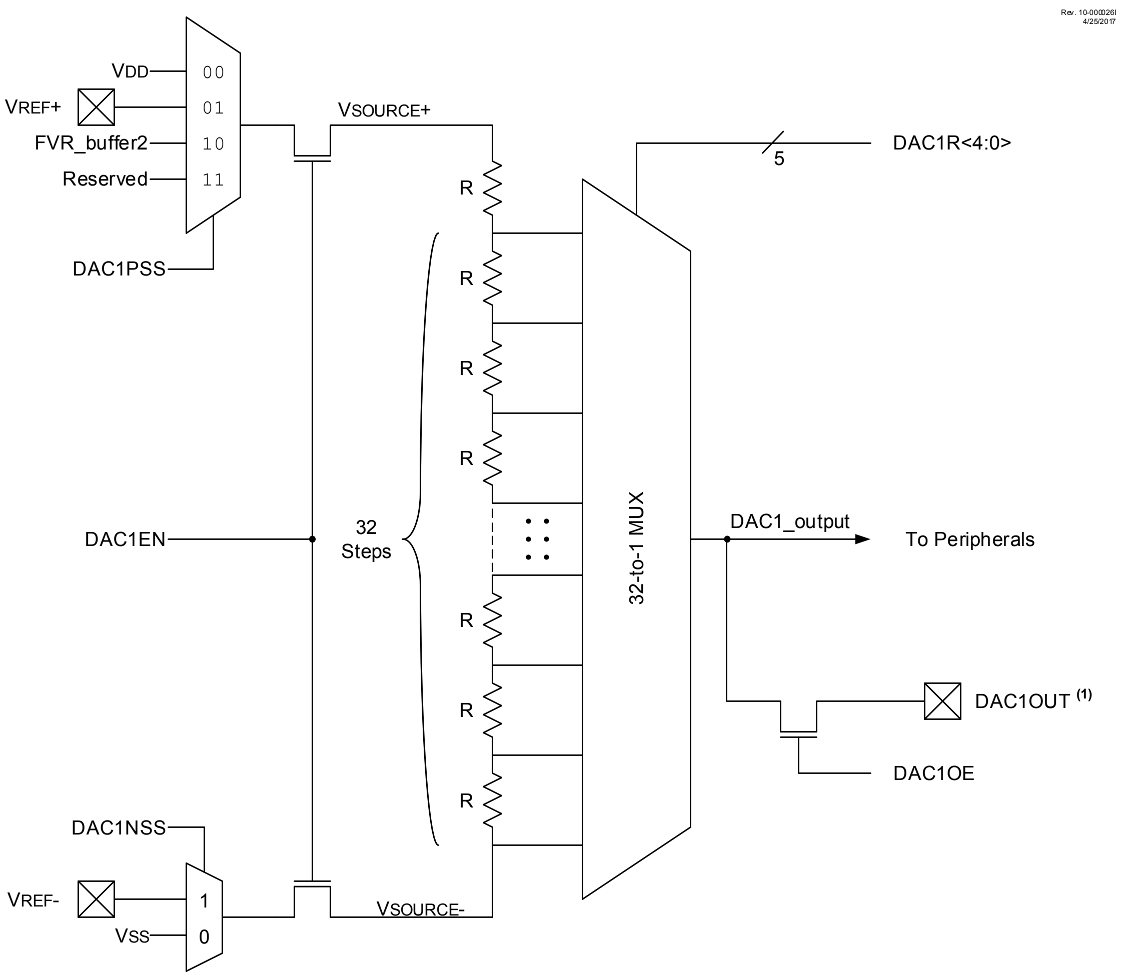
Bit 0 – GO ADC Conversion Status bit[1,2]

Value	Description
1	ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle. The bit is cleared by hardware as determined by the CONT bit
0	ADC conversion completed/not in progress

Note:

1. This bit requires ON bit to be set.
2. If cleared by software while a conversion is in progress, the results of the conversion up to this point will be transferred to ADRES and the state machine will be reset, but the ADIF interrupt flag bit will not be set; filter and threshold operations will not be performed.

Figure 21-1. Digital-to-Analog Converter Block Diagram



Note:

1. The unbuffered DACx_output is provided on the DACxOUT pin(s).

21.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DAC1R bits.

The DAC output voltage can be determined by using the following equation.

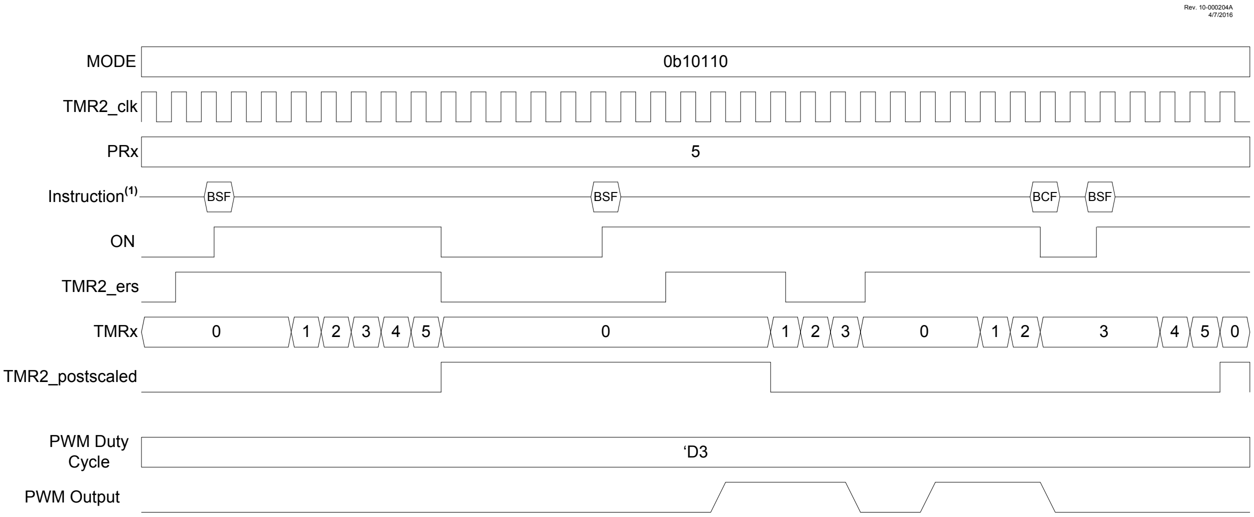
Equation 21-1. DAC Output Voltage

When EN = 1:

$$DACx\_output = \left(\left(V_{REF+} - V_{REF-}\right) x \frac{DACR[4:0]}{2^5}\right) + V_{REF-}$$

Note: See the DAC1CON0 register for the available V_{SOURCE}+ and V_{SOURCE}- selections.

Figure 27-12. Level-Triggered hardware Limit one-Shot Mode Timing Diagram (MODE = `10110`)



Note:

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

Related Links

PWM Overview

(PWM) Pulse-Width Modulation

27.7 Timer2 Operation During Sleep

When PSYNC = `1`, Timer2 cannot be operated while the processor is in Sleep mode. The contents of the T2TMR and T2PR registers will remain unchanged while processor is in Sleep mode.

When PSYNC = `0`, Timer2 will operate in Sleep as long as the clock source selected is also still running. If any internal oscillator is selected as the clock source, it will stay active during Sleep mode.

31.15.8 CWGxDBR

Name: CWGxDBR
Address: 0x60E,0x618

CWG Rising Dead-Band Count Register

Bit	7	6	5	4	3	2	1	0
			DBR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 5:0 – DBR[5:0] CWG Rising Edge Triggered Dead-Band Count bits
Reset States: POR/BOR = xxxxxx
All Other Resets = uuuuuu

Value	Description
n	Dead band is active no less than n, and no more than n+1, CWG clock periods after the rising edge
0	0 CWG clock periods. Dead-band generation is bypassed

MDCARL	
CLS<3:0>	Connection
0001	F_{OSC} (system clock)
0000	Pin selected by MDCARLPPS

32.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When synchronization is enabled, the carrier pulse that is being mixed at the time of the transition is allowed to transition low before the DSM switches over to the next carrier source.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the CHSYNC bit. Synchronization for the carrier low signal is enabled by setting the CLSYNC bit.

The figures below show the timing diagrams of using various synchronization methods.

Figure 32-2. On Off Keying (OOK) Synchronization

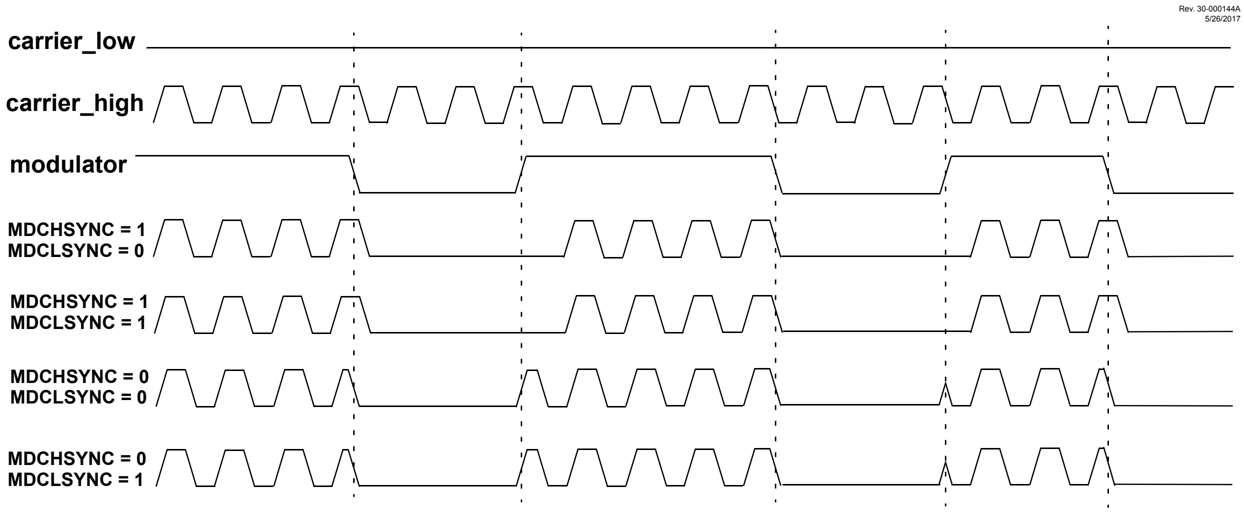
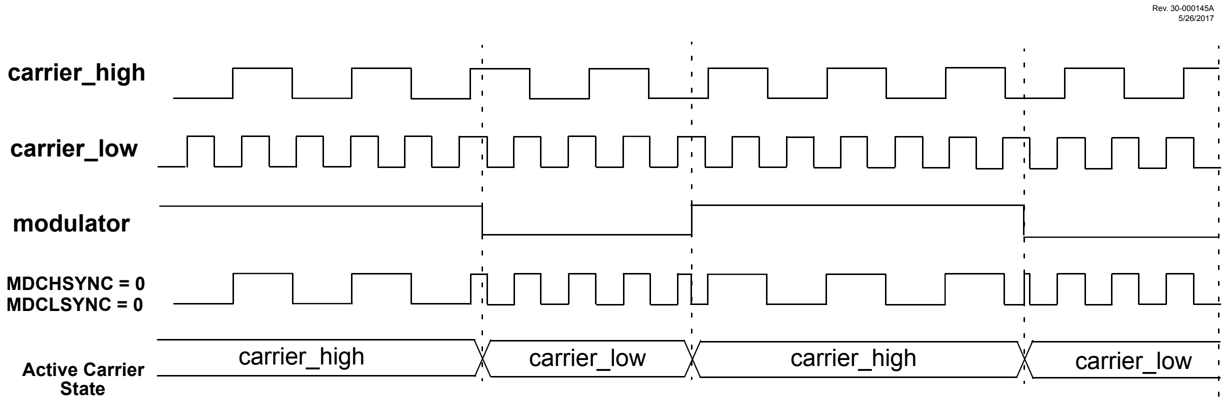


Figure 32-3. No Synchronization (MDCHSYNC = 0, MDCLSYNC = 0)



33. (CLC) Configurable Logic Cell

The Configurable Logic Cell (CLCx) module provides programmable logic that operates outside the speed limitations of software execution. The logic cell takes up to 64 input signals and, through the use of configurable gates, reduces the 64 inputs to four logic lines that drive one of eight selectable single-output logic functions.

Input sources are a combination of the following:

- I/O pins
- Internal clocks
- Peripherals
- Register bits

The output can be directed internally to peripherals and to an output pin.

Important: There are several CLC instances on this device. Throughout this section, the lower case 'x' in register names is a generic reference to the CLC instance number. For example, the first instance of the control register is CLC1CON and is generically described in this chapter as CLCxCON.

The following figure is a simplified diagram showing signal flow through the CLC. Possible configurations include:

- Combinatorial Logic
  - AND
  - NAND
  - AND-OR
  - AND-OR-INVERT
  - OR-XOR
  - OR-XNOR
- Latches
  - S-R
  - Clocked D with Set and Reset
  - Transparent D with Set and Reset

The clock divider values can be changed while the module is enabled. However, in order to prevent glitches on the output, the DIV bits should only be changed when the module is disabled (EN = 0).

34.3 Selectable Duty Cycle

The DC bits are used to modify the duty cycle of the output clock. A duty cycle of 0%, 25%, 50%, or 75% can be selected for all clock rates when the DIV value is not 0b000. When DIV=0b000 then the duty cycle defaults to 50% for all values of DC except 0b00 in which case the duty cycle is 0% (constant low output).

The duty cycle can be changed while the module is enabled. However, in order to prevent glitches on the output, the DC bits should only be changed when the module is disabled (EN = 0).

Important: The DC value at reset is 10. This makes the default duty cycle 50% and not 0%.

34.4 Operation in Sleep Mode

The reference clock module continues to operate and provide a signal output in Sleep for all clock source selections except F_{OSC} (CLK=0).

Figure 35-14. I²C Slave, 7-bit Address, Reception (SEN = 0, AHEN = 0, DHEN = 0)

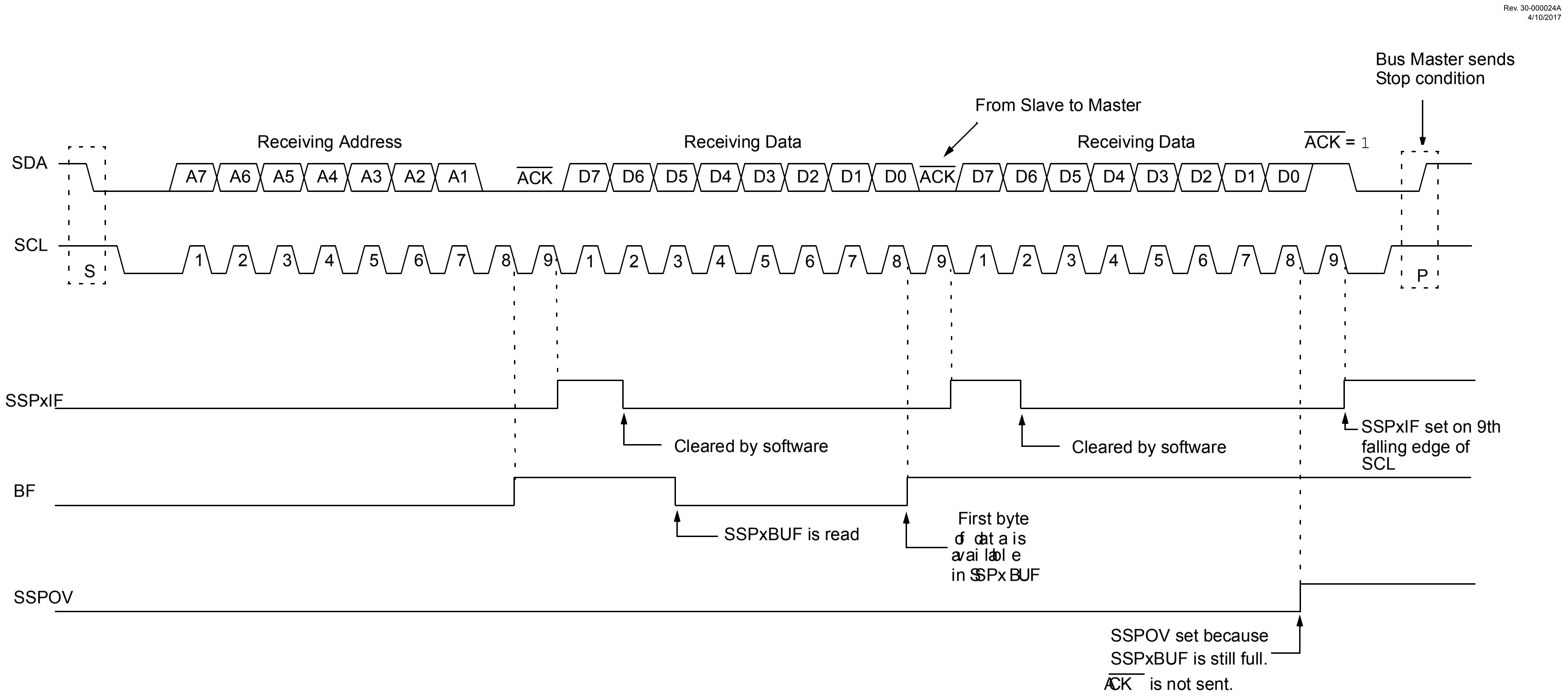
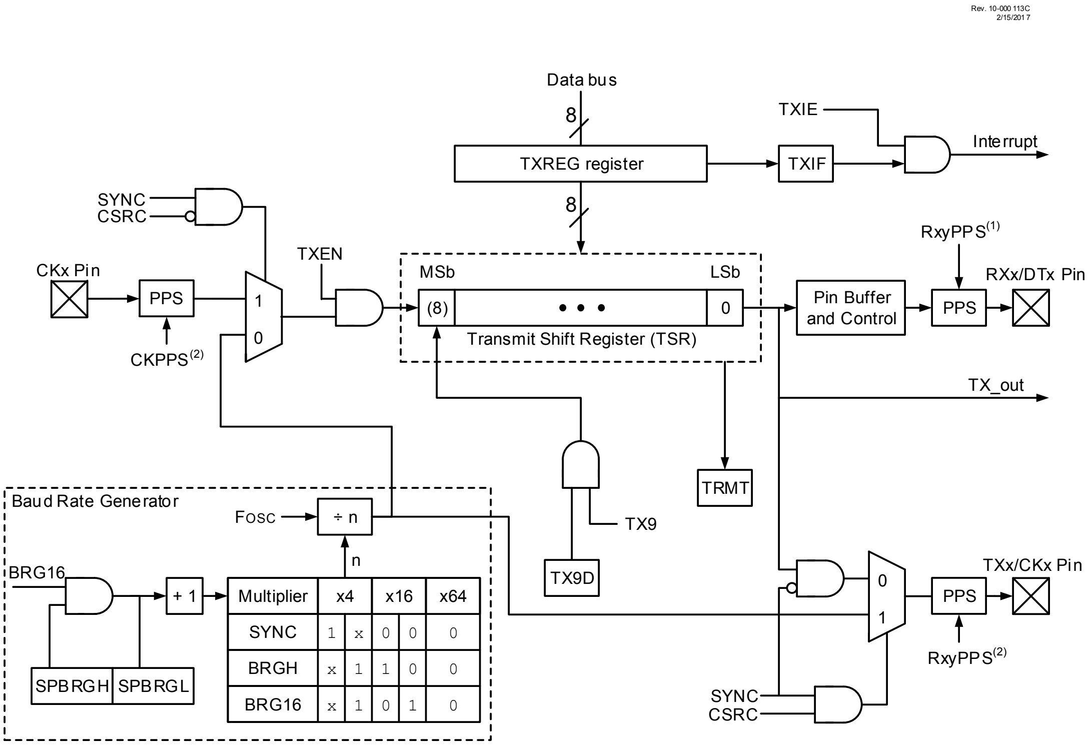


Figure 36-1. EUSART Transmit Block Diagram



Multiplier	x4		x16		x64
SYNC	1	x	0	0	0
BRGH	x	1	1	0	0
BRG16	x	1	0	1	0

Note 1: In Synchronous mode, the DT output and RX input PPS selections should enable the same pin.

2: In Master Synchronous mode the TX output and CK input PPS selections should enable the same pin.

	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	-0.01	4166	300.0	0.00	3839	300.0	0.00	2303
1200	1200	-0.02	3332	1200	-0.03	1041	1200	0.00	959	1200	0.00	575
2400	2401	-0.04	832	2399	-0.03	520	2400	0.00	479	2400	0.00	287
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35
57.6k	57.14k	-0.79	34	56.818	-1.36	21	57.60k	0.00	19	57.60k	0.00	11
115.2k	117.6k	2.12	16	113.636	-1.36	10	115.2k	0.00	9	115.2k	0.00	5

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	—
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	—	—	—
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	—
115.2k	—	—	—	—	—	—	115.2k	0.00	1	—	—	—

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287

Figure 37-9. Windowed Measurement Mode, Repeat Acquisition Timing Diagram

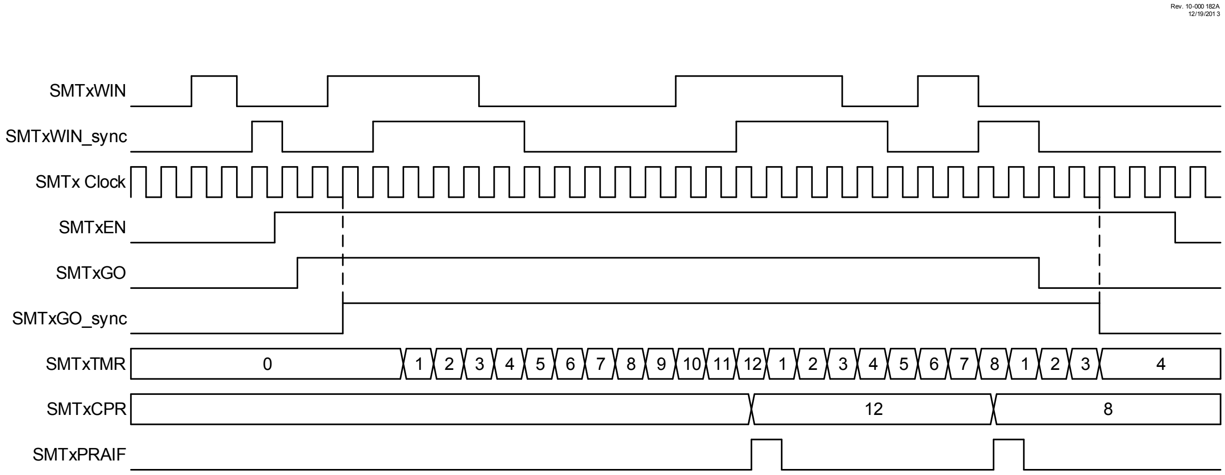
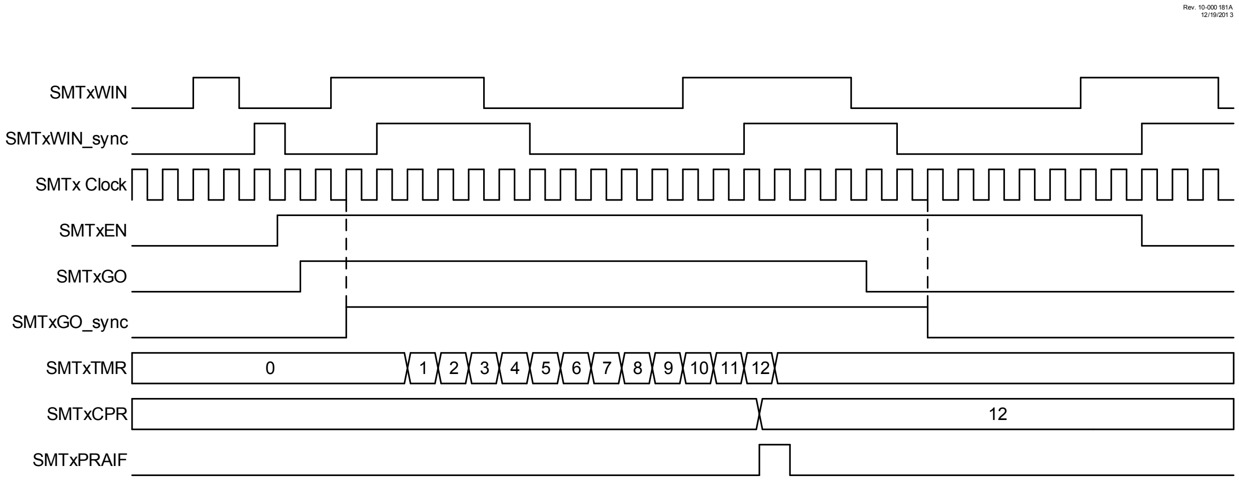


Figure 37-10. Windowed Measurement Mode, Single Acquisition Timing Diagram



37.1.6.6 Gated Window Measurement Mode

This mode measures the duty cycle of the signal input over a known input window. It does so by incrementing the timer on each pulse of the clock signal while the signal input is high, updating the SMTxCPR register and resetting the timer on every rising edge of the window input after the first. See figures below.

Figure 37-15. Capture Mode, Repeat Acquisition Timing Diagram

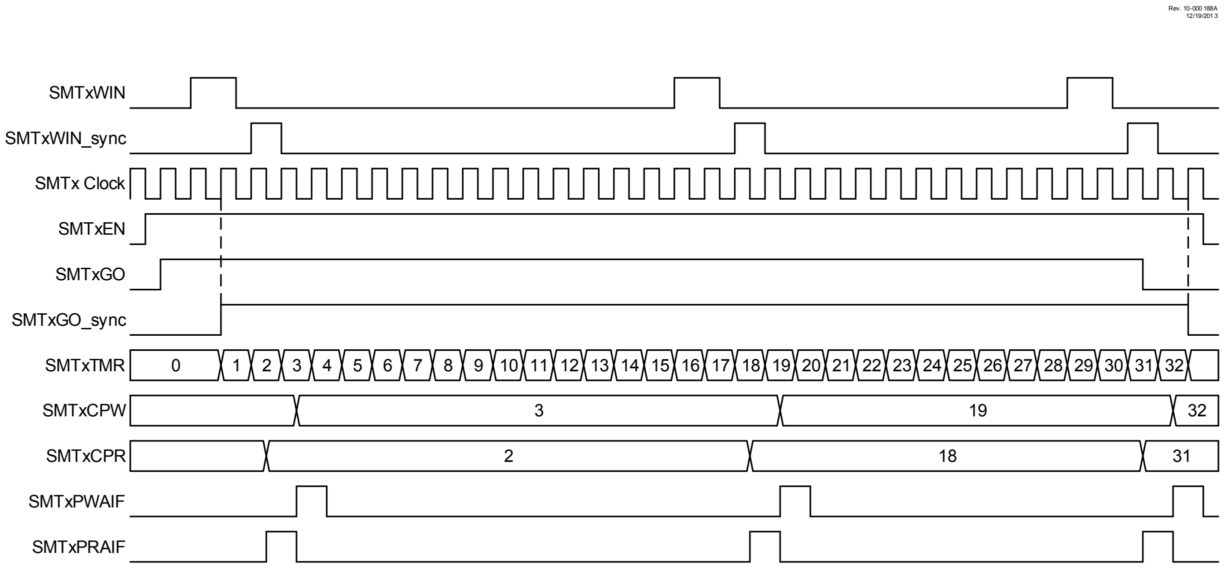
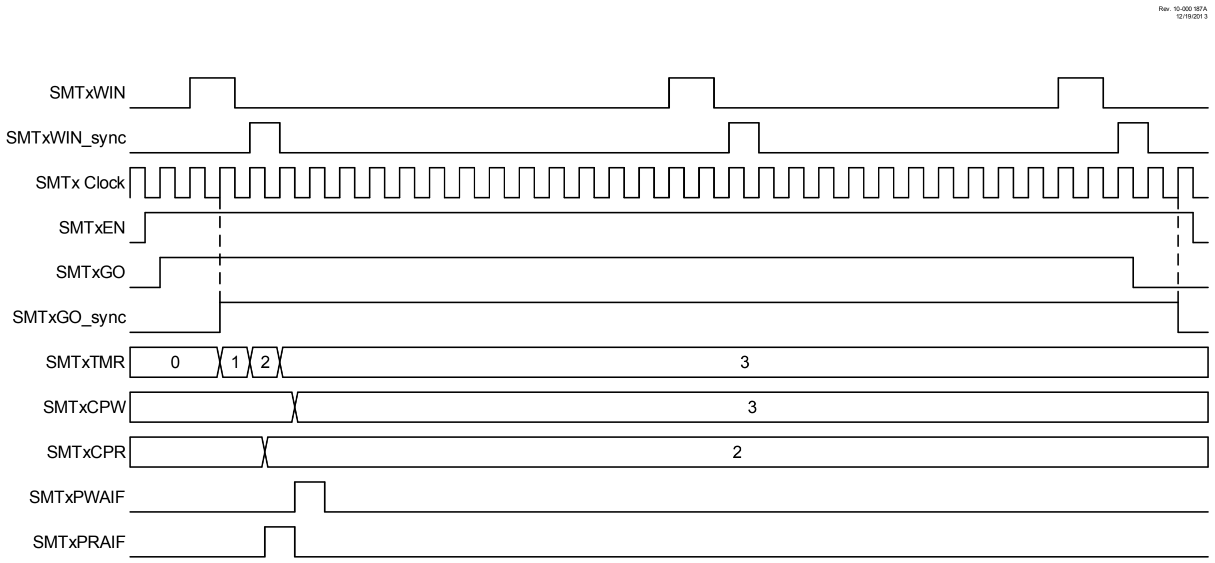


Figure 37-16. Capture Mode, Single Acquisition Timing Diagram



37.1.6.9 Counter Mode

This mode increments the timer on each pulse of the signal input. This mode is asynchronous to the SMT clock and uses the signal input as a time source. The SMTxCPW register will be updated with the current SMTxTMR value on the falling edge of the window input. See figure below.

37.3.3 SMTxSTAT

Name: SMTxSTAT
Address: 0x049A

SMT Status Register

Bit	7	6	5	4	3	2	1	0
	CPRUP	CPWUP		RST		TS	WS	AS
Access	R/W/HC	R/W/HC		R/W		RO	RO	RO
Reset	0	0		0		0	0	0

Bit 7 – CPRUP SMT Manual Period Buffer Update bit

Value	Description
1	Request update to SMTxCPR registers
0	SMTxCPR registers update is complete

Bit 6 – CPWUP SMT Manual Pulse Width Buffer Update bit

Value	Description
1	Request update to SMTxCPW registers
0	SMTxCPW registers update is complete

Bit 4 – RST SMT Manual Timer Reset bit

Value	Description
1	Request Reset to SMTxTMR registers
0	SMTxTMR registers update is complete

Bit 2 – TS SMT GO Value Status bit

Value	Description
1	SMTxTMR is incrementing
0	SMTxTMR is not incrementing

Bit 1 – WS SMT Window Status bit

Value	Description
1	SMT window is open
0	SMT window is closed

Bit 0 – AS SMT Signal Value Status bit

Value	Description
1	SMT acquisition is in progress
0	SMT acquisition is not in progress