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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18426t-i-sl

Features	PIC16(L)F18426	PIC16(L)F18446
Packages	14 - PDIP 14 - SOIC (3.9 mm) 14 - TSSOP 16 - uQFN (4x4)	20 - PDIP 20 - SOIC (7.5 mm) 20 - SSOP 20 - uQFN (4x4)
I/O Ports	A, C	A, B, C
Capture/Compare/PWM Modules (CCP)	4	4
Configurable Logic Cell (CLC)	4	4
10-Bit Pulse-Width Modulator (PWM)	2	2
12-Bit Analog-to-Digital Module (ADC^2) with Computation Accelerator	11 channels	17 channels
5-Bit Digital-to-Analog Module (DAC)	1	1
Comparators	2	2
Numerical Contolled Oscillator (NCO)	1	1
Interrupt Sources	40	40
Timers (16-/8-bit)	4	4
Serial Communications	2 MSSP 1 EUSART	2 MSSP 1 EUSART
Complementary Waveform Generator (CWG)	2	2
Zero-Cross Detect (ZCD)	1	1
Data Signal Modulator (DSM)	1	1
Reference Clock Output Module	1	1
Peripheral Pin Select (PPS)	YES	YES
Peripheral Module Disable (PMD)	YES	YES
Programmable Brown-out Reset (BOR)	YES	YES
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT
Instruction Set	50 instructions	50 instructions

14.6.15 WPUC

Name: WPUC
Address: 0x1F4F

Weak Pull-up Register

Bit	7	6	5	4	3	2	1	0
	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – WPUCn Weak Pull-up PORTC Control bits

Value	Description
1	Weak Pull-up enabled
0	Weak Pull-up disabled

Note: Bits WPUC6 and WPUC7 available on 20-pin or higher pin-count devices only; Bits unimplemented for lower pin-count devices.

19. Temperature Indicator Module

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The main purpose of the temperature indicator module is to provide a temperature-dependent voltage that can be measured by the Analog-to-Digital Converter.

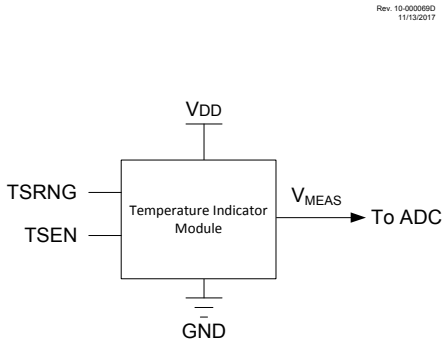
The circuit's range of operating temperature falls between -40°C and +125°C. The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately.

19.1 Module Operation

The temperature indicator module consists of a temperature-sensing circuit that provides a voltage to the device ADC. The analog voltage output, V_{MEAS}, varies inversely to the device temperature. The output of the temperature indicator is referred to as V_{MEAS}.

The following figure shows a simplified block diagram of the temperature indicator module.

Figure 19-1. Temperature Indicator Module Block Diagram



The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to the ADC link below for detailed information.

The ON/OFF bit for the module is located in the FVRCON register. The circuit is enabled by setting the TSEN bit of the FVRCON register. When the module is disabled, the circuit draws no current. Refer to the FVR link below for more information.

The circuit operates in either High or Low range. Refer to the *"Temperature Indicator Range"* for more details on the range settings.

Related Links

(FVR) Fixed Voltage Reference

Temperature Indicator Range

(ADC2) Analog-to-Digital Converter with Computation Module

- The result of the calculation (ADERR) is compared to the upper and lower thresholds, ADUTH<UTHH:UTHL> and ADLTH<LTHH:LTHL> registers, to set the UTHR and LTHR flag bits. The threshold logic is selected by MD bits. The threshold trigger option can be one of the following:
  - Never interrupt
  - Error is less than lower threshold
  - Error is greater than or equal to lower threshold
  - Error is between thresholds (inclusive)
  - Error is outside of thresholds
  - Error is less than or equal to upper threshold
  - Error is greater than upper threshold
  - Always interrupt regardless of threshold test results
  - If the threshold condition is met, the threshold interrupt flag ADTIF is set.

Note:

1. The threshold tests are signed operations.
2. If OV is set, a threshold interrupt is signaled. It is good practice for threshold interrupt handlers to verify the validity of the threshold by checking ADAOV.

Table 20-6. ADC Error Calculation Mode

CALC	Action During 1st Precharge Stage		Application
	DSEN = 0 Single-Sample Mode	DSEN = 1 CVD Double-Sample Mode(1)	
111	Reserved	Reserved	Reserved
110	Reserved	Reserved	Reserved
101	ADLFTR-ADSTPT	ADFLTR-ADSTPT	Average/filtered value vs. setpoint
100	ADPREV-ADFLTR	ADPREV-ADFLTR	First derivative of filtered value(3) (negative)
011	Reserved	Reserved	Reserved
010	ADRES-ADFLTR	(ADRES-ADPREV)-ADFLTR	Actual result vs. averaged/filtered value
001	ADRES-ADSTPT	(ADRES-ADPREV)-ADSTPT	Actual result vs. setpoint
000	ADRES-ADPREV	ADRES-ADPREV	First derivative of single measurement(2)
			Actual CVD result in CVD mode(2)

Note:

1. When PSIS = 0, the value of ADRES-ADPREV) is the value of (S2-S1) from Computation Modes.
2. When PSIS = 0
3. When PSIS = 1.

20.6.8 Continuous Sampling Mode

Setting the CONT bit automatically retriggers a new conversion cycle after updating the ADACC register. The GO bit remains set and re-triggering occurs automatically.

22.1.3 Adder

The NCO Adder is a full adder, which operates synchronously from the source clock. The addition of the previous result and the increment value replaces the accumulator value on the rising edge of each input clock.

22.1.4 Increment Registers

The increment value is stored in three registers making up a 20-bit incrementer. In order of LSB to MSB they are:

- NCOxINCL
- NCOxINCH
- NCOxINCU

When the NCO module is enabled, the NCOxINCU and NCOxINCH registers should be written first, then the NCOxINCL register. Writing to the NCOxINCL register initiates the increment buffer registers to be loaded simultaneously on the second rising edge of the NCO_clk signal.

The registers are readable and writable. The increment registers are double-buffered to allow value changes to be made without first disabling the NCO module.

When the NCO module is disabled, the increment buffers are loaded immediately after a write to the increment registers.

Important: The increment buffer registers are not user-accessible.

Related Links

NCOxINC

22.2 Fixed Duty Cycle Mode

In Fixed Duty Cycle (FDC) mode, every time the accumulator overflows (NCO_overflow), the output is toggled at a frequency rate half of the $F_{OVERFLOW}$. This provides a 50% duty cycle, provided that the increment value remains constant. For more information, see the figure below.

The FDC mode is selected by clearing the PFM bit.

26.11 CCP Special Event Trigger

When any of the CCPs are configured to trigger a special event, the trigger will clear the TMRxH:TMRxL register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPRxH:CCPRxL register pair becomes the period register for Timer1.

Timer1 should be synchronized and $F_{OSC}/4$ should be selected as the clock source in order to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMRxH or TMRxL coincides with a Special Event Trigger from the CCP, the write will take precedence.

26.12 Peripheral Module Disable

When a peripheral is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module's clock source. The Module Disable bits for Timer1 (TMR1MD) are in the PMD1 register. See Peripheral Module Disable (PMD) chapter for more information.

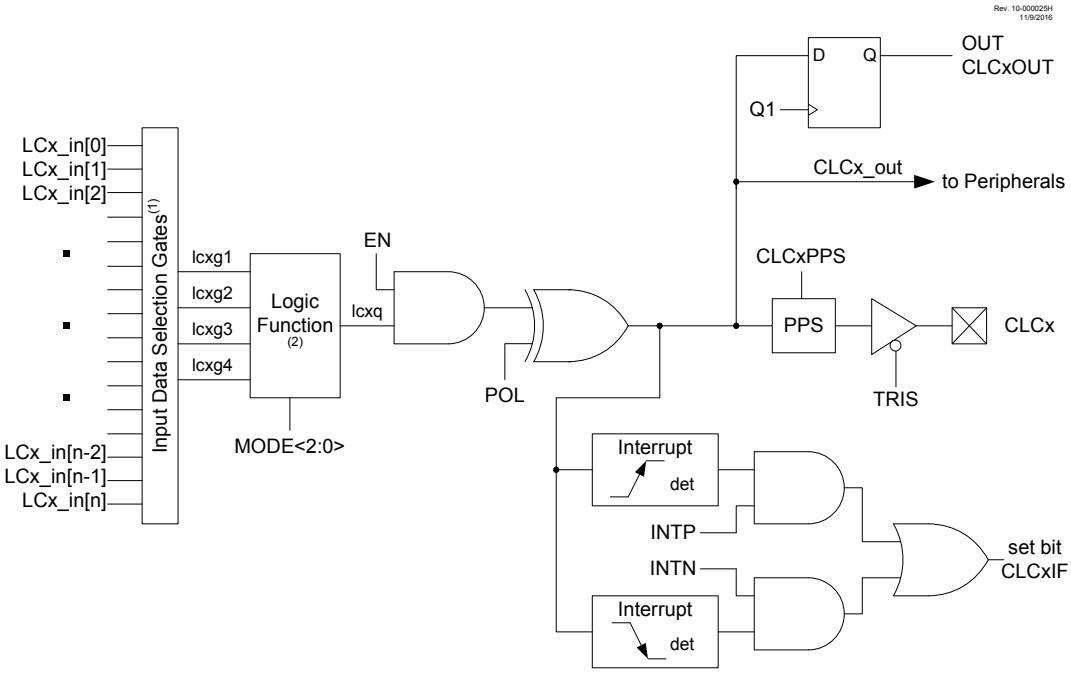
Related Links

Register Summary - PMD

12. Set the EN bit to enable the module.
13. Clear the TRIS bits that correspond to the CWG outputs to set them as outputs.

If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit in software to start the CWG.

Figure 33-1. CLC Simplified Block Diagram



Note:

1. See Figure 33-2 for input data selection and gating.
2. See Figure 33-3 for programmable logic functions.

33.1 CLC Setup

Programming the CLC module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLC Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

33.1.1 Data Selection

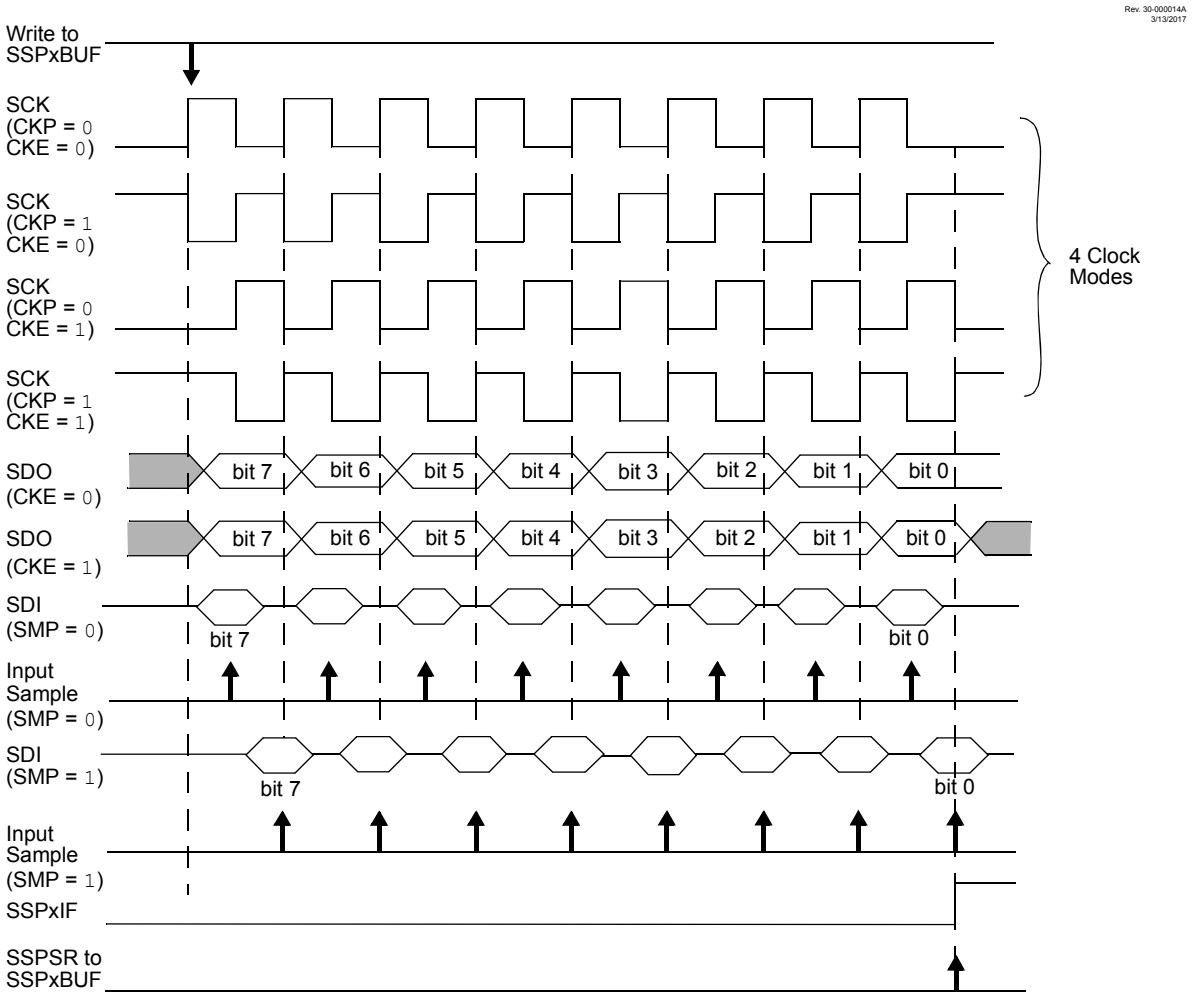
There are 64 signals available as inputs to the configurable logic. Four 64-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of the following diagram. Data inputs in the figure are identified by a generic numbered input name.

33.7 Register Summary - CLC Control

Offset	Name	Bit Pos.								
0x1E0F	CLCDATA	7:0					MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT
0x1E10	CLC1CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E11	CLC1POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E12	CLC1SEL0	7:0			D1S[5:0]					
0x1E13	CLC1SEL1	7:0			D2S[5:0]					
0x1E14	CLC1SEL2	7:0			D3S[5:0]					
0x1E15	CLC1SEL3	7:0			D4S[5:0]					
0x1E16	CLC1GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E17	CLC1GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E18	CLC1GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E19	CLC1GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E1A	CLC2CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E1B	CLC2POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E1C	CLC2SEL0	7:0			D1S[5:0]					
0x1E1D	CLC2SEL1	7:0			D2S[5:0]					
0x1E1E	CLC2SEL2	7:0			D3S[5:0]					
0x1E1F	CLC2SEL3	7:0			D4S[5:0]					
0x1E20	CLC2GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E21	CLC2GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E22	CLC2GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E23	CLC2GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E24	CLC3CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E25	CLC3POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E26	CLC3SEL0	7:0			D1S[5:0]					
0x1E27	CLC3SEL1	7:0			D2S[5:0]					
0x1E28	CLC3SEL2	7:0			D3S[5:0]					
0x1E29	CLC3SEL3	7:0			D4S[5:0]					
0x1E2A	CLC3GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E2B	CLC3GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E2C	CLC3GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E2D	CLC3GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E2E	CLC4CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E2F	CLC4POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E30	CLC4SEL0	7:0			D1S[5:0]					
0x1E31	CLC4SEL1	7:0			D2S[5:0]					
0x1E32	CLC4SEL2	7:0			D3S[5:0]					
0x1E33	CLC4SEL3	7:0			D4S[5:0]					
0x1E34	CLC4GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E35	CLC4GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E36	CLC4GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E37	CLC4GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N

Figure 35-4. SPI Mode Waveform (Master Mode)



35.2.2 SPI Slave Mode

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSPxIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

35.2.3 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole

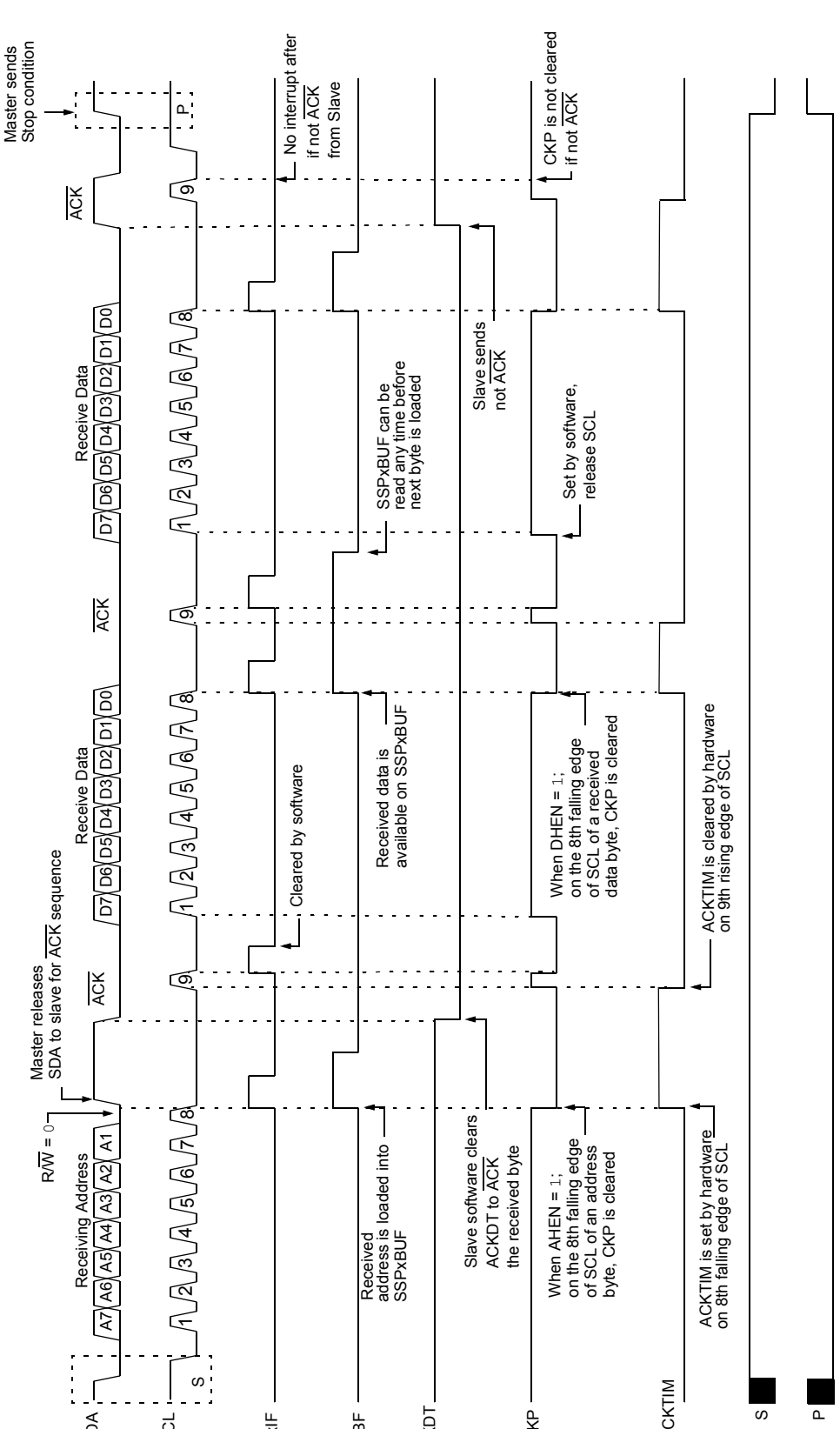


Figure 35-17. I²C Slave, 7-bit Address, Reception (SEN = 1, AHEN = 1, DHEN = 1)

36.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

36.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCxSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCxIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

36.1.2.8 Asynchronous Reception Setup

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see the EUSART Baud Rate Generator (BRG) section).
2. Set the RXxPPS register to select the RXx/DTx input pin.
3. Clear the ANSEL bit for the RXx pin (if applicable).
4. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
5. If interrupts are desired, set the RCxIE bit of the PIEx register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set the RX9 bit.
7. Enable reception by setting the CREN bit.
8. The RCxIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit was also set.
9. Read the RCxSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

36.1.2.9 9-Bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable follow these steps:

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see the EUSART Baud Rate Generator (BRG) section).
2. Set the RXxPPS register to select the RXx input pin.
3. Clear the ANSEL bit for the RXx pin (if applicable).
4. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.

36.6.1 RCxSTA

Name: RCxSTA
Address: 0x011D

Receive Status and Control Register

Bit	7	6	5	4	3	2	1	0
	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
Access	R/W	R/W	R/W	R/W	R/W	RO	R/HC	R/HC
Reset	0	0	0	0	0	0	0	0

Bit 7 – SPEN Serial Port Enable bit

Value	Description
1	Serial port enabled
0	Serial port disabled (held in Reset)

Bit 6 – RX9 9-Bit Receive Enable bit

Value	Description
1	Selects 9-bit reception
0	Selects 8-bit reception

Bit 5 – SREN Single Receive Enable bit
Controls reception. This bit is cleared by hardware when reception is complete

Value	Condition	Description
1	SYNC = 1 AND CSRC = 1	Start single receive
0	SYNC = 1 AND CSRC = 1	Single receive is complete
X	SYNC = 0 OR CSRC = 0	Don't care

Bit 4 – CREN Continuous Receive Enable bit

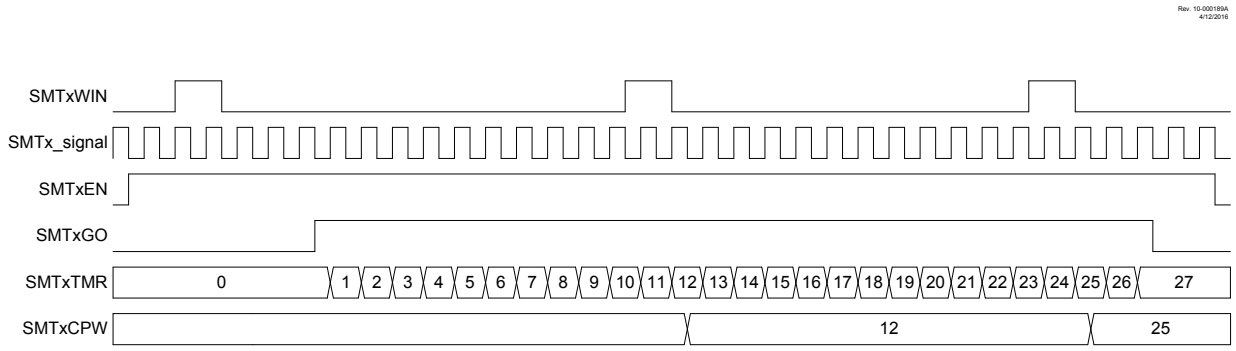
Value	Condition	Description
1	SYNC = 1	Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0	SYNC = 1	Disables continuous receive
1	SYNC = 0	Enables receiver
0	SYNC = 0	Disables receiver

Bit 3 – ADDEN Address Detect Enable bit

Value	Condition	Description
1	SYNC = 0 AND RX9 = 1	The receive buffer is loaded and the interrupt occurs only when the ninth received bit is set
0	SYNC = 0 AND RX9 = 1	All bytes are received and interrupt always occurs. Ninth bit can be used as parity bit
X	RX9 = 0 OR SYNC = 1	Don't care

Bit 2 – FERR Framing Error bit

Figure 37-17. Counter Mode Timing Diagram



37.1.6.10 Gated Counter Mode

This mode counts pulses on the signal input, gated by the window input. It begins incrementing the timer upon seeing a rising edge of the window input and updates the SMTxCPW register upon a falling edge on the window input. See figures below.

Figure 37-18. Gated Counter Mode, Repeat Acquisition Timing Diagram

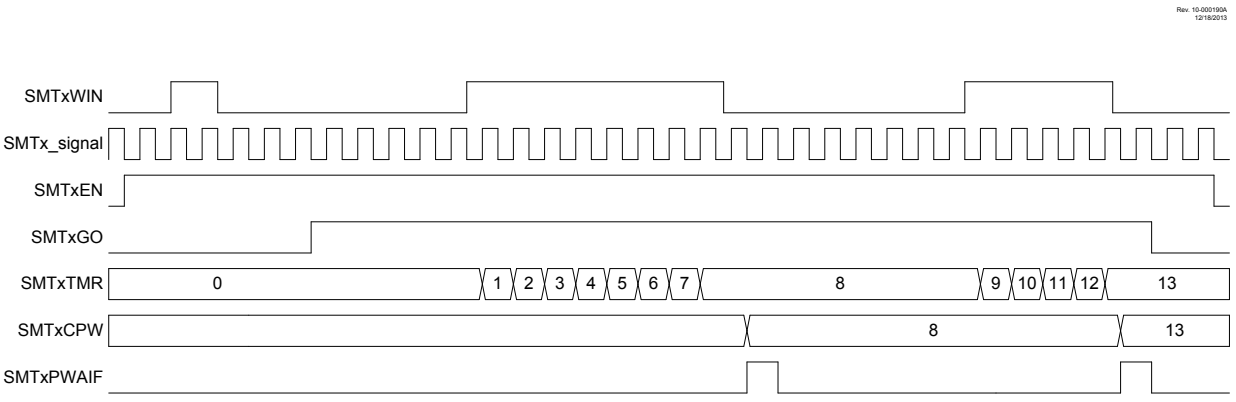
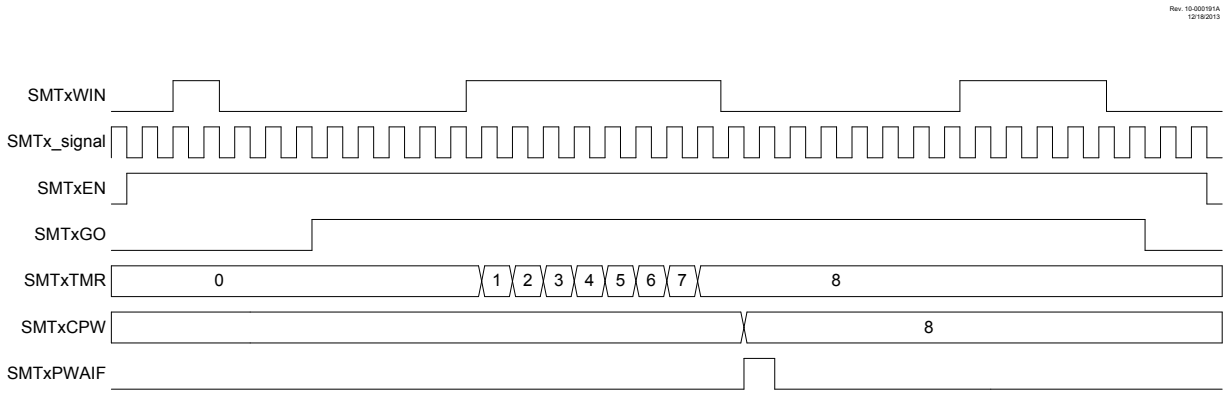


Figure 37-19. Gated Counter Mode, Single Acquisition Timing Diagram



37.1.6.11 Windowed Counter Mode

This mode counts pulses on the signal input, within a window dictated by the window input. It begins counting upon seeing a rising edge of the window input, updates the SMTxCPW register on a falling edge

Offset	Name	Bit Pos.								
0x1EB8	MDCARLPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EB9	MDCARHPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBA	MDSRCPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBB	CLCIN1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBC	CLCIN2PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBD	CLCIN3PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBE	CLCIN4PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EBF ... 0x1EC2	Reserved									
0x1EC3	ADACTPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC4	Reserved									
0x1EC5	SSP1CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC6	SSP1DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC7	SSP1SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC8	SSP2CLKPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1EC9	SSP2DATPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECA	SSP2SSPPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECB	RX1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECC	CK1PPS	7:0				PORT[1:0]		PIN[2:0]		
0x1ECD ... 0x1EFF	Reserved									
0x1F00	INDF0	7:0	INDF0[7:0]							
0x1F01	INDF1	7:0	INDF1[7:0]							
0x1F02	PCL	7:0	PCL[7:0]							
0x1F03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1F04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1F06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1F08	BSR	7:0			BSR[5:0]					
0x1F09	WREG	7:0	WREG[7:0]							
0x1F0A	PCLATH	7:0		PCLATH[6:0]						
0x1F0B	INTCON	7:0	GIE	PEIE						INTEDG
0x1F0C ... 0x1F0F	Reserved									
0x1F10	RA0PPS	7:0			PPS[5:0]					
0x1F11	RA1PPS	7:0			PPS[5:0]					
0x1F12	RA2PPS	7:0			PPS[5:0]					
0x1F13	Reserved									
0x1F14	RA4PPS	7:0			PPS[5:0]					
0x1F15	RA5PPS	7:0			PPS[5:0]					
0x1F16 ...	Reserved									

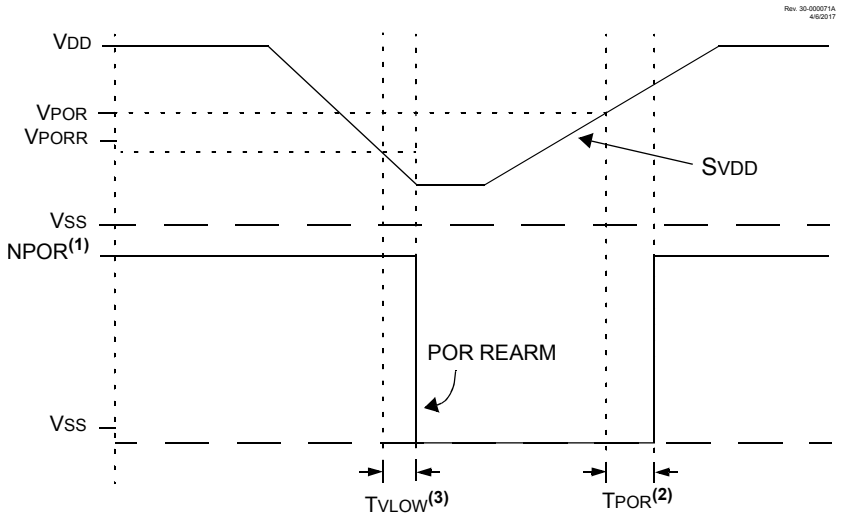
PIC16F18426/46 only							
Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
D005	V_{PORR}		—	1.5	—	V	BOR or LPBOR disabled(3)
V_{DD} Rise Rate to ensure internal Power-on Reset signal(2)							
D006	S_{VDD}		0.05	—	—	V/ms	BOR or LPBOR disabled(3)

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. This is the limit to which V_{DD} can be lowered in Sleep mode without losing RAM data.
2. See the following figure, POR and POR REARM with Slow Rising V_{DD}.
3. Please see Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-Out Reset and Low-Power Brown-Out Reset Specifications for BOR and LPBOR trip point information.

Figure 42-3. POR and POR Rearm with Slow Rising V_{DD}



Note:

1. When NPOR is low, the device is held in Reset.
2. T_{POR} 1 µs typical.
3. T_{VLOW} 2.7 µs typical.

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C, T_{AD} = 1µs							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. Total Absolute Error is the sum of the offset, gain and integral non-linearity (INL) errors.
2. The ADC conversion result never decreases with an increase in the input and has no missing codes.

42.4.8 Analog-to-Digital Converter (ADC) Conversion Timing Specifications

Table 42-14.

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
AD20	T_{AD}	ADC Clock Period	1	—	9	µs	Using F_{OSC} as the ADC clock source ADCS = 1
AD21			—	2	—	µs	Using F_{RC} as the ADC clock source ADCS = 0
AD22	T_{CNV}	Conversion Time(1)	—	13+3T_{CY}	—	—	Using F_{OSC} as the ADC clock source ADCS = 1
			—	16+2T_{CY}	—	—	Using F_{RC} as the ADC clock source ADCS = 0
AD23	T_{ACQ}	Acquisition Time	—	2	—	µs	
AD24	T_{HCD}	Sample and Hold Capacitor Disconnect Time	—	2T_{AD}+1T_{CY}	—	—	Using F_{OSC} as the ADC clock source ADCS = 1
			—	3T_{AD}+2T_{CY}	—	—	Using F_{RC} as the ADC clock source ADCS = 0

* - These parameters are characterized but not tested.

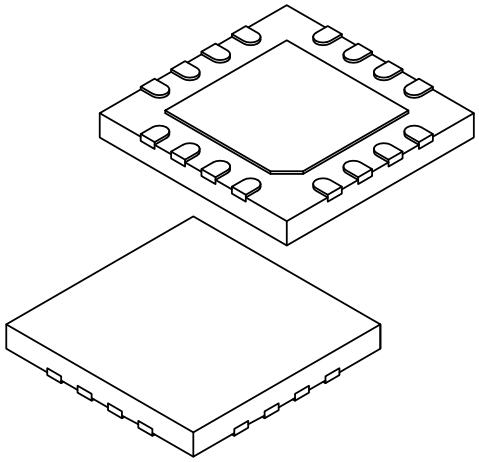
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. Does not apply for the ADCRC oscillator.

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-257A Sheet 2 of 2

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