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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

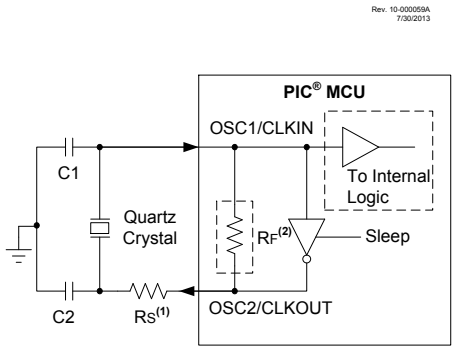
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18446-e-ss

  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules:
  - 4 CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Pulse-Width Modulators (PWM):
  - 2 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock: 0 Hz < f_{NCO} < 32 MHz
  - Resolution: $f_{NCO}/2^{20}$
- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Serial Communications:
  - EUSART
    - 1 EUSART(s)
    - RS-232, RS-485, LIN compatible
    - Auto-Baud Detect, Auto-wake-up on Start.
  - Master Synchronous Serial Port (MSSP)
    - 2 MSSP(s)
    - SPI
    - I^2C, SMBus and PMBus™ compatible
- Data Signal Modulator (DSM)
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms
- Up to 18 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable
- Timer modules:
  - Timer0:
    - 8/16-bit timer/counter
    - Synchronous or asynchronous operation
    - Programmable prescaler/postscaler
    - Time base for capture/compare function
  - Timer1/3/5 with gate control:
    - 16-bit timer/counter
    - Programmable internal or external clock sources
    - Multiple gate sources

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require operating frequencies up to 20 MHz.

Figure 9-3 and Figure 9-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

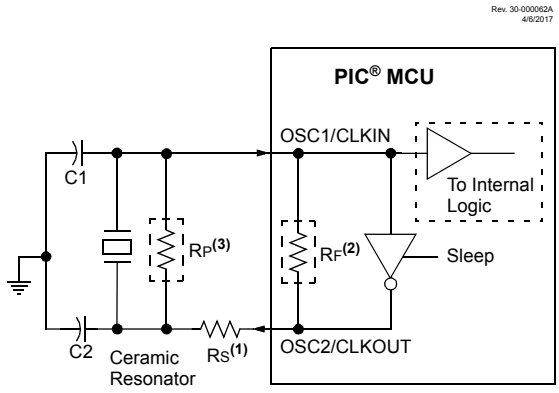
Figure 9-3. Quartz Crystal Operation (LP, XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for quartz crystals with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Figure 9-4. Ceramic Resonator Operation (XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for ceramic resonators with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).
3. An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation.

9.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR), or a wake-up from Sleep. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

9.2.1.4 4x PLL

The oscillator module contains a 4x PLL that can be used with the external clock sources to provide a system clock source. The input frequency for the PLL must fall within specifications.

The PLL can be enabled for use by one of two methods:

1. Program the RSTOSC bits in the Configuration Word 1 to '010' (enable EXTOSC with 4x PLL).
2. Write the NOSC bits to '010' (enable EXTOSC with 4x PLL).

Related Links

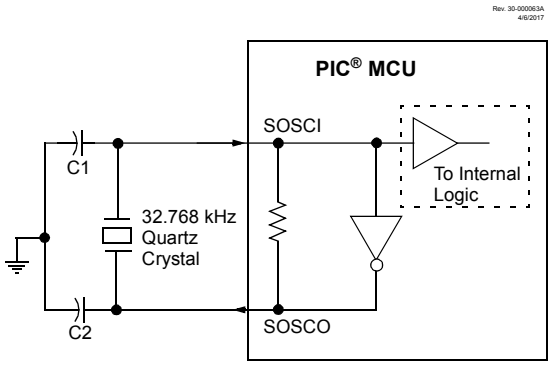
OSCCON1

PLL Specifications

9.2.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. The secondary oscillator can be selected during run-time using clock switching.

Figure 9-5. Quartz Crystal Operation (Secondary Oscillator)



Note:

1. Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
2. Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.
3. For oscillator design assistance, reference the following Microchip Application Notes:
   - AN826, *"Crystal Oscillator Basics and Crystal Selection for PIC® and PIC® Devices"* (DS00826)
   - AN849, *"Basic PIC® Oscillator Design"* (DS00849)
   - AN943, *"Practical PIC® Oscillator Analysis and Design"* (DS00943)
   - AN949, *"Making Your Oscillator Work"* (DS00949)
   - TB097, *"Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS"* (DS91097)
   - AN1288, *"Design Practices for Low-Power External Oscillators"* (DS01288)

Related Links

Clock Switching

NDIV<3:0>	Clock Divider
0001	2
0000	1

Note:

1. The default value (f) is determined by the CONFIG1[RSTOSC] Configuration bits.
2. If NOSC is written with a reserved value, the operation is ignored and NOSC is not written.
3. When CONFIG1[CSWEN] = 0, this register is read-only and cannot be changed from the POR value.
4. When NOSC = 110 (HFINTOSC 1 MHz), the NDIV bits will default to '0010' upon Reset; for all other NOSC settings the NDIV bits will default to '0000' upon Reset.
5. EXTOSC configured by CONFIG1[FEXTOSC].
6. HFINTOSC frequency is set with the FRQ bits of the OSCFRQ register.

Related Links

CONFIG1

PLL Specifications

Note:

1. 7FFFh is the maximum Program Flash Memory address for the PIC16(L)F184XX family.

Related Links

Memory Organization

13.4.5 NVMREG Write to Program Memory

Program memory is programmed using the following steps:

1. Load the address of the row to be programmed into NVMADRH:NVMADRL.
2. Load each write latch with data.
3. Initiate a programming operation.
4. Repeat steps 1 through 3 until all data is written.

Before writing to program memory, the word(s) to be written must be erased or previously unwritten. Program memory can only be erased one row at a time. No automatic erase occurs upon the initiation of the write.

Program memory can be written one or more words at a time. The maximum number of words written at one time is equal to the number of write latches. See the figure below (row writes to program memory with 32 write latches) for more details.

The write latches are aligned to the Flash row address boundary defined by the upper ten bits of NVMADRH:NVMADRL, (NVMADRH<6:0>:NVMADRL<7:5>) with the lower five bits of NVMADRL, (NVMADRL<4:0>) determining the write latch being loaded. Write operations do not cross these boundaries. At the completion of a program memory write operation, the data in the write latches is reset to contain 0x7FFF.

The following steps should be completed to load the write latches and program a row of program memory. These steps are divided into two parts. First, each write latch is loaded with data from the NVMDATH:NVMDATL using the unlock sequence with LWLO = 1. When the last word to be loaded into the write latch is ready, the LWLO bit is cleared and the unlock sequence executed. This initiates the programming operation, writing all the latches into Flash program memory.

Important: The special unlock sequence is required to load a write latch with data or initiate a Flash programming operation. If the unlock sequence is interrupted, writing to the latches or program memory will not be initiated.

1. Set the WREN bit of the NVMCON1 register.
2. Clear the NVMREGS bit of the NVMCON1 register.
3. Set the LWLO bit of the NVMCON1 register. When the LWLO bit of the NVMCON1 register is '1', the write sequence will only load the write latches and will not initiate the write to Flash program memory.
4. Load the NVMADRH:NVMADRL register pair with the address of the location to be written.
5. Load the NVMDATH:NVMDATL register pair with the program memory data to be written.
6. Execute the unlock sequence. The write latch is now loaded.
7. Increment the NVMADRH:NVMADRL register pair to point to the next location.
8. Repeat steps 5 through 7 until all but the last write latch has been loaded.

14.6.13 WPUA

Name: WPUA
Address: 0x1F39

Weak Pull-up Register

Bit	7	6	5	4	3	2	1	0
			WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5 – WPUAn Weak Pull-up PORTA Control bits

Value	Description
1	Weak Pull-up enabled
0	Weak Pull-up disabled

Note:

1. If MCLRE = 1, the weak pull-up in RA3 is always enabled; bit WPUA3 will read as '1'.
2. The weak pull-up device is automatically disabled if the pin is configured as an output.

14.6.22 INLVLA

Name: INLVLA
Address: 0x1F3C

Input Level Control Register

Bit	7	6	5	4	3	2	1	0
			INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5 – INLVLAn Input Level Select on RA Pins

Value	Description
1	ST input used for port reads and interrupt-on-change
0	TTL input used for port reads and interrupt-on-change

14.6.24 INLVLC

Name: INLVLC
Address: 0x1F52

Input Level Control Register

Bit	7	6	5	4	3	2	1	0
	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – INLVLCn Input Level Select on RC Pins

Value	Description
1	ST input used for port reads and interrupt-on-change
0	TTL input used for port reads and interrupt-on-change

Note: Bits INLVLC6 and INLVLC7 available on 20-pin or higher pin-count devices only; Bits unimplemented for lower pin-count devices.

17.6.8 IOCCN

Name: IOCCN
Address: 0x1F54

Interrupt-on-Change Negative Edge Register

Bit	7	6	5	4	3	2	1	0
	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCCNn Interrupt-on-Change Negative Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCC pin for a negative-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin

Note: IOCCN6 and IOCCN7 are available on 20-pin or higher pin-count devices only.

20.8.4 ADCON3

Name: ADCON3
Address: 0x114

ADC Control Register 3

Bit	7	6	5	4	3	2	1	0
		CALC[2:0]			SOI	MD[2:0]		
Access		R/W	R/W	R/W	R/W/HC	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 6:4 – CALC[2:0] ADC Error Calculation Mode Select bits
See ADC Error Calculation Mode table for selection details.

Bit 3 – SOI ADC Stop-on-Interrupt bit

Value	Condition	Description
1	CONT = 1	GO is cleared when the threshold conditions are met, otherwise the conversion is retriggered
0	CONT = 1	GO is not cleared by hardware, must be cleared by software to stop retriggers
x	CONT = 0	This bit is not used

Bits 2:0 – MD[2:0] Threshold Interrupt Mode Select bits

Value	Description
111	Interrupt regardless of threshold test results
110	Interrupt if ERR>UTH
101	Interrupt if ERR≤UTH
100	Interrupt if ERR<LTH or ERR>UTH
011	Interrupt if ERR>LTH and ERR<UTH
010	Interrupt if ERR≥LTH
001	Interrupt if ERR<LTH
000	Never interrupt

synchronization is only possible with the Timer1 clock source. Synchronization with the other odd numbered timers is only possible when they use the same clock source as Timer1.

Related Links

Timer1 Gate

23.4.1 Comparator Output Synchronization

The output from a comparator can be synchronized with Timer1 by setting the SYNC bit.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Figure 23-2 Comparator Block Diagram and the Timer1 Block Diagram for more information.

Related Links

Timer1 Module with Gate Control

23.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator; a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, the following bits must be set:

- EN and POL bits
- CxIE bit of the PIE2 register
- INTP bit (for a rising edge detection)
- INTN bit (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

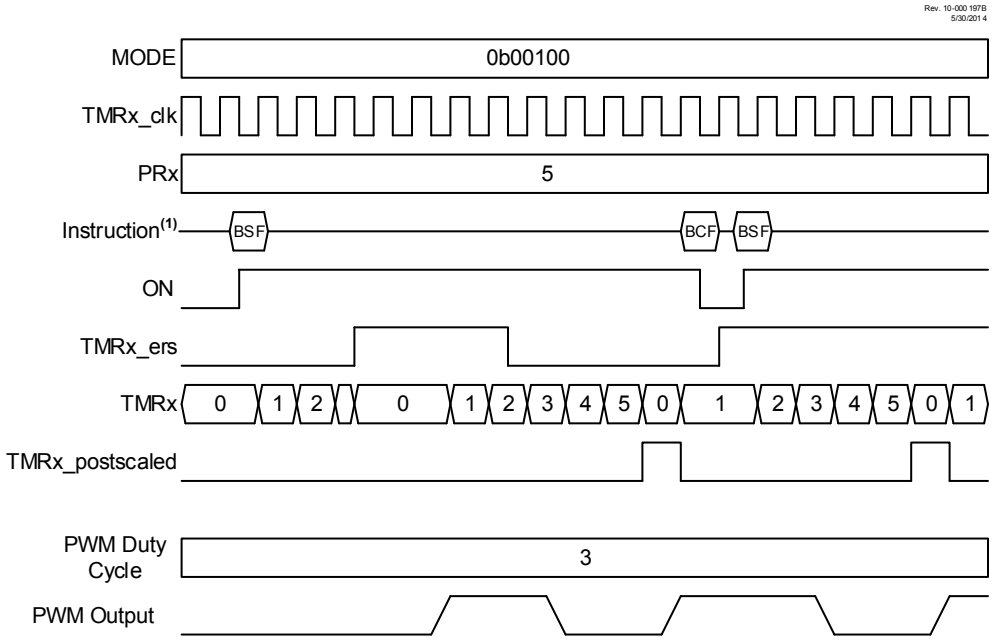
Important: Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the CxPOL bit, or by switching the comparator on or off with the CxEN bit.

23.6 Comparator Positive Input Selection

Configuring the PCH bits direct an internal voltage reference or an analog pin to the non-inverting input of the comparator:

PCH	Positive Input Source
111	CxV_P connects to V_{SS}
110	CxV_P connects to FVR Buffer 2

Figure 27-5. Edge-Triggered Hardware Limit Mode Timing Diagram (MODE = 00100)



Note:

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

Related Links

PWM Overview

(PWM) Pulse-Width Modulation

27.6.4 Level-Triggered Hardware Limit Mode

In the Level-Triggered Hardware Limit Timer modes the counter is reset by high or low levels of the external signal TMRx_ers, as shown in Figure 27-6. Selecting MODE<4:0> = `00110` will cause the timer to reset on a low level external signal. Selecting MODE<4:0> = `00111` will cause the timer to reset on a high level external signal. In the example, the counter is reset while TMRx_ers = `1`. ON is controlled by BSF and BCF instructions. When ON = `0` the external signal is ignored.

When the CCP uses the timer as the PWM time base then the PWM output will be set high when the timer starts counting and then set low only when the timer count matches the CCPRx value. The timer is reset when either the timer count matches the PRx value or two clock periods after the external Reset signal goes true and stays true.

The timer starts counting, and the PWM output is set high, on either the clock following the PRx match or two clocks after the external Reset signal relinquishes the Reset. The PWM output will remain high until the timer counts up to match the CCPRx pulse width value. If the external Reset signal goes true while the PWM output is high then the PWM output will remain high until the Reset signal is released allowing the timer to count up to match the CCPRx value.

Changing Between Capture Prescalers

```
BANKSEL CCP1CON         ;(only needed when CCP1CON is not in ACCESS space)
CLRF    CCP1CON         ;Turn CCP module off
MOVLW   NEW_CAPT_PS     ;CCP ON and Prescaler select → W
MOVWF   CCP1CON         ;Load CCP1CON with this value
```

29.2.5 Capture During Sleep

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock ($F_{OSC}/4$), or by an external clock source.

When Timer1 is clocked by $F_{OSC}/4$, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

Capture mode will operate during Sleep when Timer1 is clocked by an external clock source.

29.3 Compare Mode

The Compare mode function described in this section is available and identical for all CCP modules.

Compare mode makes use of the 16-bit odd numbered Timer resources (Timer1, Timer3, etc.). The 16-bit value of the CCPRx register is constantly compared against the 16-bit value of the TMRx register. When a match occurs, one of the following events can occur:

- Toggle the CCPx output and clear TMRx
- Toggle the CCPx output without clearing TMRx
- Set the CCPx output
- Clear the CCPx output
- Pulse output
- Pulse output and clear TMRx

The action on the pin is based on the value of the MODE control bits. At the same time, the interrupt flag CCPxIF bit is set, and an ADC conversion can be triggered, if selected.

All Compare modes can generate an interrupt and trigger an ADC conversion. When MODE = `'0001'` or `'1011'`, the CCP resets the TMRx register.

The following figure shows a simplified diagram of the compare operation.

Table 29-4. Example PWM Frequencies and Resolutions (F_{OSC} = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	16	4	1	1	1	1
T2PR Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

29.4.7 Operation in Sleep Mode

In Sleep mode, the T2TMR register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, T2TMR will continue from the previous state.

29.4.8 Changes in System Clock Frequency

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See the *"Oscillator Module (with Fail-Safe Clock Monitor)"* section for additional details.

Related Links

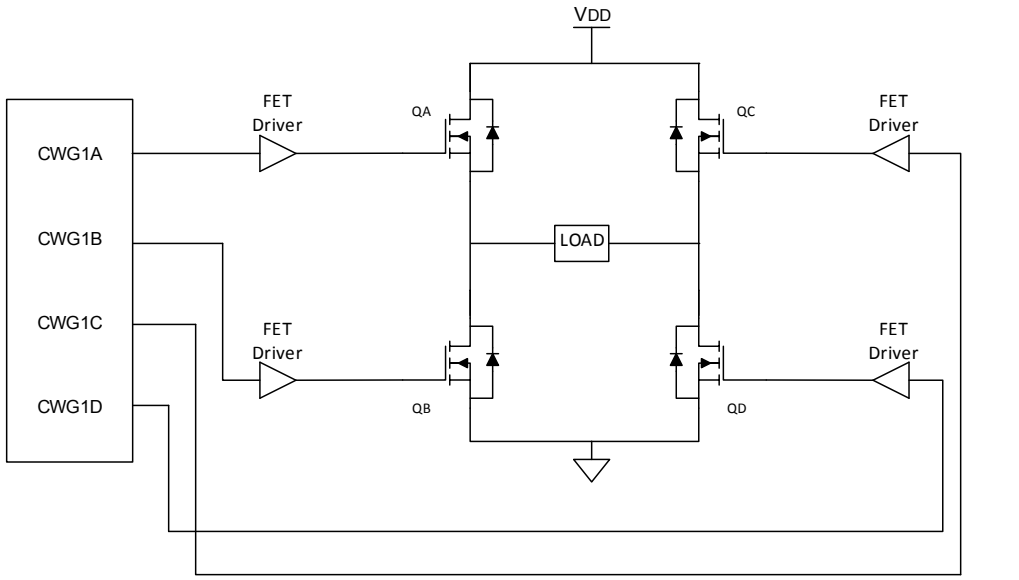
Oscillator Module (with Fail-Safe Clock Monitor)

29.4.9 Effects of Reset

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

CWG module. When connected, as shown in Figure 31-5, the outputs are appropriate for a full-bridge motor driver. Each CWG output signal has independent polarity control, so the circuit can be adapted to high-active and low-active drivers. A simplified block diagram for the Full-Bridge modes is shown in Figure 31-6.

Figure 31-5. Example of Full-Bridge Application



34.5 Register Summary: Reference CLK

Offset	Name	Bit Pos.								
0x0895	CLKRCON	7:0	EN			DC[1:0]		DIV[2:0]		
0x0896	CLKRCLK	7:0					CLK[3:0]			

34.6 Register Definitions: Reference Clock

Long bit name prefixes for the Reference Clock peripherals are shown in the following table. Refer to the "*Long Bit Names*" section for more information.

Table 34-2. TABLE 5-1:

Peripheral	Bit Name Prefix
CLKR	CLKR

Related Links

Long Bit Names

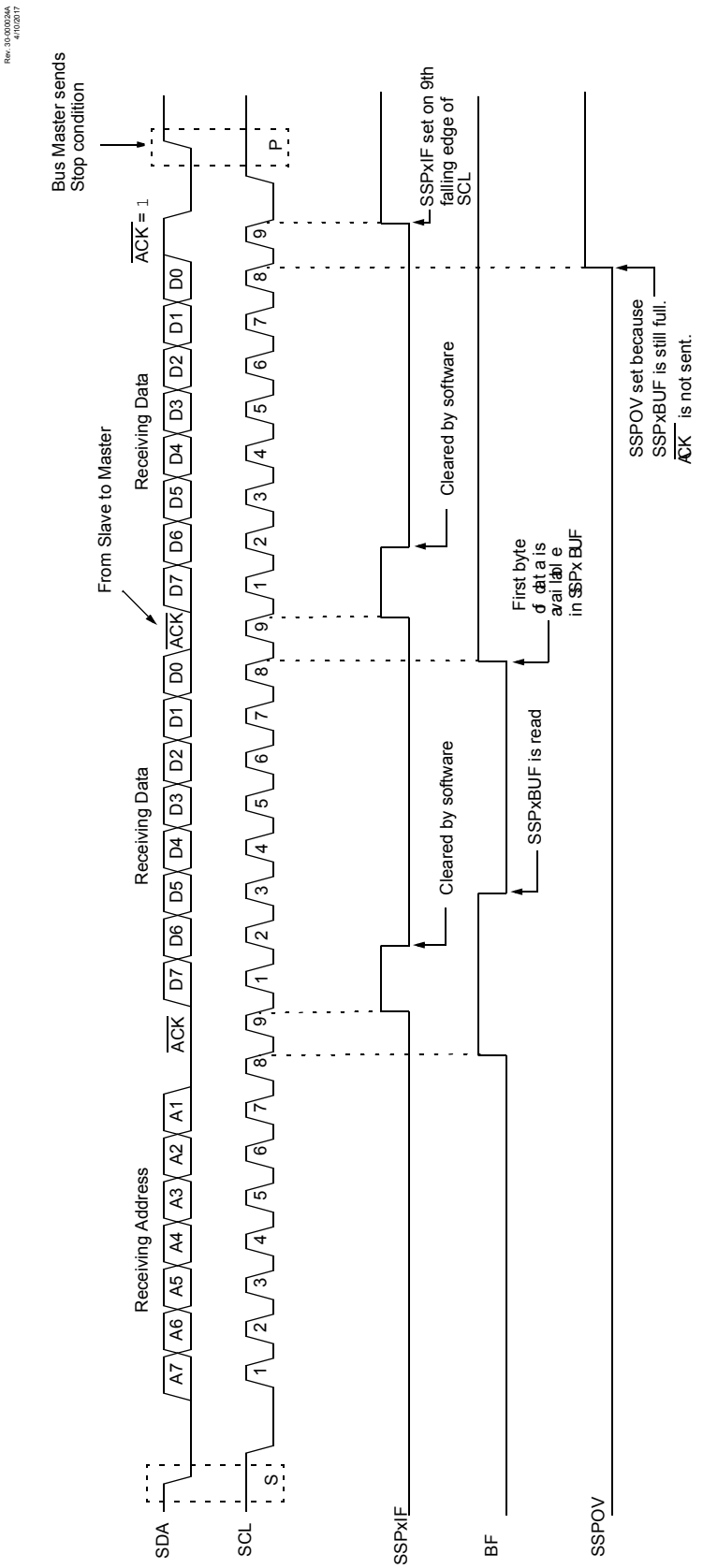


Figure 35-14. I²C Slave, 7-bit Address, Reception (SEN = 0, AHEN = 0, DHEN = 0)

Offset	Name	Bit Pos.								
0x1389	WREG	7:0	WREG[7:0]							
0x138A	PCLATH	7:0		PCLATH[6:0]						
0x138B	INTCON	7:0	GIE	PEIE						INTEDG
0x138C ... 0x13FF	Reserved									
0x1400	INDF0	7:0	INDF0[7:0]							
0x1401	INDF1	7:0	INDF1[7:0]							
0x1402	PCL	7:0	PCL[7:0]							
0x1403	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1404	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1406	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1408	BSR	7:0			BSR[5:0]					
0x1409	WREG	7:0	WREG[7:0]							
0x140A	PCLATH	7:0		PCLATH[6:0]						
0x140B	INTCON	7:0	GIE	PEIE						INTEDG
0x140C ... 0x147F	Reserved									
0x1480	INDF0	7:0	INDF0[7:0]							
0x1481	INDF1	7:0	INDF1[7:0]							
0x1482	PCL	7:0	PCL[7:0]							
0x1483	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1484	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1486	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1488	BSR	7:0			BSR[5:0]					
0x1489	WREG	7:0	WREG[7:0]							
0x148A	PCLATH	7:0		PCLATH[6:0]						
0x148B	INTCON	7:0	GIE	PEIE						INTEDG
0x148C ... 0x14FF	Reserved									
0x1500	INDF0	7:0	INDF0[7:0]							
0x1501	INDF1	7:0	INDF1[7:0]							
0x1502	PCL	7:0	PCL[7:0]							
0x1503	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1504	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1506	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1508	BSR	7:0			BSR[5:0]					
0x1509	WREG	7:0	WREG[7:0]							

Offset	Name	Bit Pos.								
... 0x19FF										
0x1A00	INDF0	7:0	INDF0[7:0]							
0x1A01	INDF1	7:0	INDF1[7:0]							
0x1A02	PCL	7:0	PCL[7:0]							
0x1A03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1A04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1A06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1A08	BSR	7:0			BSR[5:0]					
0x1A09	WREG	7:0	WREG[7:0]							
0x1A0A	PCLATH	7:0		PCLATH[6:0]						
0x1A0B	INTCON	7:0	GIE	PEIE						INTEDG
0x1A0C ... 0x1A7F	Reserved									
0x1A80	INDF0	7:0	INDF0[7:0]							
0x1A81	INDF1	7:0	INDF1[7:0]							
0x1A82	PCL	7:0	PCL[7:0]							
0x1A83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1A84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1A86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1A88	BSR	7:0			BSR[5:0]					
0x1A89	WREG	7:0	WREG[7:0]							
0x1A8A	PCLATH	7:0		PCLATH[6:0]						
0x1A8B	INTCON	7:0	GIE	PEIE						INTEDG
0x1A8C ... 0x1AFF	Reserved									
0x1B00	INDF0	7:0	INDF0[7:0]							
0x1B01	INDF1	7:0	INDF1[7:0]							
0x1B02	PCL	7:0	PCL[7:0]							
0x1B03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1B04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1B08	BSR	7:0			BSR[5:0]					
0x1B09	WREG	7:0	WREG[7:0]							
0x1B0A	PCLATH	7:0		PCLATH[6:0]						
0x1B0B	INTCON	7:0	GIE	PEIE						INTEDG
0x1B0C ...	Reserved									

42. Electrical Specifications

42.1 Absolute Maximum Ratings(†)

Parameter		Rating
Ambient temperature under bias		-40°C to +125°C
Storage temperature		-65°C to +150°C
Voltage on pins with respect to V_{SS}		
• **on V_{DD} pin:**		
	PIC16LF18426/46	-0.3V to +4.0V
	PIC16F18426/46	-0.3V to +6.5V
• **on $\overline{MCLR}$ pin:**		-0.3V to +9.0V
• **on all other pins:**		-0.3V to (V_{DD} + 0.3V)
Maximum current		
• **on V_{SS} pin(1)**	-40°C ≤ T_A ≤ +85°C	250 mA
	85°C < T_A ≤ +125°C	120 mA
• **on V_{DD} pin(1)**	-40°C ≤ T_A ≤ +85°C	250 mA
	85°C < T_A ≤ +125°C	85 mA
• **on any standard I/O pin**		±50 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD})		±20 mA
Total power dissipation(2)		800 mW

Important:

1. Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Thermal Characteristics to calculate device specifications.
2. Power dissipation is calculated as follows:
   $P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma (V_{OI} \times I_{OL})$

NOTICE: Stresses above those listed under *"Absolute Maximum Ratings"* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

42.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \le V_{DD} \le V_{DDMAX}$