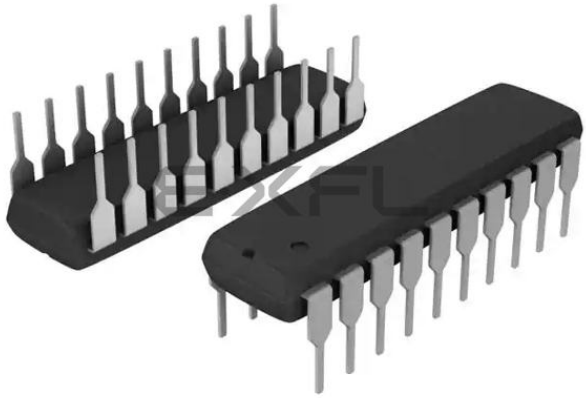

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18446-i-p

11.5.1 VREGCON

Name: VREGCON
Address: 0x812

Voltage Regulator Control Register

Bit	7	6	5	4	3	2	1	0
							VREGPM	
Access							R/W	
Reset							0	

Bit 1 – VREGPM Voltage Regulator Power Mode Selection bit
This register is available only for F devices.

Value	Description
1	Low-Power Sleep mode enabled in Sleep. Draws lowest current in Sleep, slower wake-up
0	Normal Power mode enabled in Sleep. Draws higher current in Sleep, faster wake-up

```
loaded in ADDRH:ADDRL
   ; 4. ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)
   ; 5. NVM interrupts are not taken into account

     BANKSEL    NVMADRH
     MOVF       ADDRH,W
     MOVWF      NVMADRH          ; Load initial address
     MOVF       ADDRL,W
     MOVWF      NVMADRL
     MOVLW      LOW DATA_ADDR    ; Load initial data address
     MOVWF      FSR0L
     MOVLW      HIGH DATA_ADDR
     MOVWF      FSR0H
     BCF        NVMCON1,NVMREGS  ; Set Program Flash Memory as write location
     BSF        NVMCON1,WREN     ; Enable writes
     BSF        NVMCON1,LWLO     ; Load only write latches

   LOOP

     MOVIW      FSR0++
     MOVWF      NVMDATL          ; Load first data byte
     MOVIW      FSR0++
     MOVWF      NVMDATH          ; Load second data byte

     MOVF       NVMADRL,W
     XORLW      0x1F             ; Check if lower bits of address are 00000
     ANDLW      0x1F             ; and if on last of 32 addresses
     BTFSC      STATUS,Z         ; Last of 32 words?
     GOTO       START_WRITE      ; If so, go write latches into memory

     CALL       UNLOCK_SEQ       ; If not, go load latch
     INCF       NVMADRL,F        ; Increment address
     GOTO       LOOP

   START_WRITE

     BCF        NVMCON1,LWLO     ; Latch writes complete, now write memory
     CALL       UNLOCK_SEQ       ; Perform required unlock sequence
     BCF        NVMCON1,WREN     ; Disable writes

   UNLOCK_SEQ

     MOVLW      55h
     BCF        INTCON,GIE       ; Disable interrupts
     MOVWF      NVMCON2          ; Begin unlock sequence
     MOVLW      AAh
     MOVWF      NVMCON2
     BSF        NVMCON1,WR
     BSF        INTCON,GIE       ; Unlock sequence complete, re-enable
interrupts
     return
```

13.4.6 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

1. Load the starting address of the row to be modified.
2. Read the existing data from the row into a RAM image.
3. Modify the RAM image to contain the new data to be written into program memory.
4. Load the starting address of the row to be rewritten.
5. Erase the program memory row.
6. Load the write latches with data from the RAM image.
7. Initiate a programming operation.

14.6.21 SLRCONC

Name: SLRCONC
Address: 0x1F51

Slew Rate Control Register

Bit	7	6	5	4	3	2	1	0
	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5, 6, 7 – SLRCn Slew Rate Control on RC Pins

Value	Description
1	Port pin slew rate is limited
0	Port pin slews at maximum rate

Note: Bits SLRC6 and SLRC7 available on 20-pin or higher pin-count devices only; Bits unimplemented for lower pin-count devices.

Equation 19-1. Sensor Temperature

$$T_{MEAS} = 90 + \frac{(ADC_{MEAS} - ADC_{DIA}) \times FVRA2X}{\left(2^N - 1\right) \times Mv}$$

Note: Where:
ADC_{MEAS} = ADC reading at temperature being estimated

ADC_{DIA} = ADC reading stored in the DIA

FVRA2X = FVR value stored in the DIA for 2x setting

N = Resolution of the ADC

Mv = Temperature Indicator voltage sensitivity (mV/°C)

Note: It is recommended to take the average of 10 measurements of ADC_{MEAS} to reduce noise and improve accuracy.

Related Links
Temperature Indicator Requirements

19.4.1 Calibration

19.4.1.1 Higher-Order Calibration

If the application requires more precise temperature measurement, additional calibrations steps will be necessary. For these applications, two-point or three-point calibration is recommended. An Application Note will be released in future that demonstrates higher-order calibration process. An Application Note will be released in future that demonstrates higher-order calibration process.

19.4.2 Temperature Resolution

The resolution of the ADC reading, Ma (°C/count), depends on both the ADC resolution N and the reference voltage used for conversion, as shown in the equation below. It is recommended to use the smallest V_{REF} value, such as the ADC FVR1 Output Voltage for 2x setting (FVRA2X) value from the DIA Table.

Equation 19-2. Temperature Resolution (°C/LSb)

$$M_a = \frac{V_{REF}}{2^N} * M_t$$

$$M_a = \frac{\frac{V_{REF}}{2^N}}{M_v}$$

Note: Where:
Mv = sensor voltage sensitivity (V/°C)

V_{REF} = Reference voltage of the ADC module (in Volts)

N = Resolution of the ADC.

Related Links
Fixed Voltage Reference (FVR) Specifications

20.8.7 ADREF

Name: ADREF
Address: 0x116

ADC Reference Selection Register

Bit	7	6	5	4	3	2	1	0
				NREF			PREF[1:0]	
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – NREF ADC Negative Voltage Reference Selection bit

Value	Description
1	V_{REF}- is connected to external V_{REF}-
0	V_{REF}- is connected to AV_{SS}

Bits 1:0 – PREF[1:0] ADC Positive Voltage Reference Selection bits

Value	Description
11	V_{REF}+ is connected to internal Fixed Voltage Reference (FVR) module
10	V_{REF}+ is connected to external V_{REF}+
01	Reserved
00	V_{REF}+ is connected to V_{DD}

20.8.11 ADCAP

Name: ADCAP
Address: 0x10E

ADC Additional Sample Capacitor Selection Register

Bit	7	6	5	4	3	2	1	0
				CAP[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CAP[4:0] ADC Additional Sample Capacitor Selection bits

Value	Description
1 to 31	Number of pF in the additional capacitance
0	No additional capacitance

21.7.1 DAC1CON0

Name: DAC1CON0
Address: 0x90E

DAC Control Register

Bit	7	6	5	4	3	2	1	0
	EN		OE1		PSS[1:0]			NSS
Access	R/W		R/W		R/W	R/W		R/W
Reset	0		0		0	0		0

Bit 7 – EN DAC Enable bit

Value	Description
1	DAC is enabled
0	DAC is disabled

Bit 5 – OE1 DAC Voltage Output Enable bit

Value	Description
1	DAC voltage level is output on the DAC1OUT1 pin
0	DAC voltage level is disconnected from the DAC1OUT1 pin

Bits 3:2 – PSS[1:0] DAC Positive Source Select bit

Value	Description
11	Reserved
10	FVR buffer
01	$V_{REF}+$
00	AV_{DD}

Bit 0 – NSS DAC Negative Source Select bit

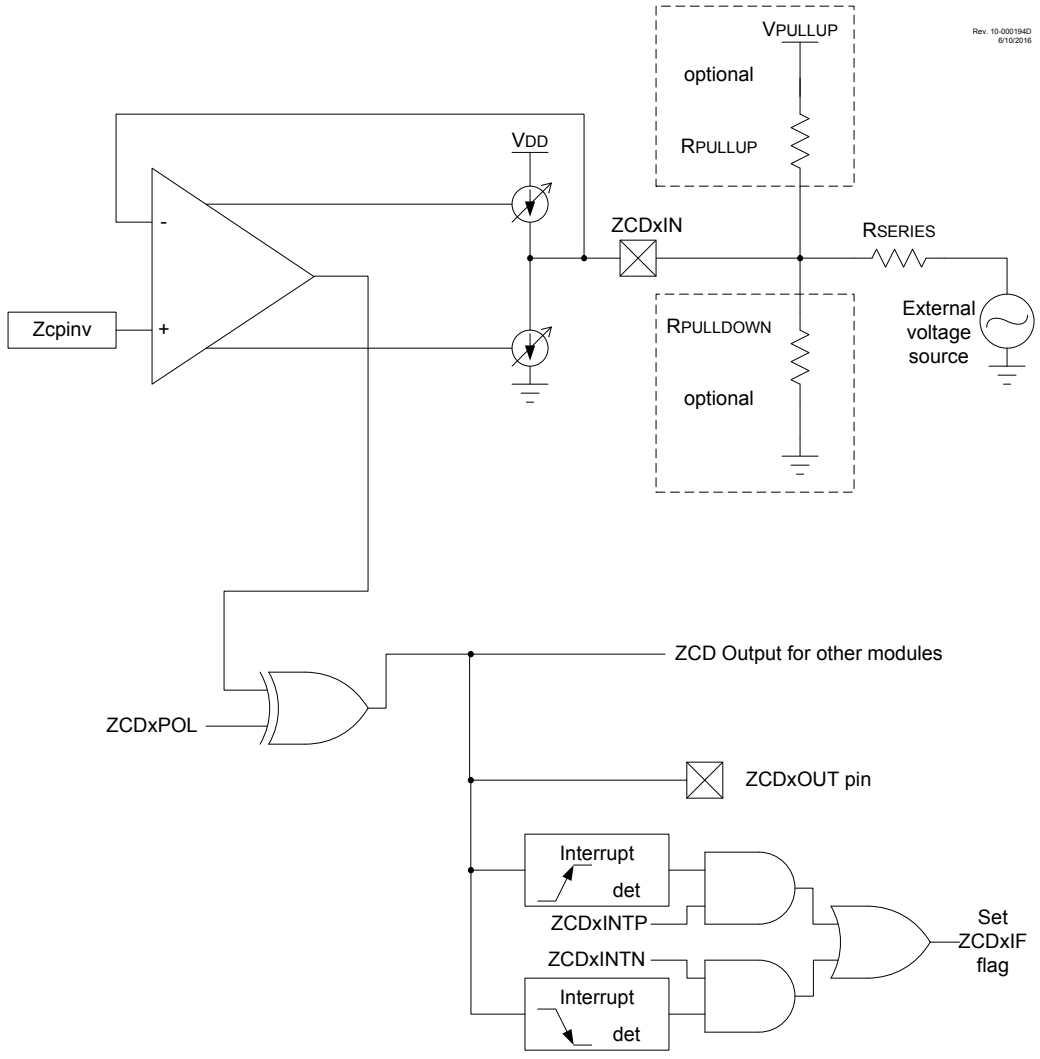
Value	Description
1	$V_{REF}-$
0	AV_{SS}

24. (ZCD) Zero-Cross Detection Module

The ZCD module detects when an A/C signal crosses through the ground potential. The actual zero crossing threshold is the zero crossing reference voltage, Zcpinv, which is typically 0.75V above ground.

The connection to the signal to be detected is through a series current-limiting resistor. The module applies a current source or sink to the ZCD pin to maintain a constant voltage on the pin, thereby preventing the pin voltage from forward biasing the ESD protection diodes. When the applied voltage is greater than the reference voltage, the module sinks current. When the applied voltage is less than the reference voltage, the module sources current. The current source and sink action keeps the pin voltage constant over the full range of the applied voltage. The ZCD module is shown in the following simplified block diagram.

Figure 24-1. Simplified ZCD Block Diagram



The ZCD module is useful when monitoring an A/C waveform for, but not limited to, the following purposes:

- A/C period measurement

PPS Outputs

25.3.3 Timer0 Interrupt

The Timer0 interrupt flag bit (TMR0IF) is set when the TMR0_out toggles. If the Timer0 interrupt is enabled (TMR0IE), the CPU will be interrupted when the TMR0IF bit is set.

When the postscaler bits (T0OUTPS) are set to 1:1 operation (no division), the T0IF flag bit will be set with every TMR0 match or rollover. In general, the TMR0IF flag bit will be set every T0OUTPS +1 matches or rollovers.

25.3.4 Timer0 Example

Timer0 Configuration:

- Timer0 Mode = 16-bit
- Clock Source = $F_{OSC}/4$ (250 kHz)
- Synchronous operation
- Prescaler = 1:1
- Postscaler = 1:2 (T0OUTPS = `1`)

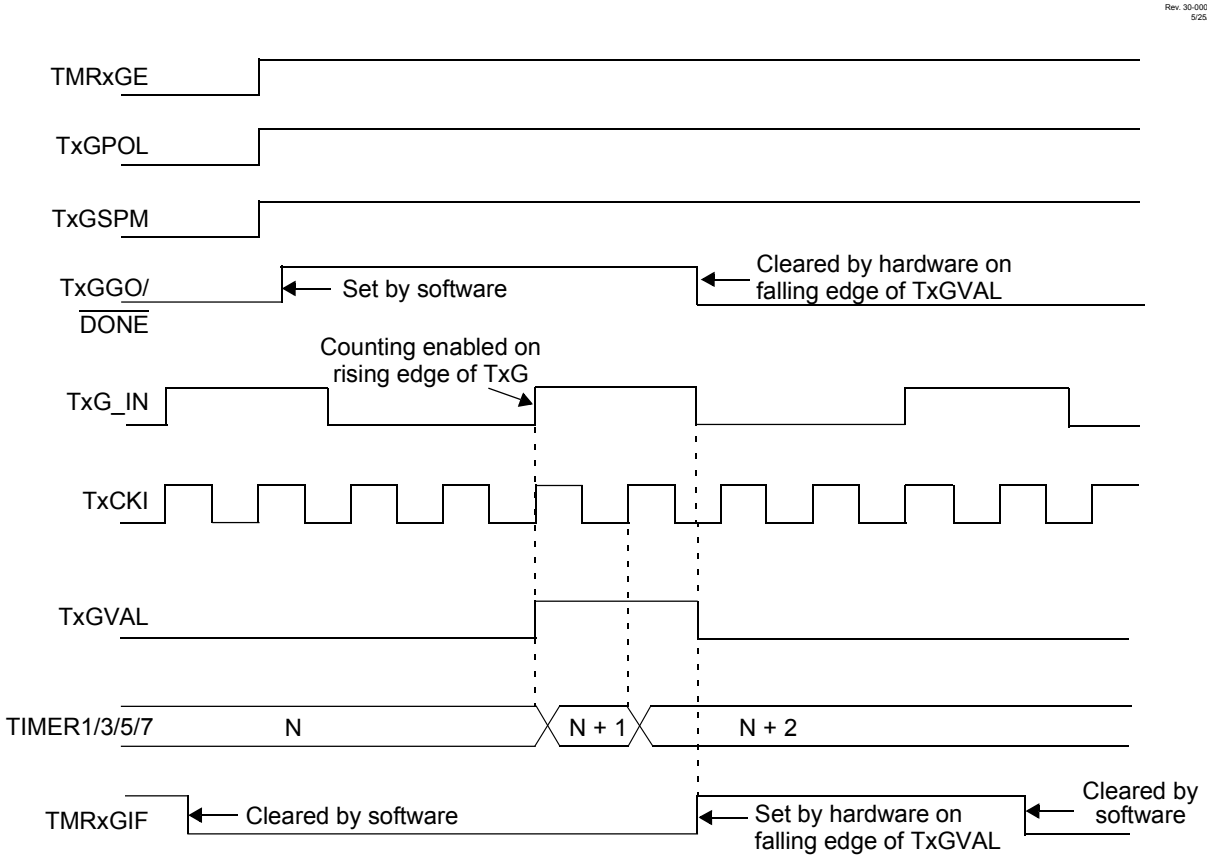
In this case the TMR0_out toggles every two rollovers of TMR0H:TMR0L. i.e. (0xFFFF)*2*(1/250kHz) = 524.28 ms

25.4 Operation During Sleep

When operating synchronously, Timer0 will halt when the device enters Sleep mode.

When operating asynchronously and selected clock source is active, Timer0 will continue to increment and wake the device from Sleep mode if Timer0 interrupt is enabled.

Figure 26-6. TIMER1 GATE SINGLE-PULSE MODE



$$T_{DEAD-BAND\_MAX} = \frac{1}{F_{CWG\_CLOCK}} \bullet DBx<5:0> + 1$$

$$T_{JITTER} = T_{DEAD-BAND\_MAX} - T_{DEAD-BAND\_MIN}$$

$$T_{JITTER} = \frac{1}{F_{CWG\_CLOCK}}$$

$$T_{DEAD-BAND\_MAX} = T_{DEAD-BAND\_MIN} + T_{JITTER}$$

Equation 31-2. Dead-Band Delay Example Calculation

$$DBx<5:0> = 0x0A = 10$$

$$F_{CWG\_CLOCK} = 8\,MHz$$

$$T_{JITTER} = \frac{1}{8\,MHz} = 125ns$$

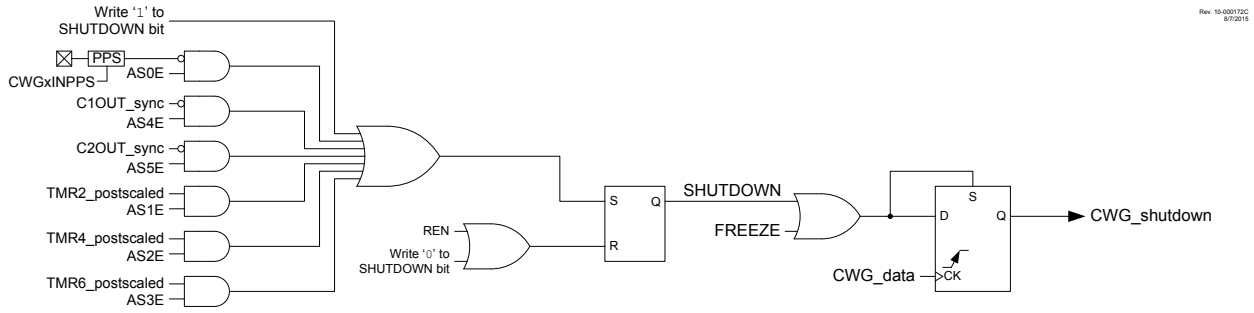
$$T_{DEAD-BAND\_MIN} = 125ns \bullet 10 = 125\mu s$$

$$T_{DEAD-BAND\_MAX} = 1.25\mu s + 0.125\,\mu s = 1.37\mu s$$

31.11 Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in the following figure.

Figure 31-16. CWG Shutdown Block Diagram



31.11.1 Shutdown

The shutdown state can be entered by either of the following two methods:

- Software generated
- External Input

31.11.1.1 Software Generated Shutdown

Setting the SHUTDOWN bit will force the CWG into the shutdown state.

When the auto-restart is disabled, the shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event. The SHUTDOWN bit indicates when a shutdown condition exists. The bit may be set or cleared in software or by hardware.

The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPxBUF register. Additionally, the SSPxSTAT register indicates the various Status conditions.

35.2.1 SPI Master Mode

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 35-3) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPxBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPxBUF register as if a normal received byte (interrupts and Status bits appropriately set).

The clock polarity is selected by appropriately programming the CKP bit and the CKE bit. This then, would give waveforms for SPI communication as shown in Figure 35-4, Figure 35-6, Figure 35-7 and Figure 35-8, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- $F_{OSC}/4$ (or T_{CY})
- $F_{OSC}/16$ (or 4 * T_{CY})
- $F_{OSC}/64$ (or 16 * T_{CY})
- Timer2 output/2
- $F_{OSC}/(4 * (SSPxADD + 1))$

Figure 35-4 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPxBUF is loaded with the received data is shown.

Important: In Master mode the clock signal output to the SCK pin is also the clock signal input to the peripheral. The pin selected for output with the RxyPPS register must also be selected as the peripheral input with the SSPxCLKPPS register. The pin that is selected using the SSPxCLKPPS register should also be made a digital I/O. This is done by clearing the corresponding ANSEL bit.

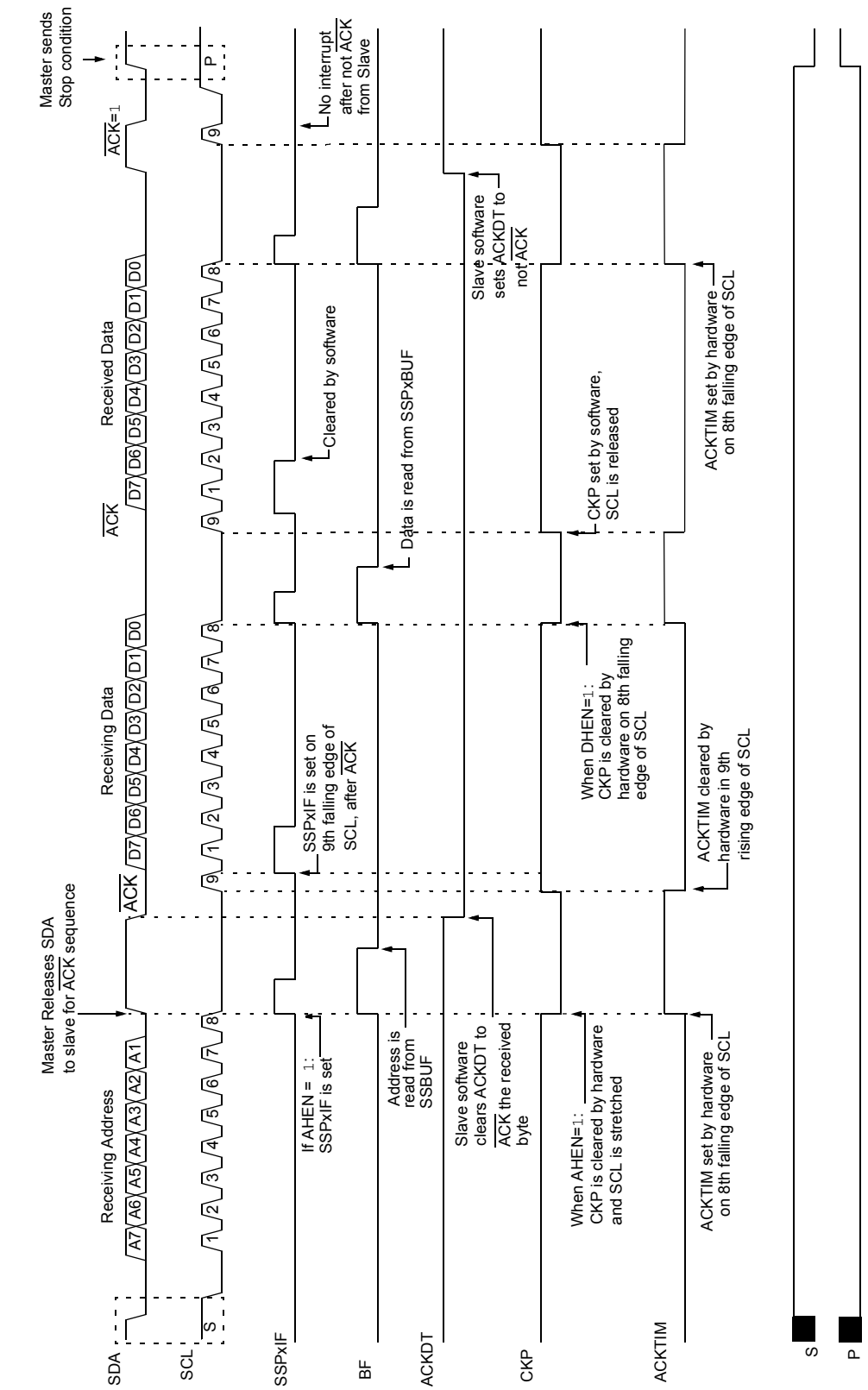


Figure 35-16. I²C Slave, 7-bit Address, Reception (SEN = 0, AHEN = 1, DHEN = 1)

Bit 1 – TRMT Transmit Shift Register (TSR) Status bit

Value	Description
1	TSR is empty
0	TSR is not empty

Bit 0 – TX9D Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note:

1. SREN and CREN bits override TXEN in Sync mode.

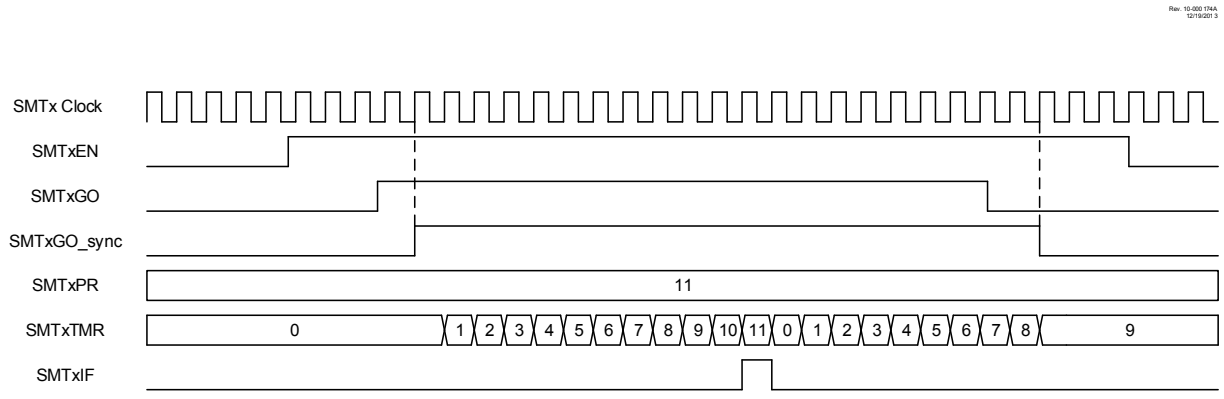
Table 37-4. Modes of Operation

MODE	Mode of operation	Synchronous operation
0000	Timer	Yes
0001	Gated Timer	Yes
0010	Period and Duty Cycle Measurement	Yes
0011	High and low time Measurement	Yes
0100	Windowed Measurement	Yes
0101	Gated Windowed Measurement	Yes
0110	Time of Flight Measurement	Yes
0111	Capture	Yes
1000	Counter	No
1001	Gated Counter	No
1010	Windowed Counter	No
1011-1111	Reserved	-

37.1.6.1 Timer Mode

Timer mode is the basic mode of operation where the SMTxTMR is used as a 24-bit timer. No data acquisition takes place in this mode. The timer increments as long as the SMTxGO bit has been set by software. No SMT window or SMT signal events affect the SMTxGO bit. Everything is synchronized to the SMT clock source. When the timer experiences a period match (SMTxTMR = SMTxPR), SMTxTMR is reset and the period match interrupt trips. See figure below.

Figure 37-2. Timer Mode Timing Diagram



37.1.6.2 Gated Timer Mode

Gated Timer mode uses the signal input (SSEL) to control whether or not the SMTxTMR will increment. Upon a falling edge of the signal, the SMTxCPW register will update to the current value of the SMTxTMR. Example waveforms for both repeated and single acquisitions are provided in figures below.

Table 42-11.

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
RST01*	T_{MCLR}	$\overline{MCLR}$ Pulse Width Low to ensure Reset	2	—	—	µs	
RST02*	T_{IOZ}	I/O high-impedance from Reset detection	—	—	2	µs	
RST03	T_{WDT}	Watchdog Timer Time-out Period	—	16	—	ms	1:512 Prescaler
RST04*	T_{PWRT}	Power-up Timer Period	—	65	—	ms	
RST05	T_{OST}	Oscillator Start-up Timer Period(1, 2)	—	1024	—	T_{OSC}	
RST06	V_{BOR}	Brown-out Reset Voltage	2.55 2.30 1.80	2.7 2.45 1.90	2.85 2.60(3) 2.05	V V V	BORV=0 BORV=1(F devices only) BORV=1(LF Devices only)
RST07	V_{BORHYS}	Brown-out Reset Hysteresis	—	40	—	mV	
RST08	T_{BORDC}	Brown-out Reset Response Time	—	3	—	µs	
RST09	V_{LPBOR}	Low-Power Brown-out Reset Voltage	1.8	1.9	2.2	V	

* - These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.
2. To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.
3. This value corresponds to V_{BORMAX}

43.1 Graphs

Figure 43-1. High Range Temperature Indicator Voltage Sensitivity Across Temperature

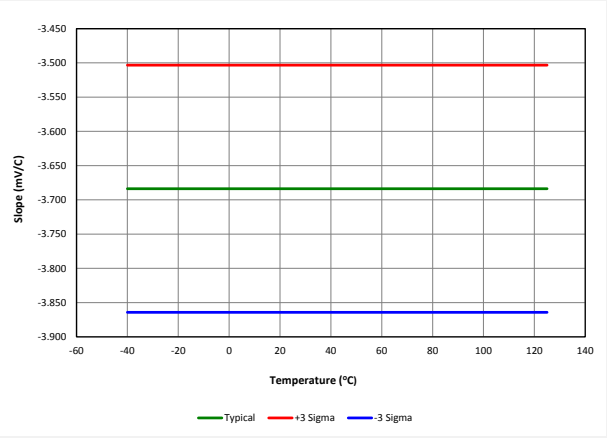
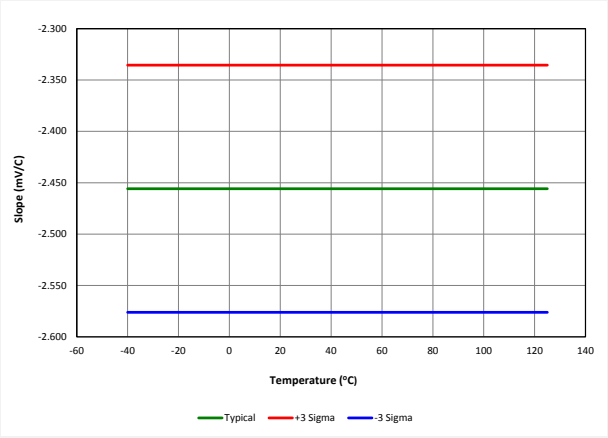
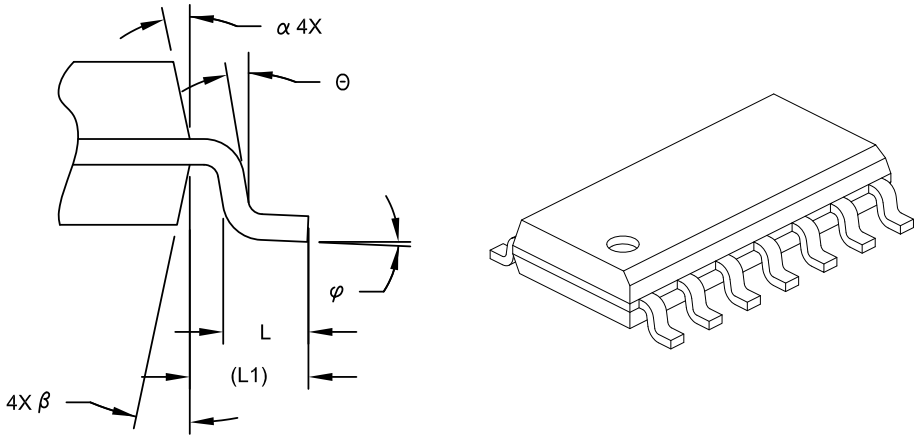


Figure 43-2. Low Range Temperature Indicator Voltage Sensitivity Across Temperature



14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

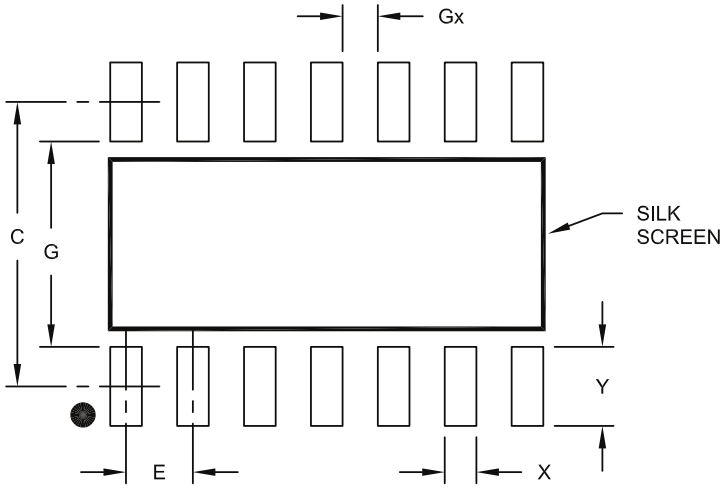
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

45. Revision A (12/2017)

Initial release of this document.