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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18446-i-ss

5. Device Information Area

The Device Information Area (DIA) is a dedicated region in the program memory space; it is a new feature in the PIC16(L)F184XX family of devices. The DIA contains the calibration data for the internal temperature indicator module, stores the Microchip Unique Identifier words, and the Fixed Voltage Reference voltage readings measured in mV. The complete DIA table is shown below, followed by a description of each region and its functionality. The data is mapped from 8100h to 811Fh in the PIC16(L)F184XX family. These locations are read-only and cannot be erased or modified. The data is programmed into the device during manufacturing.

Table 5-1. Device Information Area

Address Range	Name of Region	Standard Device Information
8100h-8108h	MUI0	Microchip Unique Identifier (9 Words)
	MUI1	
	MUI2	
	MUI3	
	MUI4	
	MUI5	
	MUI6	
	MUI7	
	MUI8	
8109h	MUI9	1 Word Reserved
810Ah-8111h	EUI0	Unassigned (8 Words)
	EUI1	
	EUI2	
	EUI3	
	EUI4	
	EUI5	
	EUI6	
	EUI7	
8112h	TSLR1	Unassigned (1 word)
8113h	TSLR2	Temperature indicator ADC reading at 90°C (low range setting)
8114h	TSLR3	Unassigned (1 word)
8115h	TSHR1	Unassigned (1 word)
8116h	TSHR2	Temperature indicator ADC reading at 90°C (high range setting)
8117h	TSHR3	Unassigned (1 word)

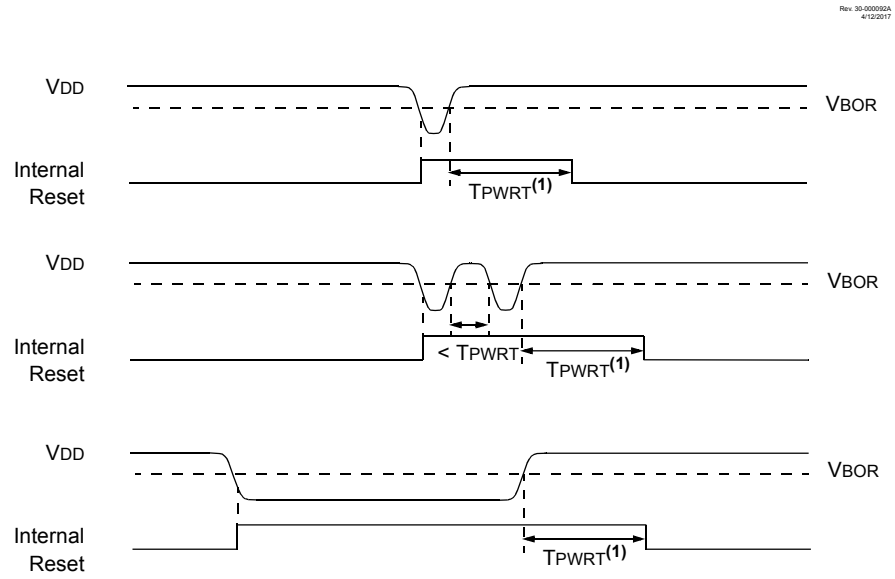
Table 8-1. BOR Operating Conditions

BOREN<1:0>	SBOREN	Device Mode	BOR Mode	Instruction Execution upon: Release of POR or Wake-up from Sleep
11	X	X	Active	Waits for release of BOR(1) (BORRDY = 1)
10	X	Awake	Active	Waits for release of BOR (BORRDY = 1) Waits for BOR Reset release
		Sleep	Disabled	
01	1	X	Active	Waits for BOR Reset release (BORRDY = 1)
	0	X	Disabled	Begins immediately (BORRDY = x)
00	X	X	Disabled	

Note:

1. In this specific case, “Release of POR” and “Wake-up from Sleep”, there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits

Figure 8-2. Brown-out Situations



Note: T_{PWRT} delay only if PWRTS bit field is programmed to a value different from ‘11’.

8.2.4 BOR is Always Off

When the BOREN bits of the Configuration Words are programmed to ‘00’, the BOR is off at all times. The device start-up is not delayed by the BOR ready condition or the V_{DD} level.

8.3 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-out Reset (LPBOR) provides an additional BOR circuit for low power operation. Refer to the figure below to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external V_{DD} pin. When too low of a voltage is detected, the device is held in Reset.

9.6.4 OSCSTAT

Name: OSCSTAT
Address: 0x890

Oscillator Status Register 1

Bit	7	6	5	4	3	2	1	0
	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR		PLLR
Access	RO	RO	RO	RO	RO	RO		RO
Reset	q	q	q	q	q	q		q

Bit 7 – EXTOR EXTOSC (external) Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 6 – HFOR HFINTOSC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 5 – MFOR MFINTOSC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 4 – LFOR LFINTOSC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 3 – SOR Secondary (Timer1) Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 2 – ADOR ADC Oscillator Ready bit

Value	Description
1	The oscillator is ready to be used
0	The oscillator is not enabled, or is not yet ready to be used

Bit 0 – PLLR PLL Ready bit

Table 15-1. PPS Input Signal Routing Options

Input Signal Name	Input Register Name	Default location at POR		Reset Value (xxxPPS<4:0>)	
		14/16-pin devices	20-pin devices	14/16-pin devices	20-pin devices
INT	INTPPS	RA2	RA2	00010	00010
T0CKI	T0CKIPPS	RA2	RA2	00010	00010
T1CKI	T1CKIPPS	RA5	RA5	00101	00101
T1G	T1GPPS	RA4	RA4	00100	00100
T2IN	T2INPPS	RA5	RA5	00101	00101
T3CKI	T3CKIPPS	RC5	RC5	10101	10101
T3G	T3GPPS	RC4	RC4	10100	10100
T4IN	T4INPPS	RC1	RC1	10001	10001
T5CKI	T5CKIPPS	RC0	RC0	10000	10000
T5G	T5GPPS	RC3	RC3	10011	10011
T6IN	T6INPPS	RC2	RC2	10010	10010
MDCARL	MDCARLPPS	RC2	RC2	10010	10010
MDCARH	MDCARHPPS	RC5	RC5	10101	10101
MDSRC	MDSRCPPS	RA1	RA1	00001	00001
CCP1IN	CCP1INPPS	RC5	RC5	10101	10101
CCP2IN	CCP2INPPS	RC3	RC3	10011	10011
CCP3IN	CCP3INPPS	RA2	RA2	00010	00010
CCP4IN	CCP4INPPS	RA4	RA4	00100	00100
CWG1IN	CWG1INPPS	RA2	RA2	00010	00010
CWG2IN	CWG2INPPS	RA2	RA2	00010	00010
CLCIN0	CLCIN0PPS	RC3	RA2	10011	00010
CLCIN1	CLCIN1PPS	RC4	RC3	10100	10011
CLCIN2	CLCIN2PPS	RC1	RB4	10001	01100
CLCIN3	CLCIN3PPS	RA5	RB5	00101	01101
ADACT	ADACTPPS	RC2	RC2	10010	10010
SCK1	SCL1PPS	RC0	RB6	10000	01110
SCL1	SCL1PPS	RC0	RB6	10000	01110
SDI1	SDA1PPS	RC1	RB4	10001	01100
SDA1	SDA1PPS	RC1	RB4	10001	01100

15.9.2 Pin Rxy Output Source Selection Register

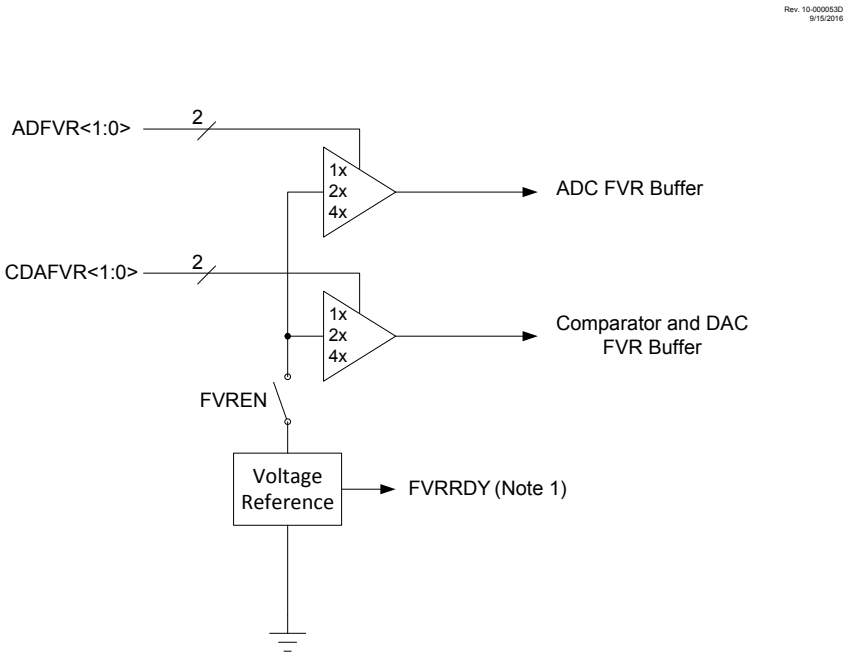
Name: RxyPPS

Important: See Register Summary - PPS for the address offset of each individual register.

Bit	7	6	5	4	3	2	1	0
			RxyPPS[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – RxyPPS[5:0] Pin Rxy Output Source Selection bits
See output source selection table for source codes.

Figure 18-1. Voltage Reference Block Diagram



Note:

1. In the case of an F device, or a device on which the BOR is enabled in the Configuration Word settings, then the FVRRDY bit will be high prior to setting FVREN as those modules require the reference voltage.

20.8.11 ADCAP

Name: ADCAP
Address: 0x10E

ADC Additional Sample Capacitor Selection Register

Bit	7	6	5	4	3	2	1	0
				CAP[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CAP[4:0] ADC Additional Sample Capacitor Selection bits

Value	Description
1 to 31	Number of pF in the additional capacitance
0	No additional capacitance

22. Numerically Controlled Oscillator (NCO) Module

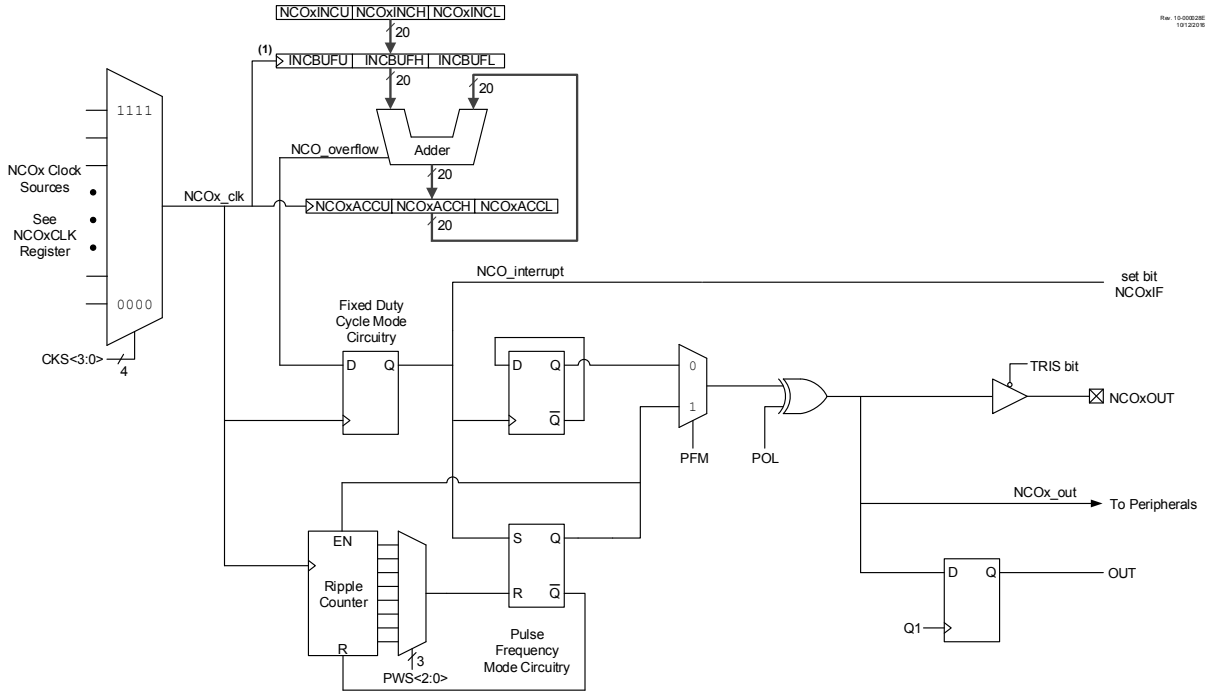
The Numerically Controlled Oscillator (NCO) module is a timer that uses overflow from the addition of an increment value to divide the input frequency. The advantage of the addition method over simple counter driven timer is that the output frequency resolution does not vary with the divider value. The NCO is most useful for application that requires frequency accuracy and fine resolution at a fixed duty cycle.

Features of the NCO include:

- 20-bit Increment Function
- Fixed Duty Cycle mode (FDC) mode
- Pulse Frequency (PF) mode
- Output Pulse Width Control
- Multiple Clock Input Sources
- Output polarity Control
- Interrupt Capability

The following figure is a simplified block diagram of the NCO module.

Figure 22-1. Numerically Controlled Oscillator Module Simplified Block Diagram



Note:

1. The increment registers are double-buffered to allow for value changes to be made without first disabling the NCO module. The full increment value is loaded into the buffer registers on the second rising edge of the NCOx_clk signal that occurs immediately after a write to NCOxINCL register. The buffers are not user-accessible and are shown here for reference.

22.8 Register Summary - NCO

Offset	Name	Bit Pos.								
0x058C	NCO1ACC	7:0	ACCL[7:0]							
		15:8	ACCH[7:0]							
		23:16					ACCU[3:0]			
0x058F	NCO1INC	7:0	INCL[7:0]							
		15:8	INCH[7:0]							
		23:16					INCU[3:0]			
0x0592	NCO1CON	7:0	EN		OUT	POL				PFM
0x0593	NCO1CLK	7:0	PWS[2:0]				CKS[3:0]			

22.9 Register Definitions: NCO

Long bit name prefixes for the NCO peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 22-2. NCO Long Bit Name Prefixes

Peripheral	Bit Name Prefix
NCO	NCO

Related Links

Long Bit Names

27.9.6 TxRST

Name: TxRST
Address: 0x291,0x297,0x29D

Timer External Reset Signal Selection Register

Bit	7	6	5	4	3	2	1	0
					RSEL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – RSEL[3:0]
External Reset Source Selection Bits

Value	Description
n	See External Reset Sources table

31.14 Register Summary - CWG Control

Offset	Name	Bit Pos.								
0x060C	CWG1CLK	7:0								CS
0x060D	CWG1ISM	7:0					ISM[3:0]			
0x060E	CWG1DBR	7:0			DBR[5:0]					
0x060F	CWG1DBF	7:0			DBF[5:0]					
0x0610	CWG1CON0	7:0	EN	LD				MODE[2:0]		
0x0611	CWG1CON1	7:0			IN		POLD	POLC	POLB	POLA
0x0612	CWG1AS0	7:0	SHUTDOWN	REN	LSBD[1:0]		LSAC[1:0]			
0x0613	CWG1AS1	7:0			AS5E	AS4E	AS3E	AS2E	AS1E	AS0E
0x0614	CWG1STR	7:0	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA
0x0615	Reserved									
0x0616	CWG2CLK	7:0								CS
0x0617	CWG2ISM	7:0					ISM[3:0]			
0x0618	CWG2DBR	7:0			DBR[5:0]					
0x0619	CWG2DBF	7:0			DBF[5:0]					
0x061A	CWG2CON0	7:0	EN	LD				MODE[2:0]		
0x061B	CWG2CON1	7:0			IN		POLD	POLC	POLB	POLA
0x061C	CWG2AS0	7:0	SHUTDOWN	REN	LSBD[1:0]		LSAC[1:0]			
0x061D	CWG2AS1	7:0			AS5E	AS4E	AS3E	AS2E	AS1E	AS0E
0x061E	CWG2STR	7:0	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA

31.15 Register Definitions: CWG Control

Long bit name prefixes for the CWG peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 31-3. CWG Bit Name Prefixes

Peripheral	Bit Name Prefix
CWG1	CWG1
CWG2	CWG2

Related Links

Long Bit Names

31.15.8 CWGxDBR

Name: CWGxDBR
Address: 0x60E,0x618

CWG Rising Dead-Band Count Register

Bit	7	6	5	4	3	2	1	0
			DBR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 5:0 – DBR[5:0] CWG Rising Edge Triggered Dead-Band Count bits
Reset States: POR/BOR = xxxxxx
All Other Resets = uuuuuu

Value	Description
n	Dead band is active no less than n, and no more than n+1, CWG clock periods after the rising edge
0	0 CWG clock periods. Dead-band generation is bypassed

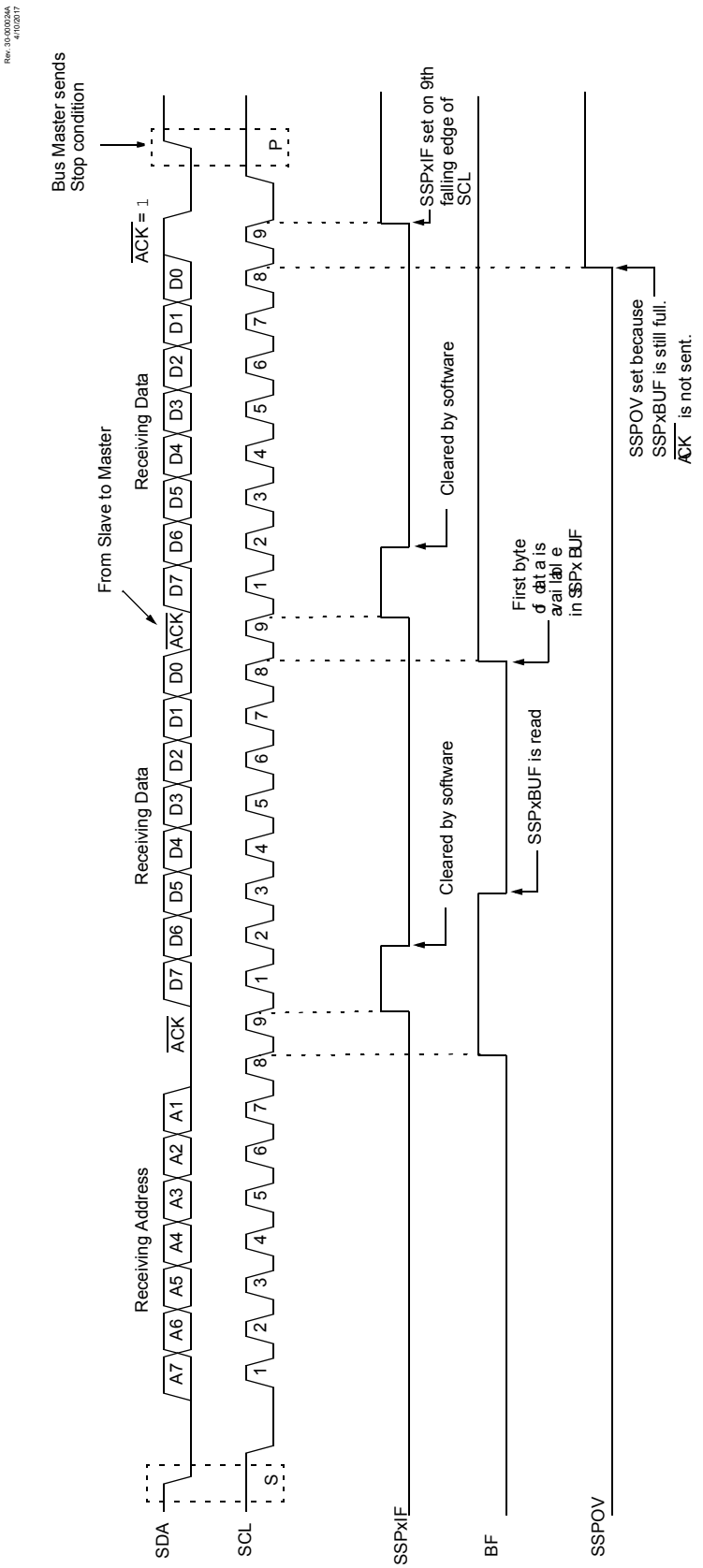
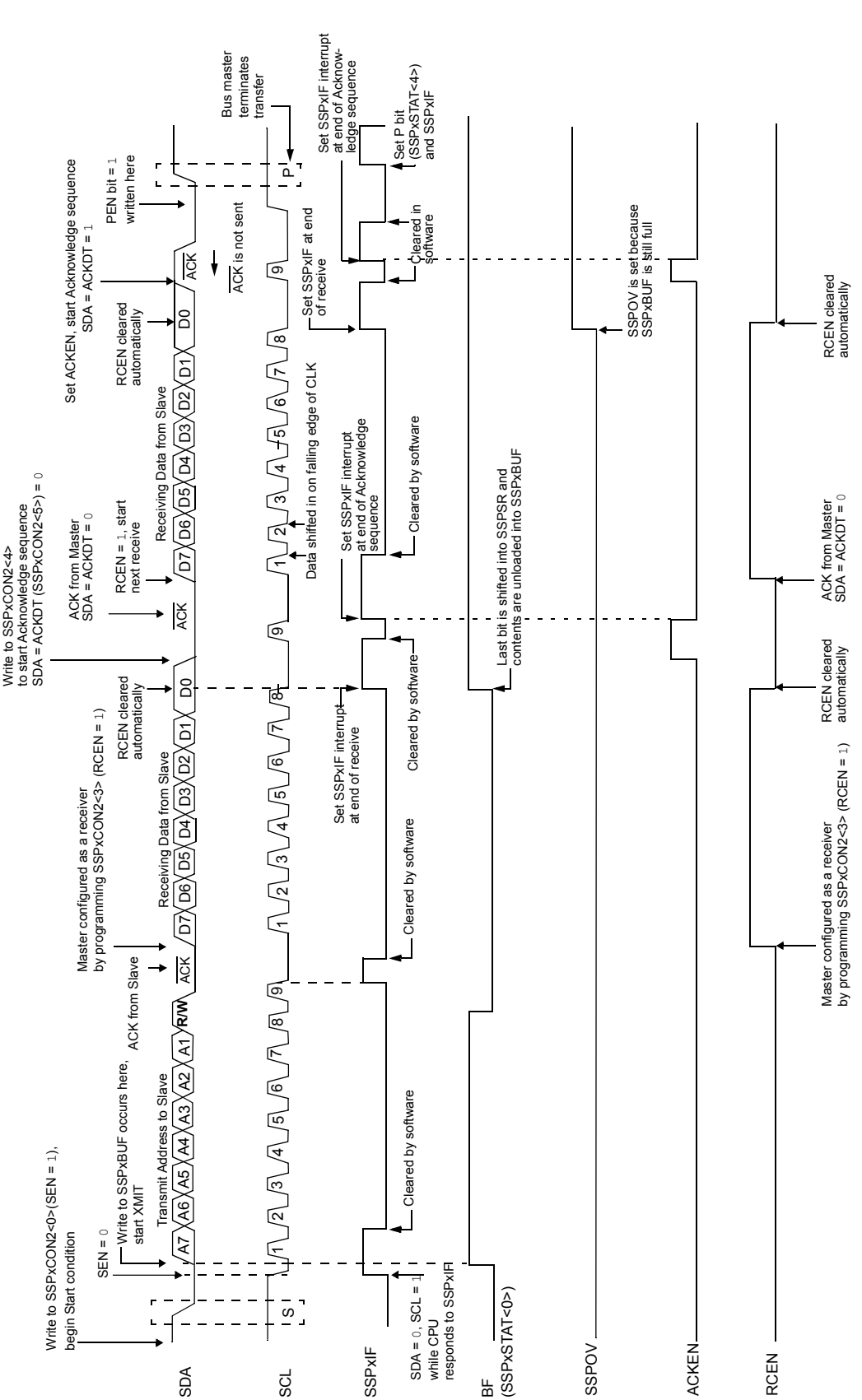


Figure 35-14. I²C Slave, 7-bit Address, Reception (SEN = 0, AHEN = 0, DHEN = 0)

Figure 35-22 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.

Figure 35-29. I²C Master Mode Waveform (Reception, 7-bit Address)



Value	Mode	Description
1	SPI	Enables the serial port. The SCKx, SDOx, SDIx, and $\overline{SSx}$ pin selections must be made with the PPS controls. Each signal must be configured with the corresponding TRIS control to the direction appropriate for the mode selected.
1	I^2C	Enables the serial port. The SDAx and SCLx pin selections must be made with the PPS controls. Since both signals are bidirectional the PPS input pin and PPS output pin selections must be made that specify the same pin. Both pins must be configured as inputs with the corresponding TRIS controls.
0	All	Disables serial port and configures these pins as I/O port pins

Bit 4 – CKP
SCK Release Control bit

Value	Mode	Description
1	SPI	Idle state for the clock is a high level
0	SPI	Idle state for the clock is a low level
1	I^2C Slave	Releases clock
0	I^2C Slave	Holds clock low (clock stretch), used to ensure data setup time
x	I^2C Master	Unused in this mode

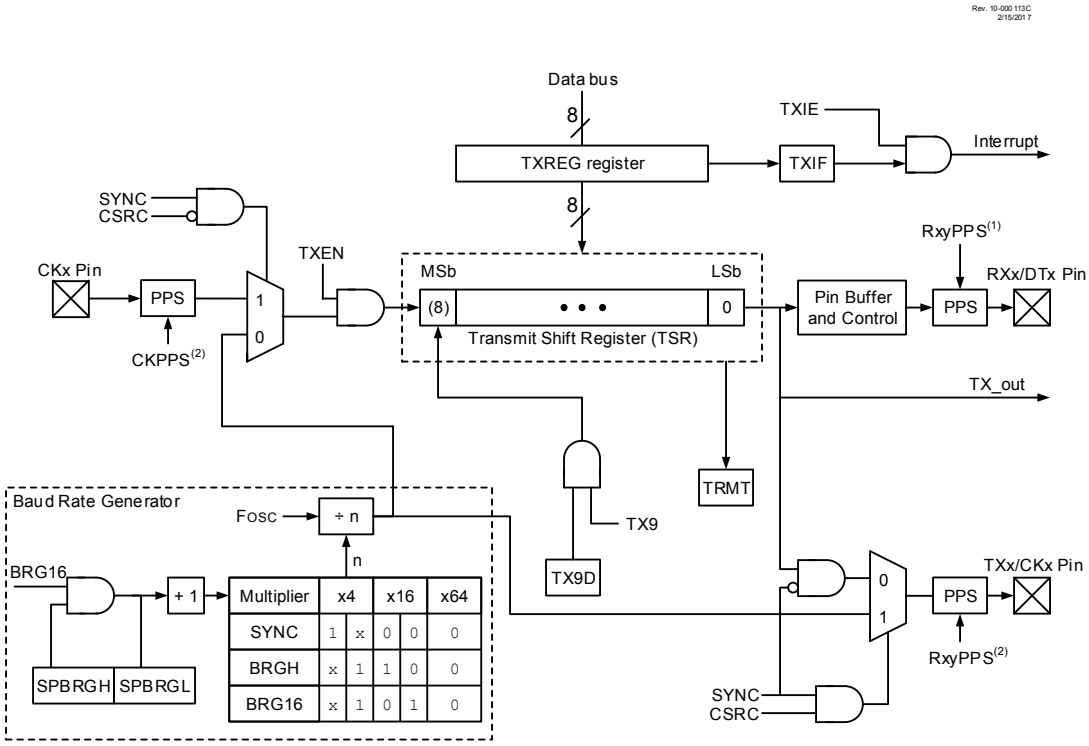
Bits 3:0 – SSPM[3:0]
Master Synchronous Serial Port Mode Select bits**(4)**

Value	Description
1111	I^2C Slave mode: 10-bit address with Start and Stop bit interrupts enabled
1110	I^2C Slave mode: 7-bit address with Start and Stop bit interrupts enabled
1101	Reserved - do not use
1100	Reserved - do not use
1011	I^2C Firmware Controlled Master mode (slave Idle)
1010	SPI Master mode: Clock = F_{OSC}/(4*(SSPxADD+1)). SSPxADD must be greater than 0.**(3)**
1001	Reserved - do not use
1000	I^2C Master mode: Clock = F_{OSC}/(4 * (SSPxADD + 1))
0111	I^2C Slave mode: 10-bit address
0110	I^2C Slave mode: 7-bit address
0101	SPI Slave mode: Clock = SCKx pin. $\overline{SSx}$ pin control is disabled
0100	SPI Slave mode: Clock = SCKx pin. $\overline{SSx}$ pin control is enabled
0011	SPI Master mode: Clock = TMR2 output/2
0010	SPI Master mode: Clock = Fosc/64
0001	SPI Master mode: Clock = Fosc/16
0000	SPI Master mode: Clock = Fosc/4

Note:

1. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.
2. When enabled, these pins must be properly configured as inputs or outputs.
3. SSPxADD = 0 is not supported.
4. Bit combinations not specifically listed here are either reserved or implemented in I^2C mode only.

Figure 36-1. EUSART Transmit Block Diagram



Note 1: In Synchronous mode, the DT output and RX input PPS selections should enable the same pin.
2: In Master Synchronous mode the TX output and CK input PPS selections should enable the same pin.

of the window input, and updates the SMTxCPR register on each rising edge of the window input after the first. See figures below.

Figure 37-20. Windowed Counter Mode, Repeat Acquisition Timing Diagram

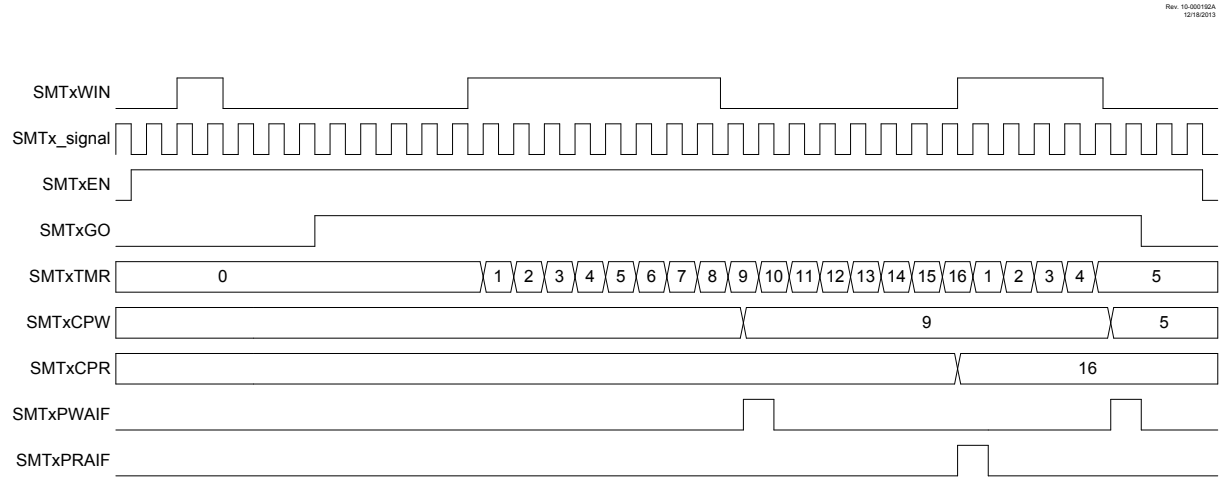
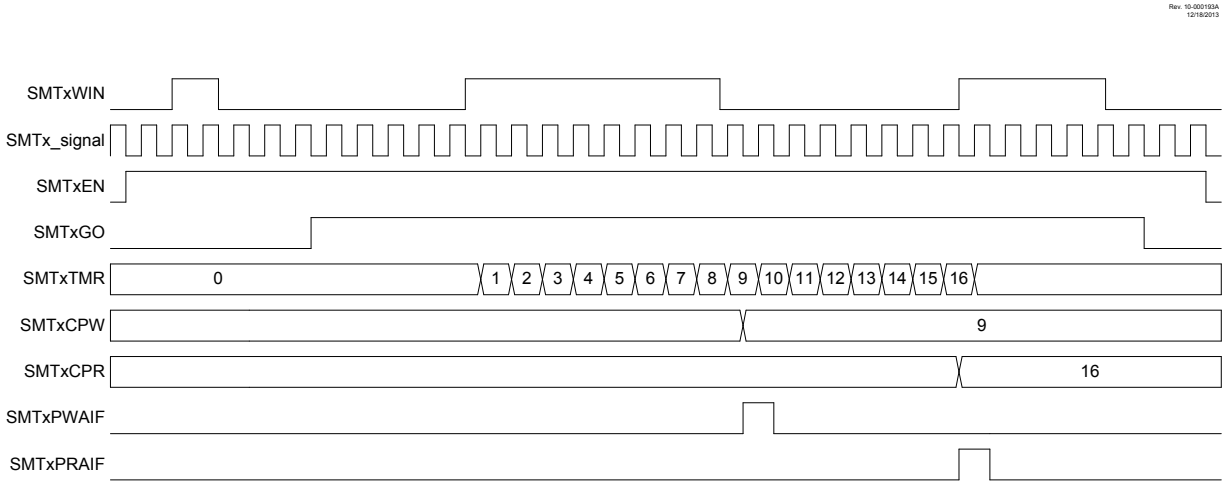


Figure 37-21. Windowed Counter Mode, Single Acquisition Timing Diagram



37.1.7 Interrupts

The SMT has three interrupts:

- **Pulse Width Acquisition Interrupt (SMTxPWAIF):** Interrupt triggers when SMTxCPW is updated
- **Period Acquisition Interrupt (SMTxPRAIF):** Interrupt triggers when SMTxCPR is updated
- **Counter Period Match Interrupt (SMTxIF):** Interrupt triggers when SMTxTMR equals SMTxPR

Each of the above interrupts can be enabled/disabled using the corresponding bits in the PIEx register.

37.1.8 Operation During Sleep

The SMT can operate during SLEEP, IDLE, and DOZE modes; provided that the clock and signal sources continue to function. System clock sources, like F_{OSC} and $F_{OSC}/4$, are disabled in Sleep.

XORLW	Exclusive OR literal with W
Syntax:	[*label*] XORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of W are XORed with the 8-bit literal ‘k’. The result is placed in W.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .XOR. (f) → dest
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

45. Revision A (12/2017)

Initial release of this document.