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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18446t-i-so

Value	Description
11	Brown-out Reset enabled, SBOREN bit is ignored
10	Brown-out Reset enabled while running, disabled in Sleep; SBOREN is ignored
01	Brown-out Reset enabled according to SBOREN
00	Brown-out Reset disabled

Bit 5 – $\overline{\text{LPBOREN}}$ Low-Power BOR Enable bit

Value	Description
1	Low-Power Brown-out Reset is disabled
0	Low-Power Brown-out Reset is enabled

Bits 2:1 – PWRTS[1:0] Power-up Timer Selection bits

Value	Description
11	PWRT disabled
10	PWRT set at 64 ms
01	PWRT set at 16 ms
00	PWRT set at 1 ms

Bit 0 – MCLRE Master Clear ($\overline{\text{MCLR}}$) Enable bit

Value	Condition	Description
	If LVP = 1	RE3 pin function is $\overline{\text{MCLR}}$ (it will reset the device when driven low)
1	If LVP = 0	$\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ (it will reset the device when driven low)
0	If LVP = 0	$\overline{\text{MCLR}}$ pin function is port defined function

Note:

1. The $\overline{\text{DEBUG}}$ bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.
2. See V_{BOR} parameter in the *"Electrical Specifications"* chapter for specific trip point voltages.

Related Links

Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-Out Reset and Low-Power Brown-Out Reset Specifications

8.14 Register Summary - BOR Control and Power Control

Offset	Name	Bit Pos.								
0x0811	BORCON	7:0	SBOREN							BORRDY
0x0812	Reserved									
0x0813	PCON0	7:0	STKOVF	STKUNF	$\overline{\text{WDTWV}}$	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
0x0814	PCON1	7:0							$\overline{\text{MEMV}}$	

8.15 Register Definitions: Power Control

9.2.1.4 4x PLL

The oscillator module contains a 4x PLL that can be used with the external clock sources to provide a system clock source. The input frequency for the PLL must fall within specifications.

The PLL can be enabled for use by one of two methods:

1. Program the RSTOSC bits in the Configuration Word 1 to '010' (enable EXTOSC with 4x PLL).
2. Write the NOSC bits to '010' (enable EXTOSC with 4x PLL).

Related Links

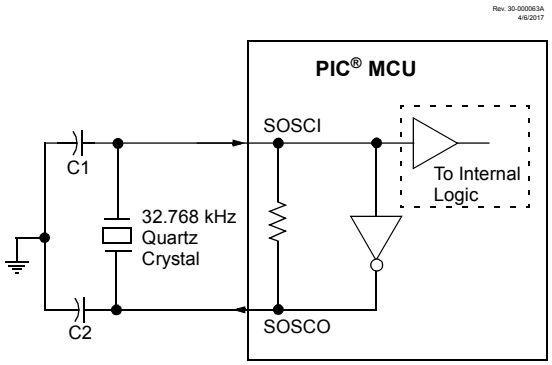
OSCCON1

PLL Specifications

9.2.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. The secondary oscillator can be selected during run-time using clock switching.

Figure 9-5. Quartz Crystal Operation (Secondary Oscillator)



Note:

1. Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
2. Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.
3. For oscillator design assistance, reference the following Microchip Application Notes:
   - AN826, *"Crystal Oscillator Basics and Crystal Selection for PIC® and PIC® Devices"* (DS00826)
   - AN849, *"Basic PIC® Oscillator Design"* (DS00849)
   - AN943, *"Practical PIC® Oscillator Analysis and Design"* (DS00943)
   - AN949, *"Making Your Oscillator Work"* (DS00949)
   - TB097, *"Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS"* (DS91097)
   - AN1288, *"Design Practices for Low-Power External Oscillators"* (DS01288)

Related Links

Clock Switching

9.4.2 Fail-Safe Operation

When the external clock fails, the FSCM overwrites the COSC bits to select HFINTOSC (3'b110). The frequency of HFINTOSC would be determined by the previous state of the HFFRQ bits and the NDIV/CDIV bits. The bit flag OSCFIF of the PIR1 register is set. Setting this flag will generate an interrupt if the OSCFIE bit of the PIE1 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation, by writing to the NOSC and NDIV bits.

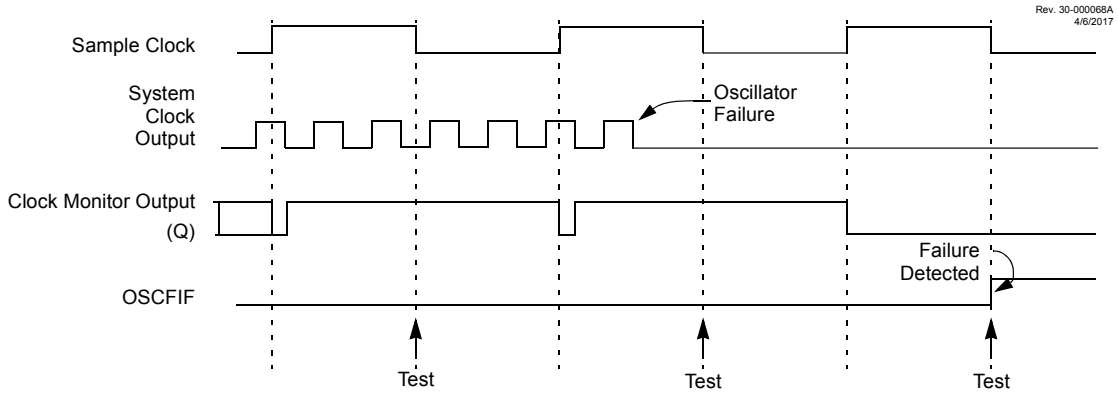
9.4.3 Fail-Safe Condition Clearing

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the NOSC and NDIV bits. When switching to the external oscillator or PLL, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON1. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSCFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSCFIF flag will again become set by hardware.

9.4.4 Reset or Wake-up from Sleep

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed.

Figure 9-10. FSCM Timing Diagram



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

CDIV/NDIV	Clock Divider
0001	2
0000	1

Note:

1. The POR value is the value present when user code execution begins.
2. The Reset value (n) is the same as the OSCCON1[NOSC/NDIV] bits.
3. EXTOSC configured by the CONFIG1[FEXTOSC] bits.
4. HFINTOSC frequency is configured with the FRQ bits of the OSCFRQ register

Related Links

CONFIG1

PLL Specifications

Value	Description
1	The PLL is ready to be used
0	The PLL is not enabled, the required input source is not ready, or the PLL is not locked.

14.6.16 ODCONA

Name: ODCONA
Address: 0x1F3A

Open-Drain Control Register

Bit	7	6	5	4	3	2	1	0
			ODCA5	ODCA4		ODCA2	ODCA1	ODCA0
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 4, 5 – ODCAn Open-Drain Configuration on RA Pins

Value	Description
1	Port pin operates as open-drain drive (sink current only)
0	Port pin operates as standard push-pull drive (source and sink current)

Bits 0, 1, 2 – ODCAn Open-Drain Configuration on RA Pins

Value	Description
1	Port pin operates as open-drain drive (sink current only)
0	Port pin operates as standard push-pull drive (source and sink current)

16.5.4 PMD3

Name: PMD3
Address: 0x799

PMD Control Register 3

Bit	7	6	5	4	3	2	1	0
		DAC1MD	ADCMD			C2MD	C1MD	ZCDMD
Access		R/W	R/W			R/W	R/W	R/W
Reset		0	0			0	0	0

Bit 6 – DAC1MD Disable DAC1 bit

Value	Description
1	DAC module disabled
0	DAC module enabled

Bit 5 – ADCMD Disable ADC bit

Value	Description
1	ADC module disabled
0	ADC module enabled

Bit 2 – C2MD Disable Comparator C2 bit

Value	Description
1	C2 module disabled
0	C2 module enabled

Bit 1 – C1MD Disable Comparator C1 bit

Value	Description
1	C1 module disabled
0	C1 module enabled

Bit 0 – ZCDMD Disable Zero-Cross Detect module bit

Value	Description
1	ZCD module disabled
0	ZCD module enabled

Table 20-3. ADC Auto-Conversion Trigger Sources

ACT	Auto-conversion Trigger Source
11111	Software write to ADPCH
11110	Reserved, do not use
11101	Software read of ADRESH
11100	Software read of ADERRH
11011 to 11000	Reserved, do not use
10111	CLC4_out
10110	CLC3_out
10101	CLC2_out
10100	CLC1_out
10011	Logical OR of all Interrupt-on-change Interrupt Flags
10010	C2_out
10001	C1_out
10000	NCO1_out
01111	PWM7_out
01110	PWM6_out
01101	CCP4_trigger
01100	CCP3_trigger
01011	CCP2_trigger
01010	CCP1_trigger
01001	SMT1_trigger
01000	TMR6_postscaled
00111	TMR5_overflow
00110	TMR4_postscaled
00101	TMR3_overflow
00100	TMR2_postscaled
00011	TMR1_overflow
00010	TMR0_overflow
00001	Pin selected by ADACTPPS
00000	External Trigger Disabled

20.2.7 ADC Conversion Procedure (Basic Mode)

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

20.8.2 ADCON1

Name: ADCON1
Address: 0x112

ADC Control Register 1

Bit	7	6	5	4	3	2	1	0
	PPOL	IPEN	GPOL					DSEN
Access	R/W	R/W	R/W					R/W
Reset	0	0	0					0

Bit 7 – PPOL Precharge Polarity bit
Action During 1st Precharge Stage

Value	Condition	Description
x	PRE=0	Bit has no effect
1	PRE>0 & ADC input is I/O pin	Pin shorted to AV_{DD}
0	PRE>0 & ADC input is I/O pin	Pin shorted to V_{SS}
1	PRE>0 & ADC input is internal	C_{HOLD} Shorted to AV_{DD}
0	PRE>0 & ADC input is internal	C_{HOLD} Shorted to V_{SS}

Bit 6 – IPEN A/D Inverted Precharge Enable bit

Value	Condition	Description
x	DSEN = 0	Bit has no effect
1	DSEN = 1	The precharge and guard signals in the second conversion cycle are the opposite polarity of the first cycle
0	DSEN = 1	Both Conversion cycles use the precharge and guards specified by PPOL and GPOL

Bit 5 – GPOL Guard Ring Polarity Selection bit

Value	Description
1	ADC guard Ring outputs start as digital high during Precharge stage
0	ADC guard Ring outputs start as digital low during Precharge stage

Bit 0 – DSEN Double-Sample Enable bit

Value	Description
1	Two conversions are performed on each trigger. Data from the first conversion appears in PREV
0	One conversion is performed for each trigger

20.8.15 ADRES

Name: ADRES
Address: 0x09D

ADC Result Register

Bit	15	14	13	12	11	10	9	8
	RESH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	RESL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 15:8 – RESH[7:0] ADC Result Register bits. High bits
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Value	Condition	Description
0x00 to 0x0F	FRM = 1	Upper 4 bits of result
0x00 to 0xFF	FRM = 0	Upper 8 bits of result

Bits 7:0 – RESL[7:0] ADC Result Register bits. Lower bits
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Value	Condition	Description
0x00 to 0xFF	FRM = 1	Lower 8 bits of result
0x00,0x10 to 0xF0	FRM = 0	Lower 4 bits of result

23.2.1 Comparator Enable

Setting the EN bit enables the comparator for operation. Clearing the CxEN bit disables the comparator, resulting in minimum current consumption.

23.2.2 Comparator Output

The output of the comparator can be monitored by reading either the CxOUT bit or the MCxOUT bit.

The comparator output can also be routed to an external pin through the RxyPPS register. The corresponding TRIS bit must be clear to enable the pin as an output.

Note:

1. The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

Related Links

RxyPPS

23.2.3 Comparator Output Polarity

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit. Clearing the CxPOL bit results in a non-inverted output.

Table 23-1 shows the output state versus input conditions, including polarity control.

Table 23-1. Comparator Output State vs. Input Conditions

Input Condition	CxPOL	CxOUT
CxVn > CxVp	0	0
CxVn < CxVp	0	1
CxVn > CxVp	1	1
CxVn < CxVp	1	0

23.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit.

See Comparator Specifications for more information.

Related Links

Comparator Specifications

23.4 Operation With Timer1 Gate

The output resulting from a comparator operation can be used as a source for gate control of the odd numbered timers (Timer1, Timer3, etc.). See the timer gate section for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to the timer by setting the SYNC bit. This ensures that the timer does not increment while a change in the comparator is occurring. However,

Important: If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

The capture source is selected by configuring the CTS bits as shown in the following table:

Table 29-2. Capture Trigger Sources

CTS	Source
111	CLC4_out
110	CLC3_out
101	CLC2_out
100	CLC1_out
011	IOC_interrupt
010	C2_out
001	C1_out
000	Pin selected by CCPxPPS

29.2.2 Timer1 Mode Resource

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See section *"Timer1 Module with Gate Control"* for more information on configuring Timer1.

Related Links

Timer1 Module with Gate Control

29.2.3 Software Interrupt Mode

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE Interrupt Priority bit of the PIEx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in Operating mode.

Important: Clocking Timer1 from the system clock (F_{OSC}) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock ($F_{OSC}/4$) or from an external clock source.

29.2.4 CCP Prescaler

There are four prescaler settings specified by the MODE bits. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. The example below demonstrates the code to perform this function.

$$T_{DEAD-BAND\_MAX} = \frac{1}{F_{CWG\_CLOCK}} \bullet DBx<5:0> + 1$$

$$T_{JITTER} = T_{DEAD-BAND\_MAX} - T_{DEAD-BAND\_MIN}$$

$$T_{JITTER} = \frac{1}{F_{CWG\_CLOCK}}$$

$$T_{DEAD-BAND\_MAX} = T_{DEAD-BAND\_MIN} + T_{JITTER}$$

Equation 31-2. Dead-Band Delay Example Calculation

$$DBx<5:0> = 0x0A = 10$$

$$F_{CWG\_CLOCK} = 8\,MHz$$

$$T_{JITTER} = \frac{1}{8\,MHz} = 125ns$$

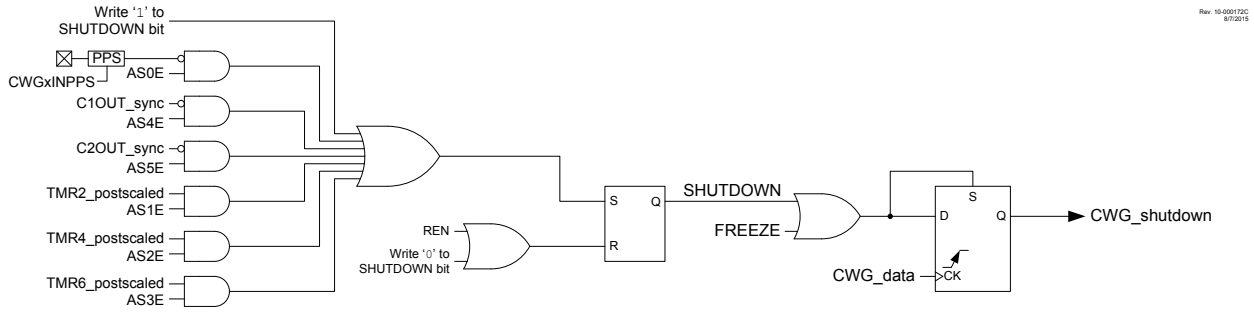
$$T_{DEAD-BAND\_MIN} = 125ns \bullet 10 = 125\mu s$$

$$T_{DEAD-BAND\_MAX} = 1.25\mu s + 0.125\,\mu s = 1.37\mu s$$

31.11 Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in the following figure.

Figure 31-16. CWG Shutdown Block Diagram



31.11.1 Shutdown

The shutdown state can be entered by either of the following two methods:

- Software generated
- External Input

31.11.1.1 Software Generated Shutdown

Setting the SHUTDOWN bit will force the CWG into the shutdown state.

When the auto-restart is disabled, the shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event. The SHUTDOWN bit indicates when a shutdown condition exists. The bit may be set or cleared in software or by hardware.

33. (CLC) Configurable Logic Cell

The Configurable Logic Cell (CLCx) module provides programmable logic that operates outside the speed limitations of software execution. The logic cell takes up to 64 input signals and, through the use of configurable gates, reduces the 64 inputs to four logic lines that drive one of eight selectable single-output logic functions.

Input sources are a combination of the following:

- I/O pins
- Internal clocks
- Peripherals
- Register bits

The output can be directed internally to peripherals and to an output pin.

Important: There are several CLC instances on this device. Throughout this section, the lower case ‘x’ in register names is a generic reference to the CLC instance number. For example, the first instance of the control register is CLC1CON and is generically described in this chapter as CLCxCON.

The following figure is a simplified diagram showing signal flow through the CLC. Possible configurations include:

- Combinatorial Logic
  - AND
  - NAND
  - AND-OR
  - AND-OR-INVERT
  - OR-XOR
  - OR-XNOR
- Latches
  - S-R
  - Clocked D with Set and Reset
  - Transparent D with Set and Reset

36.6.2 TXxSTA

Name: TXxSTA
Address: 0x011E

Transmit Status and Control Register

Bit	7	6	5	4	3	2	1	0
	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
Access	R/W	R/W	R/W	R/W	R/W	R/W	RO	R/W
Reset	0	0	0	0	0	0	1	0

Bit 7 – CSRC Clock Source Select bit

Value	Condition	Description
1	SYNC=1	Master mode (clock generated internally from BRG)
0	SYNC=1	Slave mode (clock from external source)
X	SYNC=0	Don't care

Bit 6 – TX9 9-bit Transmit Enable bit

Value	Description
1	Selects 9-bit transmission
0	Selects 8-bit transmission

Bit 5 – TXEN Transmit Enable bit
Enables transmitter(1)

Value	Description
1	Transmit enabled
0	Transmit disabled

Bit 4 – SYNC EUSART Mode Select bit

Value	Description
1	Synchronous mode
0	Asynchronous mode

Bit 3 – SENDB Send Break Character bit

Value	Condition	Description
1	SYNC=0	Send Sync Break on next transmission (cleared by hardware upon completion)
0	SYNC=0	Sync Break transmission disabled or completed
X	SYNC=1	Don't care

Bit 2 – BRGH High Baud Rate Select bit

Value	Condition	Description
1	SYNC=0	High speed, if BRG16 = 1, baud rate is baudclk/4; else baudclk/16
0	SYNC=0	Low speed
X	SYNC=1	Don't care

Offset	Name	Bit Pos.								
0x0581	INDF1	7:0	INDF1[7:0]							
0x0582	PCL	7:0	PCL[7:0]							
0x0583	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0584	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0586	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0588	BSR	7:0			BSR[5:0]					
0x0589	WREG	7:0	WREG[7:0]							
0x058A	PCLATH	7:0		PCLATH[6:0]						
0x058B	INTCON	7:0	GIE	PEIE						INTEDG
0x058C	NCO1ACC	7:0	ACCL[7:0]							
		15:8	ACCH[7:0]							
		23:16					ACCU[3:0]			
0x058F	NCO1INC	7:0	INCL[7:0]							
		15:8	INCH[7:0]							
		23:16					INCU[3:0]			
0x0592	NCO1CON	7:0	EN		OUT	POL				PFM
0x0593	NCO1CLK	7:0	PWS[2:0]				CKS[3:0]			
0x0594 ... 0x059B	Reserved									
0x059C	TMR0L	7:0	TMR0L[7:0]							
0x059D	TMR0H	7:0	TMR0H[7:0]							
0x059E	T0CON0	7:0	T0EN		T0OUT	T016BIT	T0OUTPS[3:0]			
0x059F	T0CON1	7:0	T0CS[2:0]			T0ASYNC	T0CKPS[3:0]			
0x05A0 ... 0x05FF	Reserved									
0x0600	INDF0	7:0	INDF0[7:0]							
0x0601	INDF1	7:0	INDF1[7:0]							
0x0602	PCL	7:0	PCL[7:0]							
0x0603	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0604	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0606	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0608	BSR	7:0			BSR[5:0]					
0x0609	WREG	7:0	WREG[7:0]							
0x060A	PCLATH	7:0		PCLATH[6:0]						
0x060B	INTCON	7:0	GIE	PEIE						INTEDG
0x060C	CWG1CLK	7:0								CS
0x060D	CWG1ISM	7:0					ISM[3:0]			
0x060E	CWG1DBR	7:0			DBR[5:0]					
0x060F	CWG1DBF	7:0			DBF[5:0]					
0x0610	CWG1CON0	7:0	EN	LD				MODE[2:0]		

40. Instruction Set Summary

PIC16(L)F18426/46 devices incorporate the standard set of 50 PIC16 core instructions. Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories:

- Byte Oriented
- Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 37-3 lists the instructions recognized by the MPASM™ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine entry takes two cycles (`CALL`, `CALLW`)
- Returns from interrupts or subroutines take two cycles (`RETURN`, `RETLW`, `RETFIE`)
- Program branching takes two cycles (`GOTO`, `BRA`, `BRW`, `BTFSS`, `BTFSC`, `DECFSZ`, `INCSFZ`)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format ‘`0xhh`’ to represent a hexadecimal number, where ‘`h`’ signifies a hexadecimal digit.

40.1 Read-Modify-Write Operations

Any write instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the working (W) register, or the originating file register, depending on the state of the destination designator 'd' (see the table below for more information). A read operation is performed on a register even if the instruction writes to that register.

Table 40-1. Opcode Field Descriptions

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don’t care location (= `0` or `1`). The assembler will generate code with x = `0`. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = `0`: store result in W, d = `1`: store result in file register f.

IORWF	Inclusive OR W with f
Status Affected:	Z
Description:	Inclusive OR the W register with register ‘f’. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

LSLF	Logical Left Shift
Syntax:	[*label*] LSLF f {,d}
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f<7>) → C (f<6:0>) → dest<7:1> 0 → dest<0>
Status Affected:	C, Z
Description:	The contents of register ‘f’ are shifted one bit to the left through the Carry flag. A ‘0’ is shifted into the LSb. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’. **C ← Register f ← 0**

LSRF	Logical Right Shift
Syntax:	[*label*] LSRF f {,d}
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	0 → dest<7> (f<7:1>) → dest<6:0>, (f<0>) → C
Status Affected:	C, Z
Description:	The contents of register ‘f’ are shifted one bit to the right through the Carry flag. A ‘0’ is shifted into the MSb. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’. **0 → register f → C**

42.3.2 Supply Current (I_{DD})(1,2,4)

Table 42-2.

PIC16LF18426/46 only								
Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**	
							V_{DD}	**Note**
D100	$I_{DD_{XT4}}$	XT = 4 MHz	—	530	805	µA	3.0V	
D101	$I_{DD_{HFO16}}$	HFINTOSC = 16 MHz	—	2.0	2.9	mA	3.0V	
D102	$I_{DD_{HFOPLL}}$	HFINTOSC = 32 MHz	—	3.6	5.5	mA	3.0V	
D103	$I_{DD_{HSPLL32}}$	HS+PLL = 32 MHz	—	3.6	5.6	mA	3.0V	
D104	$I_{DD_{IDLE}}$	IDLE mode, HFINTOSC = 16 MHz	—	1.6	2.0	mA	3.0V	
D105	$I_{DD_{DOZE}}$(3)	DOZE mode, HFINTOSC = 16 MHz, Doze Ratio = 16	—	1.4	—	mA	3.0V	

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins are outputs driven low; $\overline{MCLR}$ = V_{DD}; WDT disabled.
2. The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
3. $I_{DD_{DOZE}}$ = [$I_{DD_{IDLE}}$*(N-1)/N] + $I_{DD_{HFO}}$16/N where N = DOZE Ratio (see *CPUDOZE* register).
4. PMD bits are all in the default state, no modules are disabled.

PIC16F18426/46 only								
Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**	
							V_{DD}	**Note**
D100	$I_{DD_{XT4}}$	XT = 4 MHz	—	560	845	µA	3.0V	
D101	$I_{DD_{HFO16}}$	HFINTOSC = 16 MHz	—	2.2	3.0	mA	3.0V	