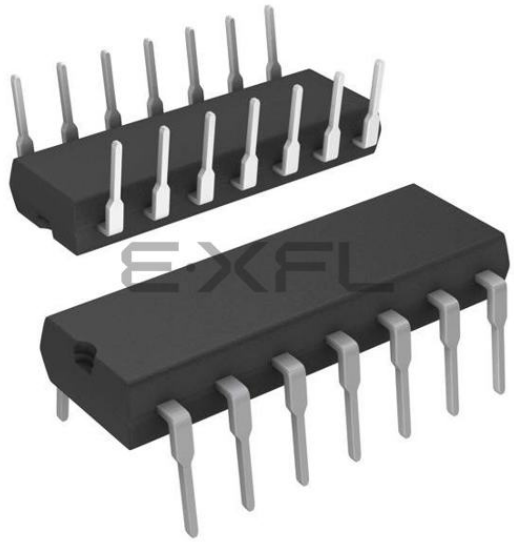

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 12 |
| Program Memory Size | 28KB (16K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 11x12b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 14-DIP (0.300", 7.62mm) |
| Supplier Device Package | 14-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18426-e-p |

## 1.2 Other Special Features

- 12-bit A/D Converter with Computation: This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead. It has a new module called ADC$^2$ with computation features, which provides a digital filter and threshold interrupt functions.
- Memory Endurance: The Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 10K for program memory and 100K for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- Self-programmability: These devices can write to their own program memory spaces under internal software control. By using a boot loader routine located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- Enhanced Peripheral Pin Select: The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections. All analog inputs and outputs remain fixed to their assigned pins.
- Windowed Watchdog Timer (WWDT):
  - Timer monitoring of overflow and underflow events
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software

## 1.3 Details on Individual Family Members

The devices of the PIC16(L)F184XX family described in the current datasheet are available in 14/20-pin packages. The block diagram for this device is shown in Figure 1-1.

The devices have the following differences:

1. Program Flash Memory
2. Data Memory SRAM
3. Data Memory EEPROM
4. A/D channels
5. I/O ports
6. Enhanced USART
7. Input Voltage Range/Power Consumption

All other features for devices in this family are identical. These are summarized in the following Device Features table.

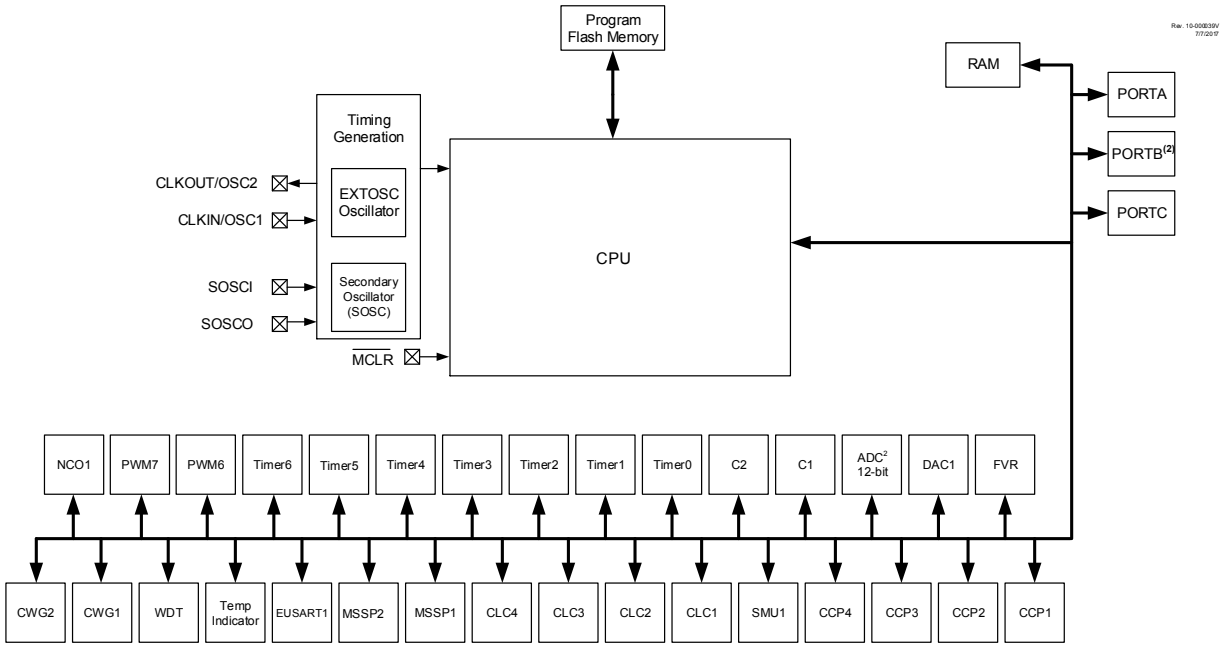
The pinouts for all devices are listed in the pin summary tables.

**Table 1-1. Device Features**

| Features | PIC16(L)F18426 | PIC16(L)F18446 |
|---|---|---|
| Program Memory (KBytes) | 28 | 28 |
| Program Memory (Instructions) | 16384 | 16384 |
| Data Memory (Bytes) | 2048 | 2048 |
| Data EEPROM Memory (Bytes) | 256 | 256 |

| Features | PIC16(L)F18426 | PIC16(L)F18446 |
|---|---|---|
| | 16-levels hardware stack | 16-levels hardware stack |
| Operating Frequency | DC – 32 MHz | DC – 32 MHz |

**Figure 1-1. PIC16(L)F18426/46 Device Block Diagram**




**Note:**

1. See applicable chapters for more information on peripherals.
2. PORTB available only on 20-pin or higher pin-count devices.

## 1.4 Register and Bit naming conventions

### 1.4.1 Register Names

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an ‘x’ in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

### 1.4.2 Bit Names

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

| Value | Description |
|---|---|
| 11 | Brown-out Reset enabled, SBOREN bit is ignored |
| 10 | Brown-out Reset enabled while running, disabled in Sleep; SBOREN is ignored |
| 01 | Brown-out Reset enabled according to SBOREN |
| 00 | Brown-out Reset disabled |

**Bit 5 – $\overline{\text{LPBOREN}}$** Low-Power BOR Enable bit

| Value | Description |
|---|---|
| 1 | Low-Power Brown-out Reset is disabled |
| 0 | Low-Power Brown-out Reset is enabled |

**Bits 2:1 – PWRTS[1:0]** Power-up Timer Selection bits

| Value | Description |
|---|---|
| 11 | PWRT disabled |
| 10 | PWRT set at 64 ms |
| 01 | PWRT set at 16 ms |
| 00 | PWRT set at 1 ms |

**Bit 0 – MCLRE** Master Clear ($\overline{\text{MCLR}}$) Enable bit

| Value | Condition | Description |
|---|---|---|
| | If LVP = 1 | RE3 pin function is $\overline{\text{MCLR}}$ (it will reset the device when driven low) |
| 1 | If LVP = 0 | $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ (it will reset the device when driven low) |
| 0 | If LVP = 0 | $\overline{\text{MCLR}}$ pin function is port defined function |

**Note:**

1. The $\overline{\text{DEBUG}}$ bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.
2. See $V_{BOR}$ parameter in the *"Electrical Specifications"* chapter for specific trip point voltages.

**Related Links**

Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-Out Reset and Low-Power Brown-Out Reset Specifications

### 7.8.12 STKPTR

**Name:** STKPTR
**Address:** 0xFED

Stack Pointer Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | STKPTR[4:0] | | | | |
| Access | | | | R/W | R/W | R/W | R/W | R/W |
| Reset | | | | 0 | 0 | 0 | 0 | 0 |

**Bits 4:0 – STKPTR[4:0]** Stack Pointer Location bits

# 14. I/O Ports

## 14.1 PORT Availability

**Table 14-1. PORT Availability Per Device**

| PORTs | PORT Description | PIC16(L)F18426 | PIC16(L)F18446 |
|---|---|---|---|
| PORTA | 6-bit wide, bidirectional port. | • | • |
| PORTB | 4-bit wide, bidirectional port. | | • |
| PORTC | 6/8-bit wide, bidirectional port. | • | • |

## 14.2 I/O Ports Description

Each port has standard registers for its operation. These registers are:

- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)
- TRISx registers (data direction)
- ANSELx registers (analog select)
- WPUx registers (weak pull-up)
- INLVLx (input level control)
- SLRCONx registers (slew rate control)
- ODCONx registers (open-drain control)

Most port pins share functions with device peripherals, both analog and digital. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output; however, the pin can still be read.

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSELx bit is set, the digital input buffer associated with that bit is disabled.

Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in the following figure:

### 17.6.7 IOCCP

**Name:** IOCCP
**Address:** 0x1F53

Interrupt-on-Change Positive Edge Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | IOCCP7 | IOCCP6 | IOCCP5 | IOCCP4 | IOCCP3 | IOCCP2 | IOCCP1 | IOCCP0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCCPn** Interrupt-on-Change Positive Edge Enable bits

| Value | Description |
|---|---|
| 1 | Interrupt-on-Change enabled on the IOCC pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge. |
| 0 | Interrupt-on-Change disabled for the associated pin. |

**Note:** IOCCP6 and IOCCP7 are available on 20-pin or higher pin-count devices only.

### 20.8.12 ADRPT

**Name:** ADRPT
**Address:** 0x09A

ADC Repeat Setting Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RPT[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7:0 – RPT[7:0]** ADC Repeat Threshold bits
Determines the number of times that the ADC is triggered for a threshold check. When ADCNT reaches this value the error threshold is checked. Used when the computation mode is Low-pass Filter, Burst Average, or Average. See Computation Modes for more details.

### 20.8.19 ADERR

**Name:** ADERR
**Address:** 0x090

ADC Setpoint Error Register

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | ERRH[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | x | x | x | x | x | x | x | x |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ADERRL[7:0] | | | | | | | |
| Access | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | x | x | x | x | x | x | x | x |

**Bits 15:8 – ERRH[7:0]**
ADC Setpoint Error MSB. Upper byte of ADC Setpoint Error calculation is determined by CALC bits.

**Bits 7:0 – ADERRL[7:0]**
ADC Setpoint Error LSB. Lower byte of ADC Setpoint Error calculation is determined by CALC bits.

### 22.9.3 NCOxACC

**Name:** NCOxACC
**Address:** 0x058C

NCO Accumulator Register

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | ACCU[3:0] | | | |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | ACCH[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ACCL[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 19:16 – ACCU[3:0]** NCO Accumulator – Upper Byte(1)

**Bits 15:8 – ACCH[7:0]** NCO Accumulator – High Byte

**Bits 7:0 – ACCL[7:0]** NCO Accumulator – Low Byte

**Note:**

1. The accumulator spans registers NCOxACCU:NCOxACCH: NCOxACCL. The 24 bits are reserved but not all are used. This register updates in real-time, asynchronously to the CPU; there is no provision to ensure atomic access to this 24-bit space using an 8-bit bus. Writing to this register while the module is operating will produce undefined results.

| T0CS | Clock Source |
|---|---|
| 001 | Pin selected by T0CKIPPS (Inverted) |
| 000 | Pin selected by T0CKIPPS (Noninverted) |

### 25.2.2 Synchronous Mode

When the T0ASYNC bit is clear, Timer0 clock is synchronized to the system clock ($F_{OSC}/4$). When operating in Synchronous mode, Timer0 clock frequency cannot exceed $F_{OSC}/4$. During Sleep mode system clock is not available and Timer0 cannot operate.

### 25.2.3 Asynchronous Mode

When the T0ASYNC bit is set, Timer0 increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows Timer0 to continue operation during Sleep mode provided the selected clock source is available.

### 25.2.4 Programmable Prescaler

Timer0 has 16 programmable input prescaler options ranging from 1:1 to 1:32768. The prescaler values are selected using the T0CKPS bits.

The prescaler counter is not directly readable or writable. The prescaler counter is cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset

**Related Links**

Resets

## 25.3 Timer0 Output and Interrupt

### 25.3.1 Programmable Postscaler

Timer0 has 16 programmable output postscaler options ranging from 1:1 to 1:16. The postscaler values are selected using the T0OUTPS bits. The postscaler divides the output of Timer0 by the selected ratio.

The postscaler counter is not directly readable or writable. The postscaler counter is cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset

### 25.3.2 Timer0 Output

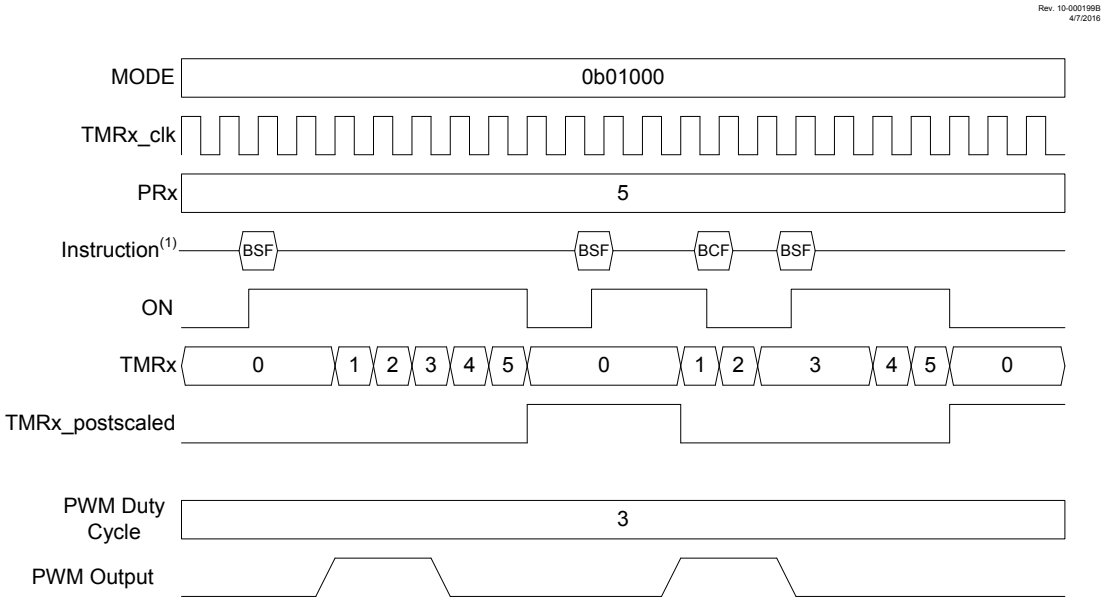
TMR0_out is the output of the postscaler. TMR0_out toggles on every match between TMR0L and TMR0H in 8-bit mode, or when TMR0H:TMR0L rolls over in 16-bit mode. If the output postscaler is used, the output is scaled by the ratio selected.

The Timer0 output can be routed to an I/O pin via the RxyPPS output selection register. The Timer0 output can be monitored through software via the T0OUT output bit.

**Related Links**

| Mode | MODE<4:0> | | Output Operation | Operation | Timer Control | | |
|---|---|---|---|---|---|---|---|
| | <4:3> | <2:0> | | | Start | Reset | Stop |
| | | 100 | Edge Triggered Start and Hardware Reset (Note 1) | Rising edge start and Rising edge Reset (Figure 27-9) | ON = 1 and TMRx_ers ↑ | TMRx_ers ↑ | |
| | | 101 | | Falling edge start and Falling edge Reset | ON = 1 and TMRx_ers ↓ | TMRx_ers ↓ | |
| | | 110 | | Rising edge start and Low level Reset (Figure 27-10) | ON = 1 and TMRx_ers ↑ | TMRx_ers = 0 | |
| | | 111 | | Falling edge start and High level Reset | ON = 1 and TMRx_ers ↓ | TMRx_ers = 1 | |
| Mono-stable | 10 | 000 | Reserved | | | | |
| | | 001 | Edge Triggered Start (Note 1) | Rising edge start (Figure 27-11) | ON = 1 and TMRx_ers ↑ | — | ON = 0 or Next clock after TMRx = PRx (Note 3) |
| | | 010 | | Falling edge start | ON = 1 and TMRx_ers ↓ | — | |
| | | 011 | | Any edge start | ON = 1 and TMRx_ers ↕ | — | |
| Reserved | | 100 | Reserved | | | | |
| Reserved | | 101 | Reserved | | | | |
| One-shot | | 110 | Level Triggered Start and Hardware Reset | High level start and Low level Reset (Figure 27-12) | ON = 1 and TMRx_ers = 1 | TMRx_ers = 0 | ON = 0 or Held in Reset (Note 2) |
| | | 111 | | Low level start & High level Reset | ON = 1 and TMRx_ers = 0 | TMRx_ers = 1 | |

**Figure 27-7. Software Start One-shot Mode Timing Diagram (MODE = 01000)**




**Note:**

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

**Related Links**

PWM Overview

(PWM) Pulse-Width Modulation

### 27.6.6 Edge-Triggered One-Shot Mode

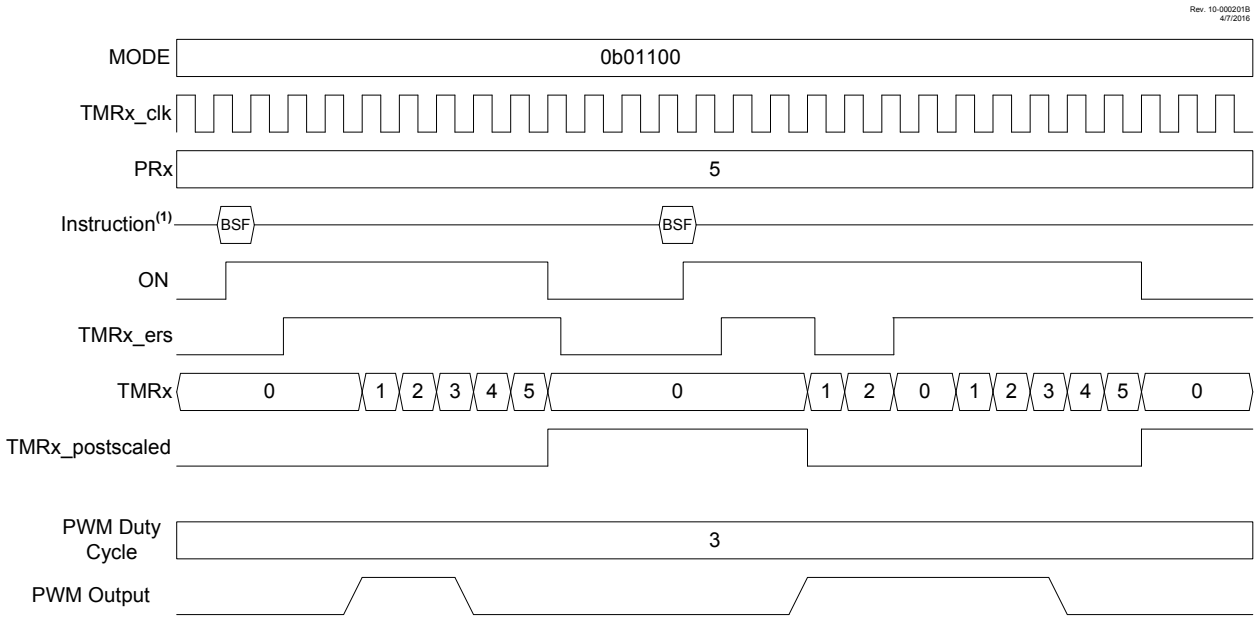
The Edge-Triggered One-Shot modes start the timer on an edge from the external signal input, after the ON bit is set, and clear the ON bit when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 01001)
- Falling edge (MODE<4:0> = 01010)
- Rising or Falling edge (MODE<4:0> = 01011)

If the timer is halted by clearing the ON bit then another TMRx_ers edge is required after the ON bit is set to resume counting. Figure 27-8 illustrates operation in the rising edge One-Shot mode.

When Edge-Triggered One-Shot mode is used in conjunction with the CCP then the edge-trigger will activate the PWM drive and the PWM drive will deactivate when the timer matches the CCPRx pulse width value and stay deactivated when the timer halts at the PRx period count match.

**Figure 27-9. Edge-Triggered Hardware Limit One-Shot Mode Timing Diagram (MODE = 01100)**




**Note:**

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

**Related Links**

PWM Overview

(PWM) Pulse-Width Modulation

### 27.6.8 Level Reset, Edge-Triggered Hardware Limit One-Shot Modes

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = 01110)
- High Reset level (MODE<4:0> = 01111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control, a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation, the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

### 27.9.4 TxHLT

**Name:** TxHLT
**Address:** 0x28F,0x295,0x29B

Timer Hardware Limit Control Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PSYNC | CPOL | CSYNC | MODE[4:0] | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7 – PSYNC**
Timer Prescaler Synchronization Enable bit(1, 2)

| Value | Description |
|---|---|
| 1 | Timer Prescaler Output is synchronized to $F_{OSC}/4$ |
| 0 | Timer Prescaler Output is not synchronized to $F_{OSC}/4$ |

**Bit 6 – CPOL**
Timer Clock Polarity Selection bit(3)

| Value | Description |
|---|---|
| 1 | Falling edge of input clock clocks timer/prescaler |
| 0 | Rising edge of input clock clocks timer/prescaler |

**Bit 5 – CSYNC**
Timer Clock Synchronization Enable bit(4, 5)

| Value | Description |
|---|---|
| 1 | ON bit is synchronized to timer clock input |
| 0 | ON bit is not synchronized to timer clock input |

**Bits 4:0 – MODE[4:0]**
Timer Control Mode Selection bits(6, 7)

| Value | Description |
|---|---|
| 00000 to 11111 | See Table 27-3 |

**Note:**

1. Setting this bit ensures that reading TxTMR will return a valid data value.
2. When this bit is '1', Timer cannot operate in Sleep mode.
3. CKPOL should not be changed while ON = 1.
4. Setting this bit ensures glitch-free operation when the ON is enabled or disabled.
5. When this bit is set then the timer operation will be delayed by two input clocks after the ON bit is set.
6. Unless otherwise indicated, all modes start upon ON = 1 and stop upon ON = 0 (stops occur without affecting the value of TxTMR).

**Changing Between Capture Prescalers**

```
BANKSEL CCP1CON         ;(only needed when CCP1CON is not in ACCESS space)
CLRF    CCP1CON         ;Turn CCP module off
MOVLW   NEW_CAPT_PS     ;CCP ON and Prescaler select → W
MOVWF   CCP1CON         ;Load CCP1CON with this value
```

### 29.2.5 Capture During Sleep

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock ($F_{OSC}/4$), or by an external clock source.

When Timer1 is clocked by $F_{OSC}/4$, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

Capture mode will operate during Sleep when Timer1 is clocked by an external clock source.

## 29.3 Compare Mode

The Compare mode function described in this section is available and identical for all CCP modules.

Compare mode makes use of the 16-bit odd numbered Timer resources (Timer1, Timer3, etc.). The 16-bit value of the CCPRx register is constantly compared against the 16-bit value of the TMRx register. When a match occurs, one of the following events can occur:

- Toggle the CCPx output and clear TMRx
- Toggle the CCPx output without clearing TMRx
- Set the CCPx output
- Clear the CCPx output
- Pulse output
- Pulse output and clear TMRx

The action on the pin is based on the value of the MODE control bits. At the same time, the interrupt flag CCPxIF bit is set, and an ADC conversion can be triggered, if selected.

All Compare modes can generate an interrupt and trigger an ADC conversion. When MODE = `'0001'` or `'1011'`, the CCP resets the TMRx register.

The following figure shows a simplified diagram of the compare operation.

**Table 30-1. Example PWM Frequencies and Resolutions (Fosc = 20 MHz)**

| PWM Frequency | 0.31 kHz | 4.88 kHz | 19.53 kHz | 78.12 kHz | 156.3 kHz | 208.3 kHz |
|---|---|---|---|---|---|---|
| Timer Prescale | 64 | 4 | 1 | 1 | 1 | 1 |
| T2PR Value | 0xFF | 0xFF | 0xFF | 0x3F | 0x1F | 0x17 |
| Maximum Resolution (bits) | 10 | 10 | 10 | 8 | 7 | 6.6 |

**Table 30-2. Example PWM Frequencies and Resolutions (Fosc = 8 MHz)**

| PWM Frequency | 0.31 kHz | 4.90 kHz | 19.61 kHz | 76.92 kHz | 153.85 kHz | 200.0 kHz |
|---|---|---|---|---|---|---|
| Timer Prescale | 64 | 4 | 1 | 1 | 1 | 1 |
| T2PR Value | 0x65 | 0x65 | 0x65 | 0x19 | 0x0C | 0x09 |
| Maximum Resolution (bits) | 8 | 8 | 8 | 6 | 5 | 5 |

## 30.6 Operation in Sleep Mode

In Sleep mode, the T2TMR register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, T2TMR will continue from its previous state.

## 30.7 Changes in System Clock Frequency

The PWM frequency is derived from the system clock frequency ($F_{OSC}$). Any changes in the system clock frequency will result in changes to the PWM frequency.

**Related Links**

Oscillator Module (with Fail-Safe Clock Monitor)

## 30.8 Effects of Reset

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.

## 30.9 Setup for PWM Operation using PWMx Output Pins

The following steps should be taken when configuring the module for PWM operation using the PWMx pins:

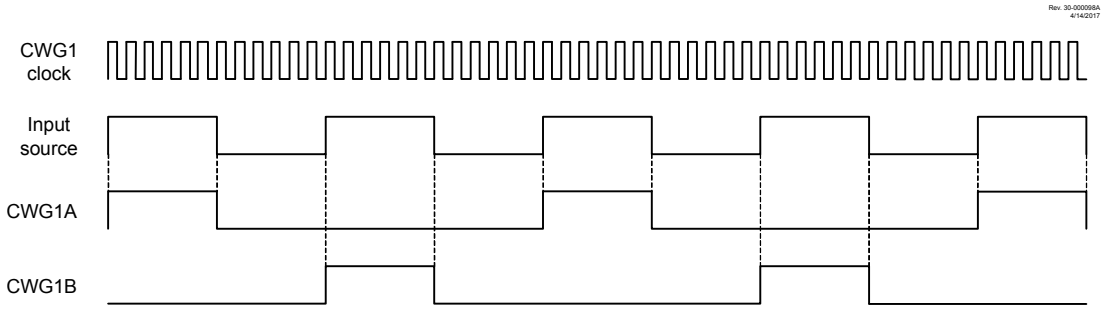
1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the T2PR register with the PWM period value.
4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIRx register.(1)
   - Select the timer clock source to be as $F_{OSC}/4$ using the TxCLKCON register. This is required for correct operation of the PWM module.

power supply designs. Steering modes are not used in Push-Pull mode. A basic block diagram for the Push-Pull mode is shown in Figure 31-4.

The push-pull sequencer is reset whenever EN = 0 or if an auto-shutdown event occurs. The sequencer is clocked by the first input pulse, and the first output appears on CWG1A.

The unused outputs CWGxC and CWGxD drive copies of CWGxA and CWGxB, respectively, but with polarity controlled by the POLC and POLD bits of the CWGxCON1 register, respectively.

**Figure 31-3. CWG Push-Pull Mode Operation**



| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x180C ... 0x187F | Reserved | | | | | | | | | |
| 0x1880 | INDF0 | 7:0 | INDF0[7:0] | | | | | | | |
| 0x1881 | INDF1 | 7:0 | INDF1[7:0] | | | | | | | |
| 0x1882 | PCL | 7:0 | PCL[7:0] | | | | | | | |
| 0x1883 | STATUS | 7:0 | | | | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| 0x1884 | FSR0 | 7:0 | FSRL[7:0] | | | | | | | |
| | | 15:8 | FSRH[7:0] | | | | | | | |
| 0x1886 | FSR1 | 7:0 | FSRL[7:0] | | | | | | | |
| | | 15:8 | FSRH[7:0] | | | | | | | |
| 0x1888 | BSR | 7:0 | | | BSR[5:0] | | | | | |
| 0x1889 | WREG | 7:0 | WREG[7:0] | | | | | | | |
| 0x188A | PCLATH | 7:0 | | PCLATH[6:0] | | | | | | |
| 0x188B | INTCON | 7:0 | GIE | PEIE | | | | | | INTEDG |
| 0x188C ... 0x18FF | Reserved | | | | | | | | | |
| 0x1900 | INDF0 | 7:0 | INDF0[7:0] | | | | | | | |
| 0x1901 | INDF1 | 7:0 | INDF1[7:0] | | | | | | | |
| 0x1902 | PCL | 7:0 | PCL[7:0] | | | | | | | |
| 0x1903 | STATUS | 7:0 | | | | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| 0x1904 | FSR0 | 7:0 | FSRL[7:0] | | | | | | | |
| | | 15:8 | FSRH[7:0] | | | | | | | |
| 0x1906 | FSR1 | 7:0 | FSRL[7:0] | | | | | | | |
| | | 15:8 | FSRH[7:0] | | | | | | | |
| 0x1908 | BSR | 7:0 | | | BSR[5:0] | | | | | |
| 0x1909 | WREG | 7:0 | WREG[7:0] | | | | | | | |
| 0x190A | PCLATH | 7:0 | | PCLATH[6:0] | | | | | | |
| 0x190B | INTCON | 7:0 | GIE | PEIE | | | | | | INTEDG |
| 0x190C ... 0x197F | Reserved | | | | | | | | | |
| 0x1980 | INDF0 | 7:0 | INDF0[7:0] | | | | | | | |
| 0x1981 | INDF1 | 7:0 | INDF1[7:0] | | | | | | | |
| 0x1982 | PCL | 7:0 | PCL[7:0] | | | | | | | |
| 0x1983 | STATUS | 7:0 | | | | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| 0x1984 | FSR0 | 7:0 | FSRL[7:0] | | | | | | | |
| | | 15:8 | FSRH[7:0] | | | | | | | |
| 0x1986 | FSR1 | 7:0 | FSRL[7:0] | | | | | | | |
| | | 15:8 | FSRH[7:0] | | | | | | | |
| 0x1988 | BSR | 7:0 | | | BSR[5:0] | | | | | |
| 0x1989 | WREG | 7:0 | WREG[7:0] | | | | | | | |
| 0x198A | PCLATH | 7:0 | | PCLATH[6:0] | | | | | | |
| 0x198B | INTCON | 7:0 | GIE | PEIE | | | | | | INTEDG |
| 0x198C | Reserved | | | | | | | | | |

| PIC16LF18426/46 only | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | |
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.†** | **Max.** | **Units** | **Conditions** |
| D003 | $V_{DR}$ | | 1.5 | — | — | V | Device in Sleep mode |
| **Power-on Reset Release Voltage(2)** | | | | | | | |
| D004 | $V_{POR}$ | | — | 1.6 | — | V | BOR or LPBOR disabled(3) |
| **Power-on Reset Rearm Voltage(2)** | | | | | | | |
| D005 | $V_{PORR}$ | | — | 0.8 | — | V | BOR or LPBOR disabled(3) |
| **$V_{DD}$ Rise Rate to ensure internal Power-on Reset signal(2)** | | | | | | | |
| D006 | $S_{VDD}$ | | 0.05 | — | — | V/ms | BOR or LPBOR disabled(3) |

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

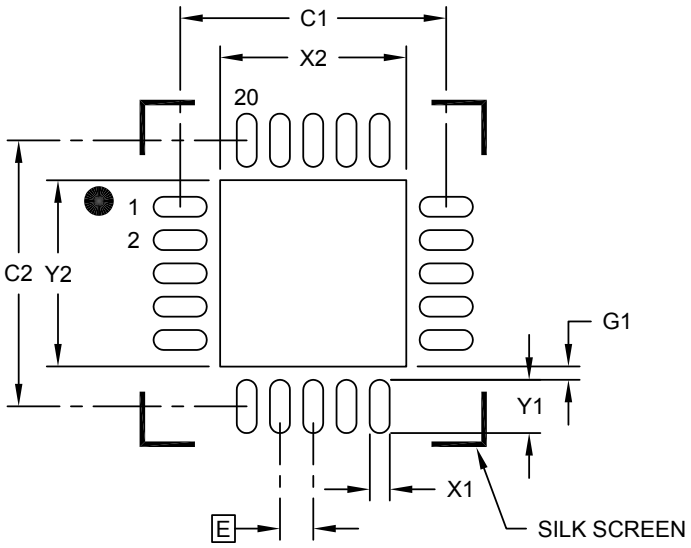
**Note:**

1. This is the limit to which $V_{DD}$ can be lowered in Sleep mode without losing RAM data.
2. See the following figure, POR and POR REARM with Slow Rising $V_{DD}$.
3. Please see Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-Out Reset and Low-Power Brown-Out Reset Specifications for BOR and LPBOR trip point information.

| PIC16F18426/46 only | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Standard Operating Conditions (unless otherwise stated)** | | | | | | | |
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.†** | **Max.** | **Units** | **Conditions** |
| **Supply Voltage** | | | | | | | |
| D002 | $V_{DD}$ | | 2.3 | — | 5.5 | V | $F_{OSC}$ ≤ 16 MHz |
| | | | 2.5 | — | 5.5 | V | $F_{OSC}$ > 16 MHz |
| **RAM Data Retention(1)** | | | | | | | |
| D003 | $V_{DR}$ | | 1.7 | — | — | V | Device in Sleep mode |
| **Power-on Reset Release Voltage(2)** | | | | | | | |
| D004 | $V_{POR}$ | | — | 1.6 | — | V | BOR or LPBOR disabled(3) |
| **Power-on Reset Rearm Voltage(2)** | | | | | | | |

### 20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 2.80 |
| Optional Center Pad Length | Y2 | | | 2.80 |
| Contact Pad Spacing | C1 | | 4.00 | |
| Contact Pad Spacing | C2 | | 4.00 | |
| Contact Pad Width (X20) | X1 | | | 0.30 |
| Contact Pad Length (X20) | Y1 | | | 0.80 |
| Contact Pad to Center Pad (X20) | G1 | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2255A