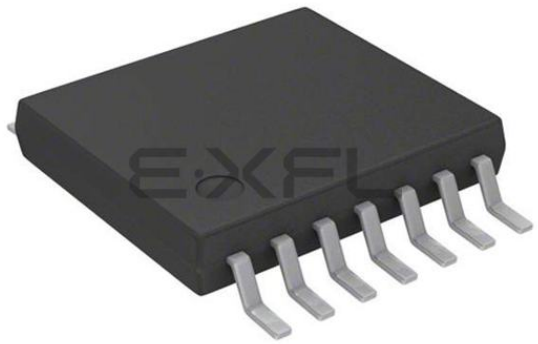

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18426-e-st

7.9 Register Summary: Shadow Registers

Offset	Name	Bit Pos.								
0x1FE4	STATUS_SHAD	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x1FE5	WREG_SHAD	7:0	WREG[7:0]							
0x1FE6	BSR_SHAD	7:0			BSR[5:0]					
0x1FE7	PCLATH_SHAD	7:0		PCLATH[6:0]						
0x1FE8	FSR0_SHAD	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x1FEA	FSR1_SHAD	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							

7.10 Register Definitions: Shadow Registers

- Write of Program Flash Memory write latches to program memory
- Write of Program Flash Memory write latches to User IDs
- Write to EEPROM

The unlock sequence consists of the following steps and must be completed in order:

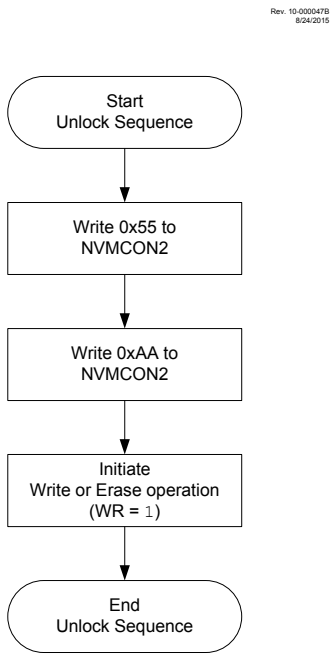
- Write 55h to NVMCON2
- Write AAh to NMVCON2
- Set the WR bit of NVMCON1

Once the WR bit is set, the processor will stall internal operations until the operation is complete and then resume with the next instruction.

Important: The two `NOP` instructions after setting the WR bit that were required in previous devices are not required for PIC16(L)F184XX devices. See figure below.

Since the unlock sequence must not be interrupted, global interrupts should be disabled prior to the unlock sequence and re-enabled after the unlock sequence is completed.

Figure 13-2. NVM Unlock Sequence Flowchart



NVM Unlock Sequence

```
BCF      INTCON, GIE       ; Recommended so sequence is not interrupted
BANKSEL  NVMCON1           ;
BSF      NVMCON1, WREN     ; Enable write/erase
MOVLW    55h               ; Load 55h
MOVWF    NVMCON2           ; Step 1: Load 55h into NVMCON2
MOVLW    AAh               ; Step 2: Load W with AAh
MOVWF    NVMCON2           ; Step 3: Load AAH into NVMCON2
```

14.6.4 TRISA

Name: TRISA
Address: 0x012

Tri-State Control Register

Bit	7	6	5	4	3	2	1	0
			TRISA5	TRISA4		TRISA2	TRISA1	TRISA0
Access			R/W	R/W	RO	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 4, 5 – TRISAx TRISA Port I/O Tri-state Control bits

Value	Description
1	PORTA pin configured as an input (tri-stated)
0	PORTA pin configured as an output

Bits 0, 1, 2 – TRISAn TRISA Port I/O Tri-state Control bits

Value	Description
1	PORTA pin configured as an input (tri-stated)
0	PORTA pin configured as an output

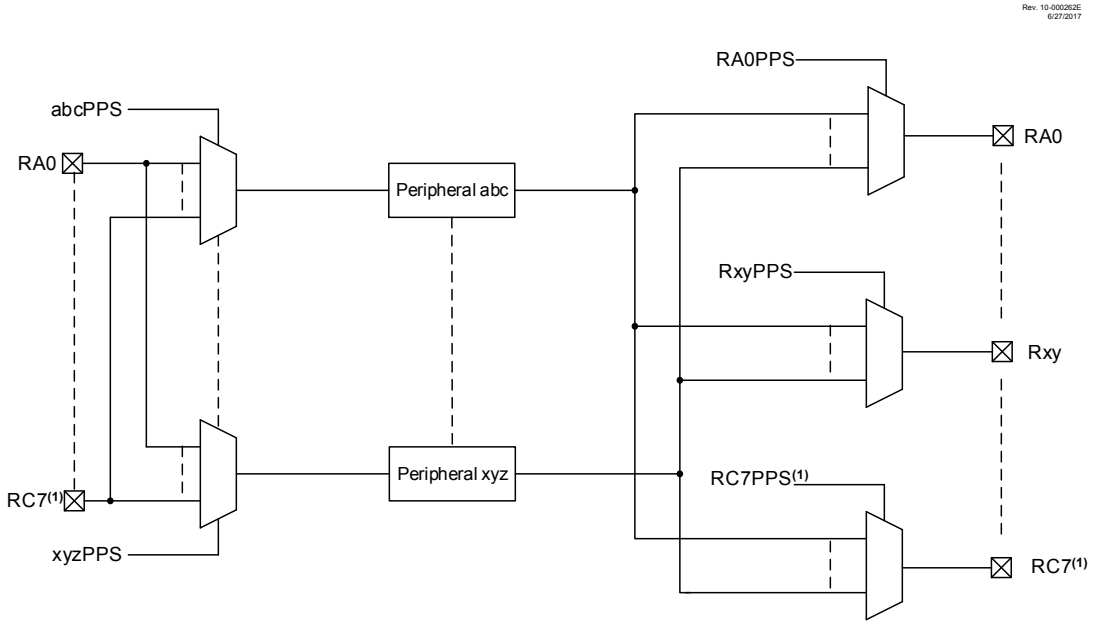
Note: Bits TRISA0 and TRISA1 are read-only when $\overline{\text{DEBUG}}$ is enabled, and will read '1'.

15. (PPS) Peripheral Pin Select Module

The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections.

All analog inputs and outputs remain fixed to their assigned pins. Input and output selections are independent as shown in the figure below.

Figure 15-1. Simplified PPS Block Diagram



Note:

1. Not present on 14-pin devices.

15.1 PPS Inputs

Each peripheral has an xxxPPS register with which the input pin to the peripheral is selected. Not all ports are available for input as shown in the following table.

Multiple peripherals can operate from the same source simultaneously. Port reads always return the pin level regardless of peripheral PPS selection. If a pin also has analog functions associated, the ANSEL bit for that pin must be cleared to enable the digital input buffer.

Important: The notation “xxx” in the generic register name is a place holder for the peripheral identifier. For example, xxx = INT for the INTPPS register.

```
    BCF      PPSLOCK,PPSLOCKED
; restore interrupts
    BSF      INTCON,GIE
```

Note:

1. The PPSLOCK bit can only be set or cleared after the unlock sequence shown above.
2. If PPS1WAY = 1, the PPSLOCK bit cannot be cleared after it has been set.

15.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

Related Links

PPSLOCK

15.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

15.7 Effects of a Reset

A device Power-on-Reset (POR) clears all PPS input and output selections to their default values. All other Resets leave the selections unchanged. Default input selections are shown in the input selection register table. The PPS one-way is also removed.

15.9.2 Pin Rxy Output Source Selection Register

Name: RxyPPS

Important: See Register Summary - PPS for the address offset of each individual register.

Bit	7	6	5	4	3	2	1	0
			RxyPPS[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – RxyPPS[5:0] Pin Rxy Output Source Selection bits
See output source selection table for source codes.

Value	Description
01	ADC FVR Buffer Gain is 1x, (1.024V)
00	ADC FVR Buffer is off

Note:

1. FVRRDY is always '1'.
2. Fixed Voltage Reference output cannot exceed V_{DD}.
3. See *"Temperature Indicator Module"* section for additional information

Related Links

Temperature Indicator Module

INTCON register must be cleared. If all three of these bits are set, the execution will switch to the Interrupt Service Routine.

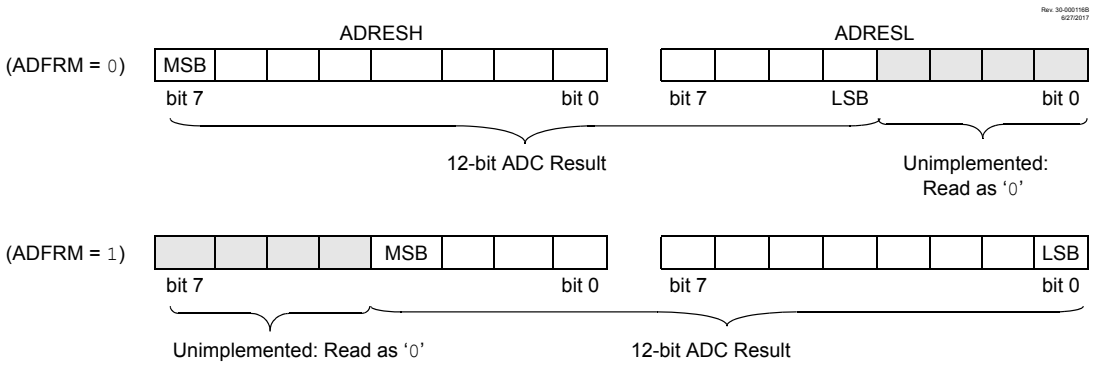
20.1.6 Result Formatting

The 12-bit ADC conversion result can be supplied in two formats, left justified or right justified. The FRM bit controls the output format.

The figure below shows the two output formats.

Writes to the ADRES register pair are always right justified regardless of the selected format mode. Therefore, data read after writing to ADRES when FRM = 0 will be shifted left four places.

Figure 20-3. 12-Bit ADC Conversion Result Format



20.2 ADC Operation

20.2.1 Starting a Conversion

To enable the ADC module, the ON bit must be set to a '1'. A conversion may be started by any of the following:

- Software setting the GO bit to '1'
- An external trigger (source selected by ADCON2)
- A continuous-mode retrigger (see *"Continuous Sampling mode"* section.)

.

Important: The GO bit should not be set in the same instruction that turns on the ADC.

Related Links

ADC Conversion Procedure (Basic Mode)
Continuous Sampling Mode
ADCON0
ADCON2

20.8.3 ADCON2

Name: ADCON2
Address: 0x113

ADC Control Register 2

Bit	7	6	5	4	3	2	1	0
	PSIS	CRS[2:0]			ACLR	MD[2:0]		
Access	R/W	R/W	R/W	R/W	R/W/HC	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – PSIS ADC Previous Sample Input Select bits

Value	Description
1	FLTR is transferred to PREV at start-of-conversion
0	ADRES is transferred to PREV at start-of-conversion

Bits 6:4 – CRS[2:0] ADC Accumulated Calculation Right Shift Select bits

Value	Condition	Description
0 to 7	MD = b'100'	Low-pass filter time constant is 2^{CRS}, filter gain is 1:1
0 to 7	MD = b'011' to b'001'	The accumulated value is right-shifted by CRS (divided by 2^{CRS})**(1,2)**
x	MD = b'000' to b'001'	These bits are ignored

Bit 3 – ACLR A/D Accumulator Clear Command bit**(3)**

Value	Description
1	ACC, AOV and CNT registers are cleared
0	Clearing action is complete (or not started)

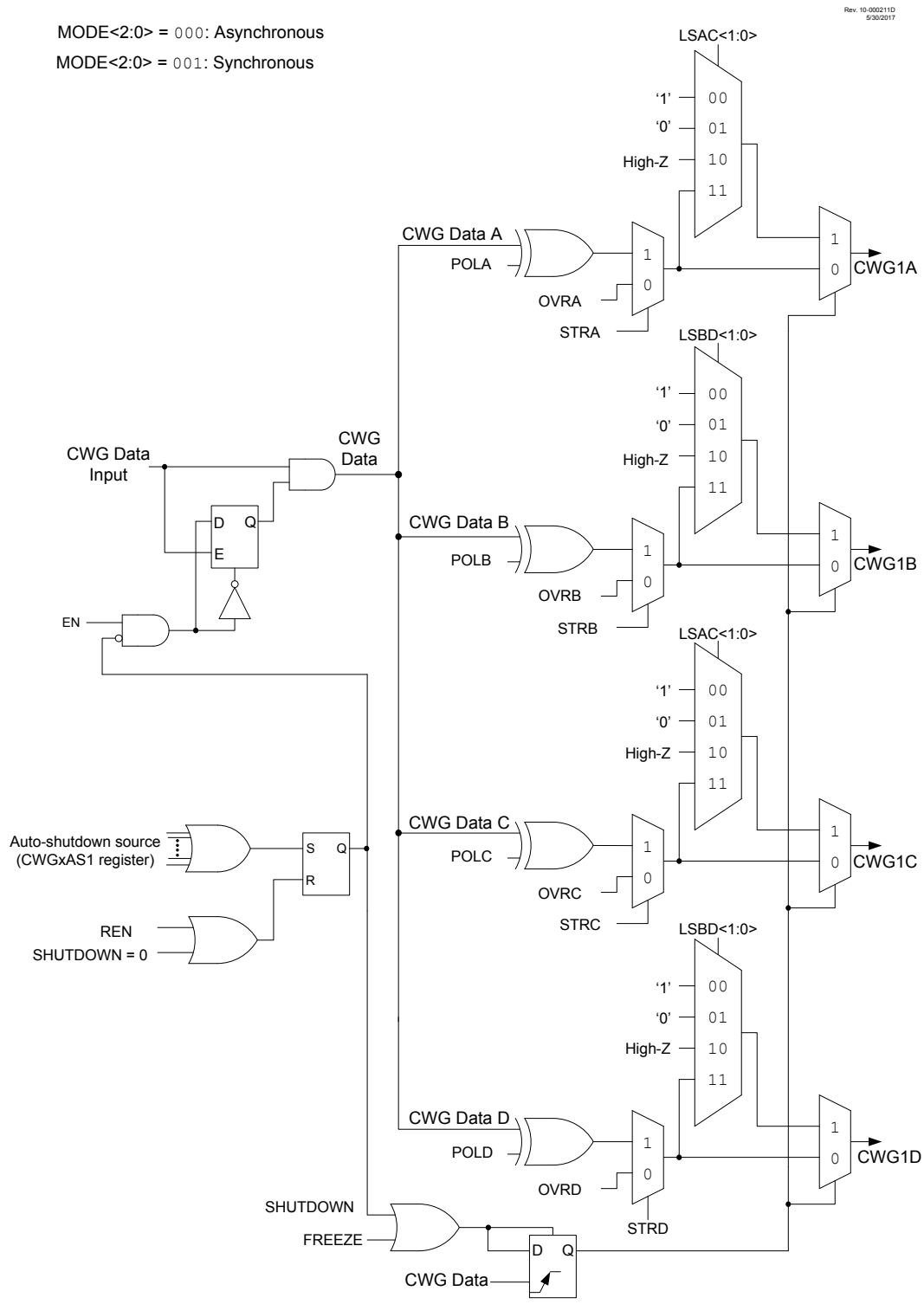
Bits 2:0 – MD[2:0] ADC Operating Mode Selection bits**(4)**

Value	Description
111-101	Reserved
100	Low-pass Filter mode
011	Burst Average mode
010	Average mode
001	Accumulate mode
000	Basic (Legacy) mode

Note:

1. To correctly calculate an average, the number of samples (set in RPT) must be 2^{CRS}.
2. CRS = `3'b111` is a reserved option.
3. This bit is cleared by hardware when the accumulator operation is complete; depending on oscillator selections, the delay may be many instructions.
4. See Computation Modes for Full mode descriptions.

Figure 31-9. Simplified CWG Block Diagram (Output Steering Modes)



For example, when STRA = 0 then the corresponding pin is held at the level defined by OVRA. When STRA = 1, then the pin is driven by the modulated input signal.

The POLy bits control the signal polarity only when STRy = 1.

the Baud Rate Generator is turned off until another write to the SSPxBUF takes place, holding SCL low and allowing SDA to float.

35.6.6.1 BF Status Flag

In Transmit mode, the BF bit is set when the CPU writes to SSPxBUF and is cleared when all eight bits are shifted out.

35.6.6.2 WCOL Status Flag

If the user writes the SSPxBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

The WCOL bit must be cleared by software before the next transmission.

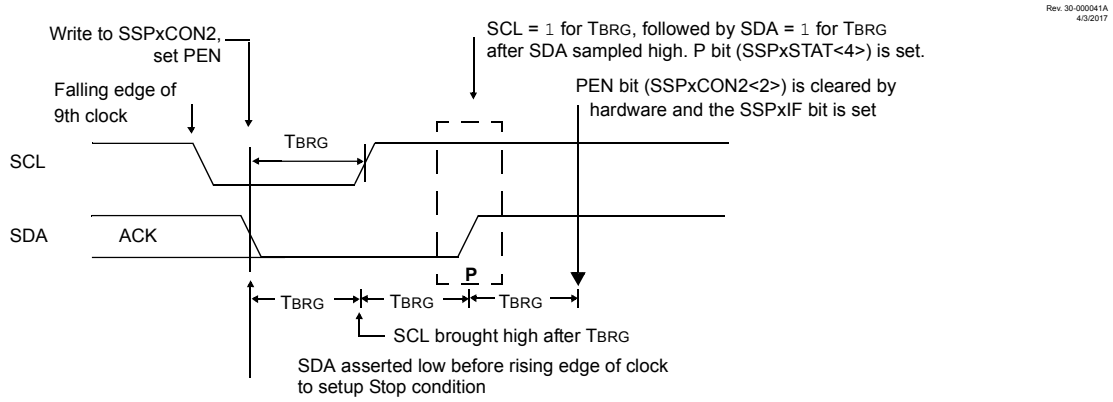
35.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit is cleared when the slave has sent an Acknowledge ($\overline{ACK}$ = 0) and is set when the slave does not Acknowledge ($\overline{ACK}$ = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

35.6.6.4 Typical transmit sequence:

1. The user generates a Start condition by setting the SEN bit.
2. SSPxIF is set by hardware on completion of the Start.
3. SSPxIF is cleared by software.
4. The MSSP module will wait the required start time before any other operation takes place.
5. The user loads the SSPxBUF with the slave address to transmit.
6. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
7. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit.
8. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
9. The user loads the SSPxBUF with eight bits of data.
10. Data is shifted out the SDA pin until all eight bits are transmitted.
11. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit.
12. Steps 8-11 are repeated for all transmitted data bytes.
13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits. Interrupt is generated once the Stop/Restart condition is complete.

Figure 35-31. Stop Condition in Receive or Transmit Mode



Note: TBRG = one Baud Rate Generator period.

35.6.9.1 Write Collision on Stop

If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

35.6.10 Sleep Operation

While in Sleep mode, the I^2C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

35.6.11 Effects of a Reset

A Reset disables the MSSP module and terminates the current transfer.

35.6.12 Multi-Master Mode

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLxIF bit.

The states where arbitration can be lost are:

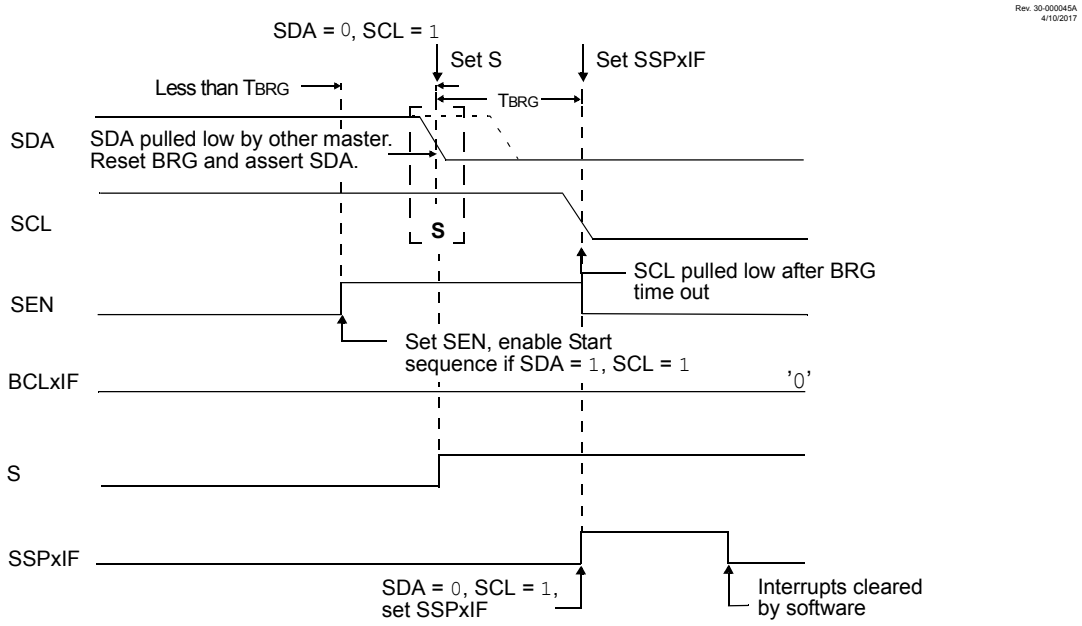
- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

35.6.13 Multi -Master Communication, Bus Collision and Bus Arbitration

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLxIF and reset the I^2C port to its Idle state (Figure 35-32).

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 35-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Figure 35-35. BRG Reset Due to SDA Arbitration During Start Condition



Important: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

35.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

1. A low level is sampled on SDA when SCL goes from low level to high level (Case 1).
2. SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 35-36). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—

36.2.1 Auto-Baud Detect

The EUSART module supports automatic detection and calibration of the baud rate.

In the Auto-Baud Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII “U”) which is the Sync character for the LIN bus. The unique feature of this character is that it has five rising edges including the Stop bit edge.

Setting the ABDEN bit of the BAUDxCON register starts the auto-baud calibration sequence. While the ABD sequence takes place, the EUSART state machine is held in Idle. On the first rising edge of the receive line, after the Start bit, the SPxBRG begins counting up using the BRG counter clock as shown in Figure 36-7. The fifth rising edge will occur on the RXx pin at the end of the eighth bit period. At that time, an accumulated value totaling the proper BRG period is left in the SPxBRGH, SPxBRGL register pair, the ABDEN bit is automatically cleared and the RCxIF interrupt flag is set. The value in the RCxREG needs to be read to clear the RCxIF interrupt. RCxREG content should be discarded. When calibrating for modes that do not use the SPxBRGH register the user can verify that the SPxBRGL register did not overflow by checking for 00h in the SPxBRGH register.

The BRG auto-baud clock is determined by the BRG16 and BRGH bits as shown in Table 36-3. During ABD, both the SPxBRGH and SPxBRGL registers are used as a 16-bit counter, independent of the BRG16 bit setting. While calibrating the baud rate period, the SPxBRGH and SPxBRGL registers are clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed.

Note:

37.3.8 SMTxCPR

Name: SMTxCPR
Address: 0x048F

SMT Captured Period Register

Bit	23	22	21	20	19	18	17	16
	CPRU[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bit	15	14	13	12	11	10	9	8
	CPRH[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	CPRL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	x	x	x	x	x	x	x	x

Bits 23:16 – CPRU[7:0] Upper byte of SMT capture period register
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Bits 15:8 – CPRH[7:0] High byte of SMT capture period register
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Bits 7:0 – CPRL[7:0] Lower byte of SMT capture period register
Reset States: POR/BOR = xxxxxxxx
All Other Resets = uuuuuuuu

Offset	Name	Bit Pos.								
0x0581	INDF1	7:0	INDF1[7:0]							
0x0582	PCL	7:0	PCL[7:0]							
0x0583	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0584	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0586	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0588	BSR	7:0			BSR[5:0]					
0x0589	WREG	7:0	WREG[7:0]							
0x058A	PCLATH	7:0		PCLATH[6:0]						
0x058B	INTCON	7:0	GIE	PEIE						INTEDG
0x058C	NCO1ACC	7:0	ACCL[7:0]							
		15:8	ACCH[7:0]							
		23:16					ACCU[3:0]			
0x058F	NCO1INC	7:0	INCL[7:0]							
		15:8	INCH[7:0]							
		23:16					INCU[3:0]			
0x0592	NCO1CON	7:0	EN		OUT	POL				PFM
0x0593	NCO1CLK	7:0	PWS[2:0]				CKS[3:0]			
0x0594 ... 0x059B	Reserved									
0x059C	TMR0L	7:0	TMR0L[7:0]							
0x059D	TMR0H	7:0	TMR0H[7:0]							
0x059E	T0CON0	7:0	T0EN		T0OUT	T016BIT	T0OUTPS[3:0]			
0x059F	T0CON1	7:0	T0CS[2:0]			T0ASYNC	T0CKPS[3:0]			
0x05A0 ... 0x05FF	Reserved									
0x0600	INDF0	7:0	INDF0[7:0]							
0x0601	INDF1	7:0	INDF1[7:0]							
0x0602	PCL	7:0	PCL[7:0]							
0x0603	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x0604	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0606	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x0608	BSR	7:0			BSR[5:0]					
0x0609	WREG	7:0	WREG[7:0]							
0x060A	PCLATH	7:0		PCLATH[6:0]						
0x060B	INTCON	7:0	GIE	PEIE						INTEDG
0x060C	CWG1CLK	7:0								CS
0x060D	CWG1ISM	7:0					ISM[3:0]			
0x060E	CWG1DBR	7:0			DBR[5:0]					
0x060F	CWG1DBF	7:0			DBF[5:0]					
0x0610	CWG1CON0	7:0	EN	LD				MODE[2:0]		

Offset	Name	Bit Pos.								
0x1E10	CLC1CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E11	CLC1POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E12	CLC1SEL0	7:0			D1S[5:0]					
0x1E13	CLC1SEL1	7:0			D2S[5:0]					
0x1E14	CLC1SEL2	7:0			D3S[5:0]					
0x1E15	CLC1SEL3	7:0			D4S[5:0]					
0x1E16	CLC1GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E17	CLC1GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E18	CLC1GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E19	CLC1GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E1A	CLC2CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E1B	CLC2POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E1C	CLC2SEL0	7:0			D1S[5:0]					
0x1E1D	CLC2SEL1	7:0			D2S[5:0]					
0x1E1E	CLC2SEL2	7:0			D3S[5:0]					
0x1E1F	CLC2SEL3	7:0			D4S[5:0]					
0x1E20	CLC2GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E21	CLC2GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E22	CLC2GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E23	CLC2GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E24	CLC3CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E25	CLC3POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E26	CLC3SEL0	7:0			D1S[5:0]					
0x1E27	CLC3SEL1	7:0			D2S[5:0]					
0x1E28	CLC3SEL2	7:0			D3S[5:0]					
0x1E29	CLC3SEL3	7:0			D4S[5:0]					
0x1E2A	CLC3GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E2B	CLC3GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E2C	CLC3GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E2D	CLC3GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E2E	CLC4CON	7:0	EN		OUT	INTP	INTN	MODE[2:0]		
0x1E2F	CLC4POL	7:0	POL				G4POL	G3POL	G2POL	G1POL
0x1E30	CLC4SEL0	7:0			D1S[5:0]					
0x1E31	CLC4SEL1	7:0			D2S[5:0]					
0x1E32	CLC4SEL2	7:0			D3S[5:0]					
0x1E33	CLC4SEL3	7:0			D4S[5:0]					
0x1E34	CLC4GLS0	7:0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
0x1E35	CLC4GLS1	7:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
0x1E36	CLC4GLS2	7:0	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
0x1E37	CLC4GLS3	7:0	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
0x1E38 ... 0x1E7F	Reserved									
0x1E80	INDF0	7:0	INDF0[7:0]							
0x1E81	INDF1	7:0	INDF1[7:0]							
0x1E82	PCL	7:0	PCL[7:0]							

42. Electrical Specifications

42.1 Absolute Maximum Ratings(†)

Parameter		Rating
Ambient temperature under bias		-40°C to +125°C
Storage temperature		-65°C to +150°C
Voltage on pins with respect to V_{SS}		
• **on V_{DD} pin:**		
	PIC16LF18426/46	-0.3V to +4.0V
	PIC16F18426/46	-0.3V to +6.5V
• **on $\overline{MCLR}$ pin:**		-0.3V to +9.0V
• **on all other pins:**		-0.3V to (V_{DD} + 0.3V)
Maximum current		
• **on V_{SS} pin(1)**	-40°C ≤ T_A ≤ +85°C	250 mA
	85°C < T_A ≤ +125°C	120 mA
• **on V_{DD} pin(1)**	-40°C ≤ T_A ≤ +85°C	250 mA
	85°C < T_A ≤ +125°C	85 mA
• **on any standard I/O pin**		±50 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD})		±20 mA
Total power dissipation(2)		800 mW

Important:

1. Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Thermal Characteristics to calculate device specifications.
2. Power dissipation is calculated as follows:
   $P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma (V_{OI} \times I_{OL})$

NOTICE: Stresses above those listed under *"Absolute Maximum Ratings"* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

42.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \le V_{DD} \le V_{DDMAX}$

42.4.13 Timer0 and Timer1 External Clock Requirements

Table 42-19.

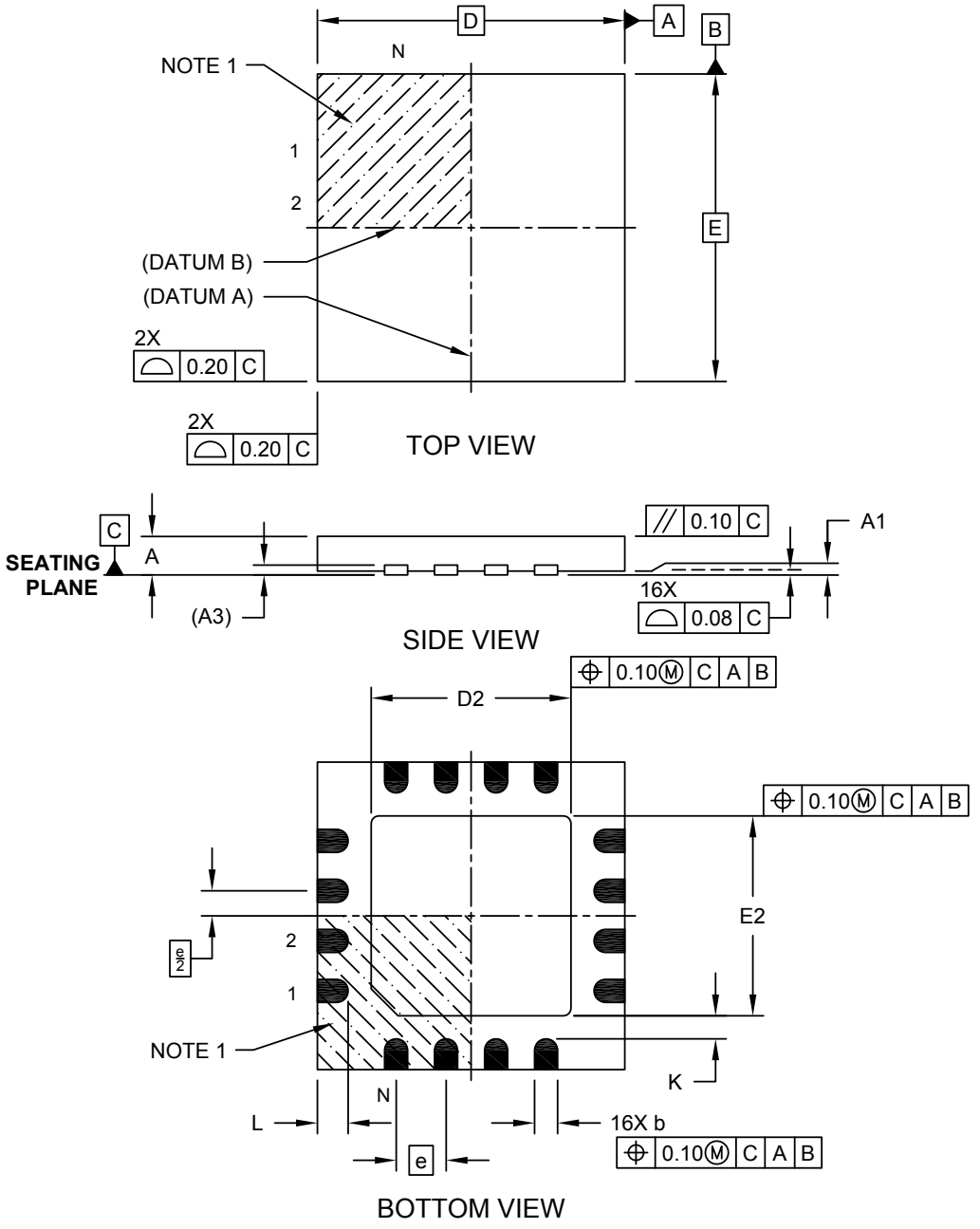
Standard Operating Conditions (unless otherwise stated) Operating Temperature: -40°C≤T_A≤+125°C								
Param No.	**Sym.**	**Characteristic**		**Min.**	**Typ. †**	**Max.**	**Units**	**Conditions**
40*	T_T0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY}$ +20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	T_T0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY}$ +20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	T_T0P	T0CKI Period		Greater of: 20 or (T_{CY} +40)/N	—	—	ns	N = Prescale value
45*	T_T1H	T1CKI High Time	Synchronous, No Prescaler	$0.5T_{CY}$ +20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	T_T1L	T1CKI Low Time	Synchronous, No Prescaler	$0.5T_{CY}$ +20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	T_T1P	T1CKI Input Period	Synchronous	Greater of: 30 or (T_{CY} +40)/N	—	—	ns	N = Prescale value
			Asynchronous	60	—	—	ns	
49*	$TCKEZ_{TMR}1$	Delay from External Clock Edge to Timer Increment		2 T_{OSC}	—	7 T_{OSC}	—	Timers in Sync mode

* - These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-257A Sheet 1 of 2