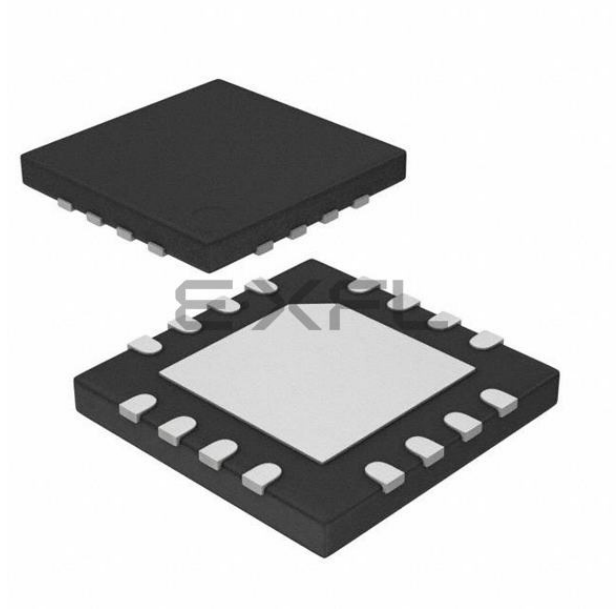

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18426-i-jq

7.8.4 STATUS

Name: STATUS
Address: 0x03 + n*0x80 [n=0..63]

Status Register

Bit	7	6	5	4	3	2	1	0
				$\overline{TO}$	$\overline{PD}$	Z	DC	C
Access				RO	RO	R/W	R/W	R/W
Reset				1	1	0	0	0

Bit 4 – $\overline{TO}$ Time-Out bit
Reset States: POR/BOR = 1
All Other Resets = q

Value	Description
1	Set at power-up or by execution of `CLRWDT` or `SLEEP` instruction
0	A WDT time-out occurred

Bit 3 – $\overline{PD}$ Power-Down bit
Reset States: POR/BOR = 1
All Other Resets = q

Value	Description
1	Set at power-up or by execution of `CLRWDT` instruction
0	Cleared by execution of the `SLEEP` instruction

Bit 2 – Z Zero bit
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	The result of an arithmetic or logic operation is zero
0	The result of an arithmetic or logic operation is not zero

Bit 1 – DC Digit Carry/$\overline{Borrow}$ bit(1)
`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions
Reset States: POR/BOR = 0
All Other Resets = u

Value	Description
1	A carry-out from the 4th low-order bit of the result occurred
0	No carry-out from the 4th low-order bit of the result

Bit 0 – C Carry/$\overline{Borrow}$ bit(1)
`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions
Reset States: POR/BOR = 0
All Other Resets = u

7.8.5 FSR0

Name: FSR0
Address: 0x04 + n*0x80 [n=0..63]

Indirect Address Register. The FSR value is the address of the data to which the INDF register points.

Bit	15	14	13	12	11	10	9	8
	FSRH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FSRL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – FSRH[7:0]
Most significant address of INDF data

Bits 7:0 – FSRL[7:0]
Least significant address of INDF data

Related Links
Core Registers

Important: An internal Reset event (RESET instruction, BOR, WWDT, POR, STKOVF, STKUNF) does not drive the $\overline{MCLR}$ pin low.

Related Links
Master Clear (MCLR) Pin

8.4.2 $\overline{MCLR}$ Disabled

When $\overline{MCLR}$ is disabled, the $\overline{MCLR}$ becomes input-only and pin functions such as internal weak pull-ups are under software control.

Related Links
I/O Priorities

8.5 Windowed Watchdog Timer (WWDT) Reset

The Windowed Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period or window set. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register and the $\overline{RWDT}$ bit are changed to indicate a WDT Reset. The $\overline{WDTWV}$ bit indicates if the WDT Reset has occurred due to a timeout or a window violation.

Related Links
STATUS
(WWDT) Windowed Watchdog Timer

8.6 RESET Instruction

A RESET instruction will cause a device Reset. The $\overline{RI}$ bit will be set to '0'. See *"Reset Condition for Special Registers"* table for default conditions after a RESET instruction has occurred.

8.7 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words.

Related Links
CONFIG2
Overflow/Underflow Reset

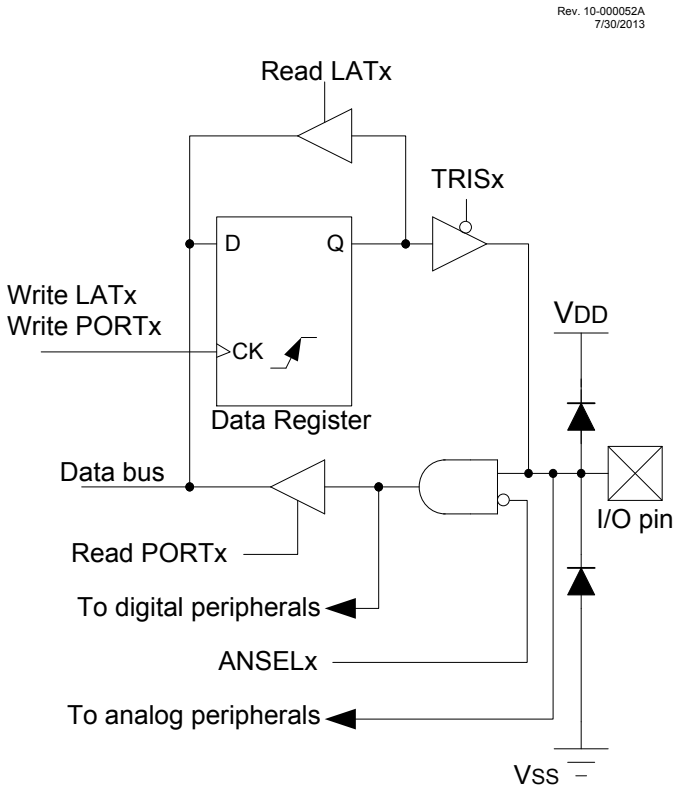
8.8 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

8.9 Power-up Timer (PWRT)

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow V_{DD} to stabilize before allowing the device to start running.

Figure 14-1. Generic I/O Port Operation



14.3 I/O Priorities

Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See *"Peripheral Pin Select (PPS) Module"* for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over digital outputs and force the digital output driver into a high-impedance state.

The pin function priorities are as follows:

1. Configuration bits
2. Analog outputs (disable the input buffers)
3. Analog inputs
4. Port inputs and outputs from PPS

Related Links

(PPS) Peripheral Pin Select Module

14.4 PORTx Registers

In this section the generic names such as PORTx, LATx, TRISx, etc. can be associated with PORTA, PORTB, PORTC, etc, depending on availability per device (see related link below).

Related Links

PORT Availability

14.4.1 Data Register

PORTx is a bidirectional port, and its corresponding data direction register is TRISx. Setting a TRISx bit (‘1’) will make the corresponding PORTx pin an input (i.e., disable the output driver). Clearing a TRISx bit (‘0’) will make the corresponding PORTx pin an output (i.e., it enables output driver and puts the contents of the output latch on the selected pin). The example below shows how to initialize PORTA.

Reading the PORTx register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATx).

The PORT data latch LATx holds the output port data and contains the latest value of a LATx or PORTx write.

EXAMPLE-1: Initializing PORTA

```
; This code example illustrates initializing the PORTA register.
; The other ports are initialized in the same manner.

    BANKSEL    PORTA        ;
    CLRF       PORTA        ;Init PORTA
    BANKSEL    LATA         ;Data Latch
    CLRF       LATA         ;
    BANKSEL    ANSELA       ;
    CLRF       ANSELA       ;digital I/O
    BANKSEL    TRISA        ;
    MOVLW      B'00111000'  ;Set RA<5:3> as inputs
    MOVWF      TRISA        ;and set RA<2:0> as outputs
```

Related Links

PORTA

TRISA

LATA

14.4.2 Direction Control

The TRISx register controls the PORTx pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISx register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

14.4.3 Open-Drain Control

The ODCONx register controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONx bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONx bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Important: It is not necessary to set open-drain control when using the pin for I^2C; the I^2C module controls the pin and makes the pin open-drain.

14.4.4 Slew Rate Control

The SLRCONx register controls the slew rate option for each port pin. Slew rate for each port pin can be controlled independently. When an SLRCONx bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONx bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

14.4.5 Input Threshold Control

The INLVLx register controls the input voltage threshold for each of the available PORTx input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTx register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See link below for more information on threshold levels.

Important: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

14.4.6 Analog Control

The ANSELx register is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELx bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELx bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Important: The ANSELx bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.4.7 Weak Pull-up Control

The WPUx register controls the individual weak pull-ups for each port pin.

14.4.8 PORTx Functions and Output Priorities

Each PORTx pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic, or by enabling an analog output, such as the DAC. See the link below for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

Related Links

(PPS) Peripheral Pin Select Module

15.9.3 PPS Lock Register

Name: PPSLOCK
Address: 0x1E8F

Bit	7	6	5	4	3	2	1	0
								PPSLOCKED
Access								R/W
Reset								0

Bit 0 – PPSLOCKED PPS Locked bit

Value	Description
1	PPS is locked. PPS selections can not be changed.
0	PPS is not locked. PPS selections can be changed.

25.6.3 TMR0H

Name: TMR0H
Address: 0x59D

Timer0 Period/Count High Register

Bit	7	6	5	4	3	2	1	0
	TMR0H[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TMR0H[7:0] TMR0 Most Significant Counter bits

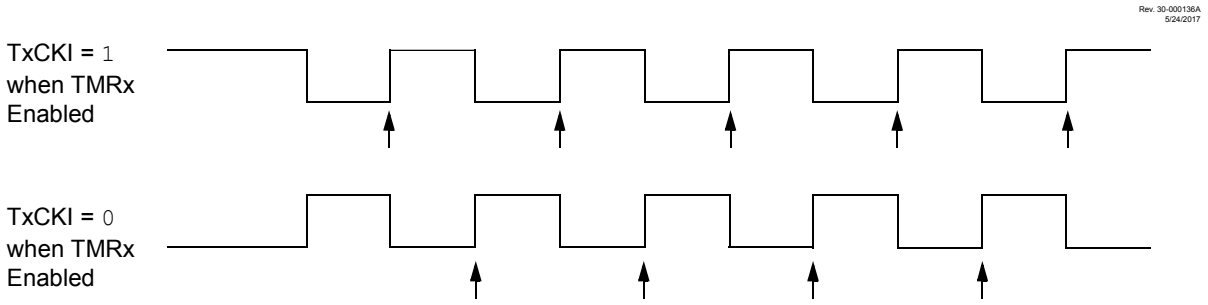
Value	Condition	Description
0 to 255	T016BIT = 0	8-bit Timer 0 Period Value. TMR0L continues counting from 0 when this value is reached.
0 to 255	T016BIT = 1	16-bit Timer 0 Most Significant Byte

When the F_{OSC} internal clock source is selected, the Timer1 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1 value. To utilize the full resolution of Timer1, an asynchronous input signal must be used to gate the Timer1 clock input.

Important: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- Timer1 enabled after POR
- Write to TMRxH or TMRxL
- Timer1 is disabled
- Timer1 is disabled (TMRxON = 0) when TxCKI is high then Timer1 is enabled (TMRxON = 1) when TxCKI is low. Refer to the figure below.

Figure 26-2. Timer1 Incrementing Edge



Note:

1. Arrows indicate counter increments.
2. In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

26.2.2 External Clock Source

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When enabled to count, Timer1 is incremented on the rising edge of the external clock input of the TxCKIPPS pin. This external clock source can be synchronized to the system clock or it can run asynchronously.

26.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMRxH or TMRxL.

26.4 Secondary Oscillator

A secondary low-power 32.768 kHz oscillator circuit is built-in between pins SOSCI (input) and SOSCO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal. The secondary oscillator is not dedicated only to Timer1; it can also be used by other modules.

30.12.1 PWMxCON

Name: PWMxCON
Address: 0x38E,0x392

PWM Control Register

Bit	7	6	5	4	3	2	1	0
	EN		OUT	POL				
Access	R/W		RO	R/W				
Reset	0		0	0				

Bit 7 – EN PWM Module Enable bit

Value	Description
1	PWM module is enabled
0	PWM module is disabled

Bit 5 – OUT PWM Module Output Level When Bit is Read

Bit 4 – POL PWM Output Polarity Select bit

Value	Description
1	PWM output is inverted
0	PWM output is normal

31.15.4 CWGxISM

Name: CWGxISM
Address: 0x60D,0x617

CWGx Input Selection Register

Bit	7	6	5	4	3	2	1	0
					ISM[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – ISM[3:0] CWG Data Input Source Select bits

Table 31-4. CWG Data Input Sources

ISM	Data Source
1111	Reserved
1110	CLC4_out
1101	CLC3_out
1100	CLC2_out
1011	CLC1_out
1010	DSM1_out
1001	C2_out
1000	C1_out
0111	NCO1_out
0110	PWM7_out
0101	PWM6_out
0100	CCP4_out
0011	CCP3_out
0010	CCP2_out
0001	CCP1_out
0000	Pin selected by CWGxINPPS

33.8 Register Definitions: Configurable Logic Cell

Long bit name prefixes for the CLC peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

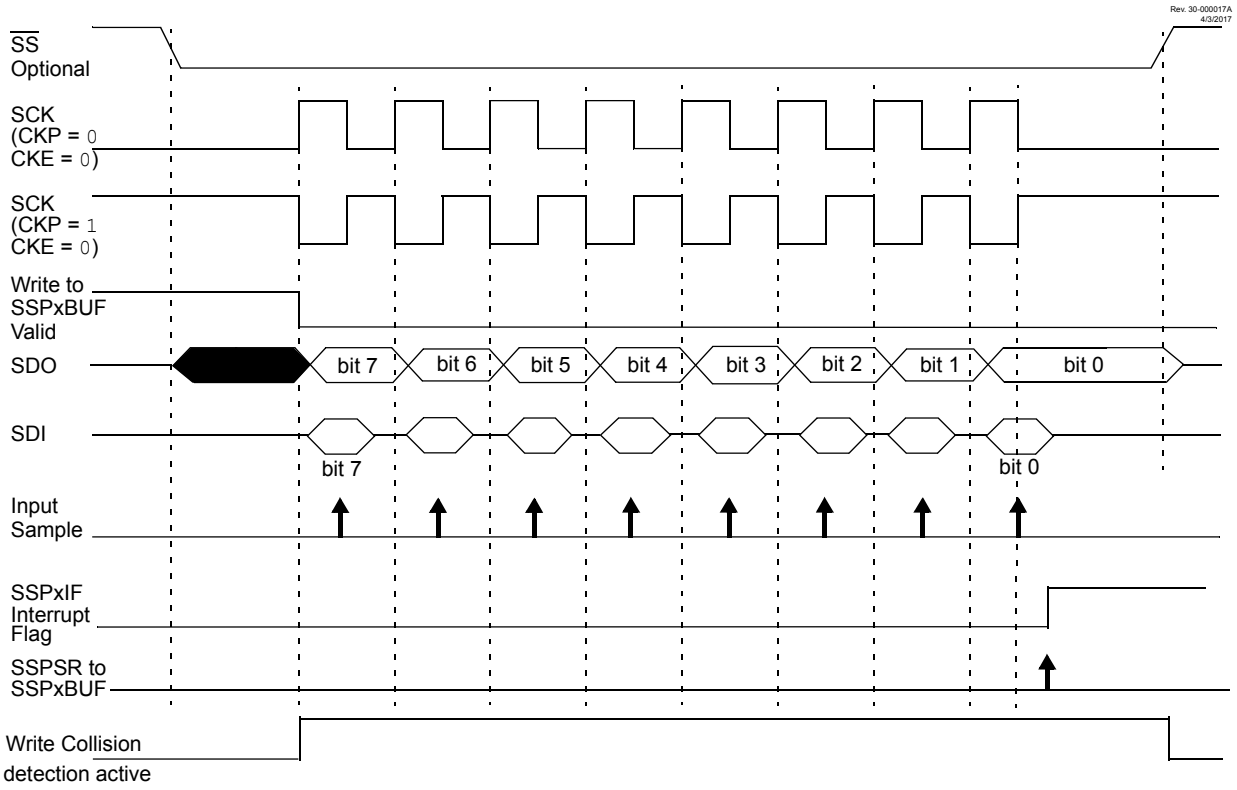
Table 33-2. CLC Bit Name Prefixes

Peripheral	Bit Name Prefix
CLC1	LC1
CLC2	LC2
CLC3	LC3
CLC4	LC4

Related Links

Long Bit Names

Figure 35-7. SPI Mode Waveform (Slave Mode with CKE = 0)



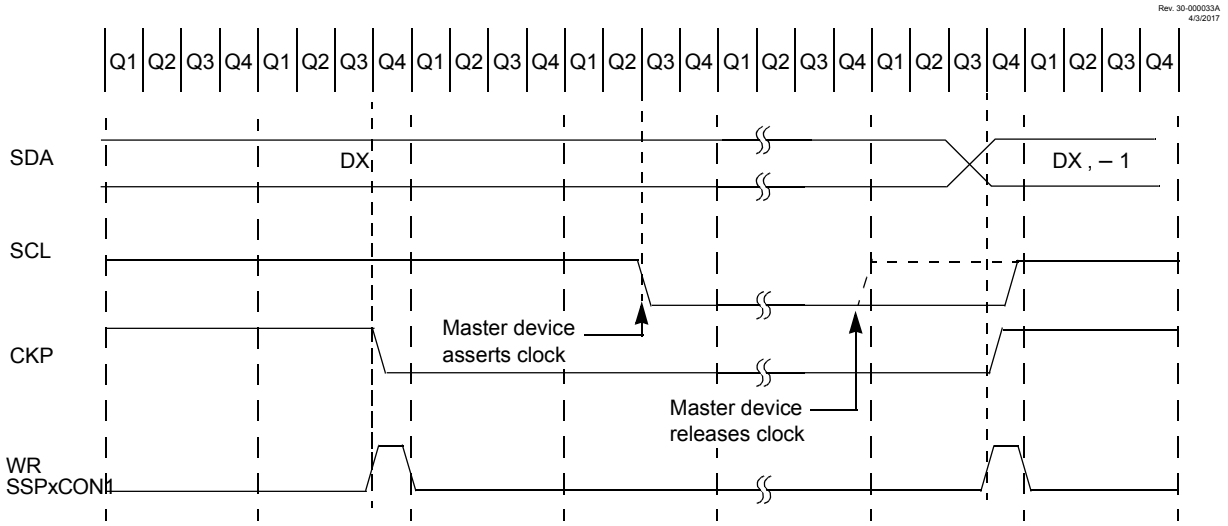
This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 35-16 displays a module using both address and data holding. Figure 35-17 includes the operation with the SEN bit of the SSPxCON2 register set.

1. S bit is set; SSPxIF is set if interrupt on Start detect is enabled.
2. Matching address with R/W bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCL.
3. Slave clears the SSPxIF.
4. Slave can look at the ACKTIM bit to determine if the SSPxIF was after or before the $\overline{ACK}$.
5. Slave reads the address value from SSPxBUF, clearing the BF flag.
6. Slave sets $\overline{ACK}$ value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSPxIF is set after an $\overline{ACK}$, not after a NACK.
9. If SEN = 1, the slave hardware will stretch the clock after the $\overline{ACK}$.
10. Slave clears SSPxIF.

Important: SSPxIF is still set after the ninth falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set

11. SSPxIF set and CKP cleared after eighth falling edge of SCL for a received data byte.
12. Slave looks at ACKTIM bit to determine the source of the interrupt.
13. Slave reads the received data from SSPxBUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an $\overline{ACK}$ = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit.

Figure 35-23. Clock Synchronization Timing

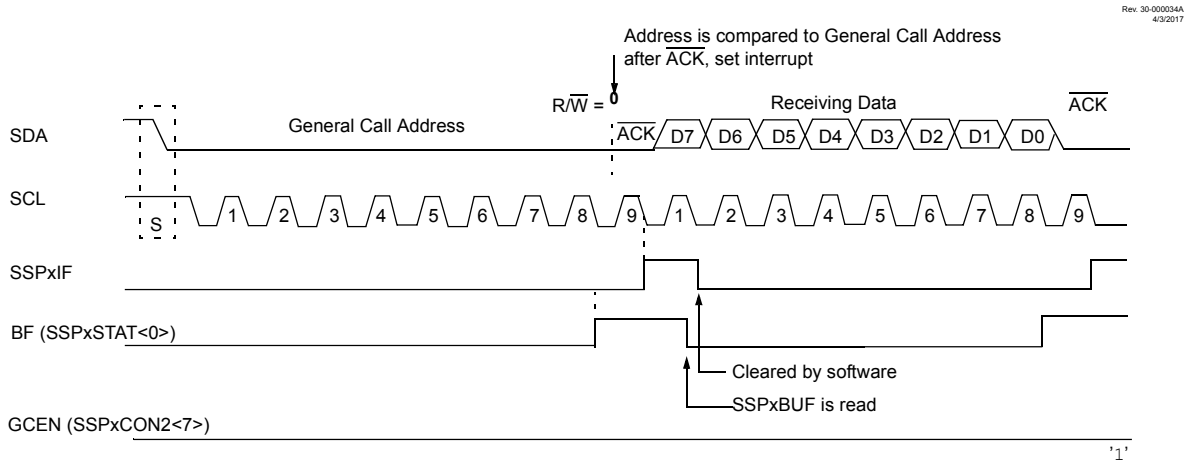


35.5.8 General Call Address Support

The addressing procedure for the I²C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I²C protocol, defined as address 0x00. When the GCEN bit is set, the slave module will automatically $\overline{\text{ACK}}$ the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/$\overline{\text{W}}$ bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. The following figure shows a general call reception sequence.

Figure 35-24. Slave Mode General Call Address Sequence



In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

6. If 9-bit reception is desired, set the RX9 bit.
7. Set the CREN bit to enable reception.
8. The RCxIF bit will be set when reception is complete. An interrupt will be generated if the RCxIE bit was set.
9. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCxSTA register.
10. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCxREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

36.4 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

36.4.1 Synchronous Receive During Sleep

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCxSTA and TXxSTA Control registers must be configured for Synchronous Slave Reception (see Synchronous Slave Reception Setup:).
- If interrupts are desired, set the RCxIE bit of the PIEx register and the GIE and PEIE bits of the INTCON register.
- The RCxIF interrupt flag must be cleared by reading RCxREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RXx/DTx and TXx/CKx pins, respectively. When the data word has been completely clocked in by the external device, the RCxIF interrupt flag bit of the PIRx register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the `SLEEP` instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

36.4.2 Synchronous Transmit During Sleep

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- The RCxSTA and TXxSTA Control registers must be configured for synchronous slave transmission (see Synchronous Slave Transmission Setup).
- The TXxIF interrupt flag must be cleared by writing the output data to the TXxREG, thereby filling the TSR and transmit buffer.
- Interrupt enable bits TXxIE of the PIEx register and PEIE of the INTCON register must set.
- If interrupts are desired, set the GIEx bit of the INTCON register.

Upon entering Sleep mode, the device will be ready to accept clocks on TXx/CKx pin and transmit data on the RXx/DTx pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXxREG will transfer to the TSR and the TXxIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXxREG is available to accept another character for transmission. Writing TXxREG will clear the TXxIF flag.

37.3.5 SMTxWIN

Name: SMTxWIN
Address: 0x049D

SMT Window Input Select Register

Bit	7	6	5	4	3	2	1	0
				WSEL[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – WSEL[4:0] SMT Window Selection bits

Table 37-6. SMT Window Selection

WSEL<4:0>	SMT1 Window Source
11111-11000	Reserved
10111	NCO1OUT
10110	Reserved
10101	CLKREFOUT
10100	CLC4OUT
10011	CLC3OUT
10010	CLC2OUT
10001	CLC1OUT
10000	ZCDOUT
01111	C2OUT
01110	C1OUT
01101	PWM7OUT
01100	PWM6OUT
01011	CCP4OUT
01010	CCP3OUT
01001	CCP2OUT
01000	CCP1OUT
00111	TMR6_postscaled_out
00110	TMR4_postscaled_out
00101	TMR2_postscaled_out
00100	TMR0_overflow
00011	SOSC

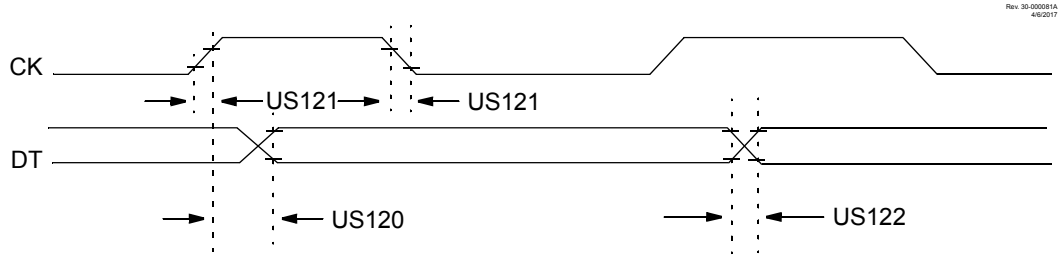
I/O and CLKOUT Timing Specifications

42.4.16 EUSART Synchronous Transmission Requirements

Table 42-22.

Standard Operating Conditions (unless otherwise stated)						
Param No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US120	$T_{CK}H2_{DT}V$	SYNC XMIT (Master and Slave)	—	80	ns	$3.0V \le V_{DD} \le 5.5V$
		Clock high to data-out valid	—	100	ns	$1.8V \le V_{DD} \le 5.5V$
US121	T_{CKRF}	Clock out rise time and fall time	—	45	ns	$3.0V \le V_{DD} \le 5.5V$
		(Master mode)	—	50	ns	$1.8V \le V_{DD} \le 5.5V$
US122	T_{DTRF}	Data-out rise time and fall time	—	45	ns	$3.0V \le V_{DD} \le 5.5V$
			—	50	ns	$1.8V \le V_{DD} \le 5.5V$

Figure 42-15. EUSART Synchronous Transmission (Master/Slave) Timing



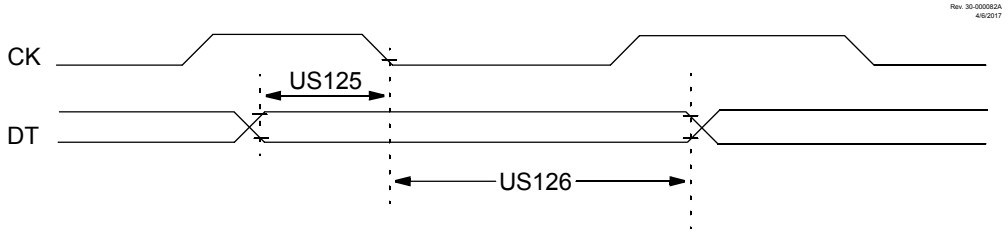
Note: Refer to Figure 42-4 for load conditions.

42.4.17 EUSART Synchronous Receive Requirements

Table 42-23.

Standard Operating Conditions (unless otherwise stated)						
Param No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US125	$T_{DT}V2_{CKL}$	SYNC RCV (Master and Slave)	10	—	ns	
		Data-setup before CK ↓ (DT hold time)				
US126	$T_{CK}L2_{DTL}$	Data-hold after CK ↓ (DT hold time)	15	—	ns	

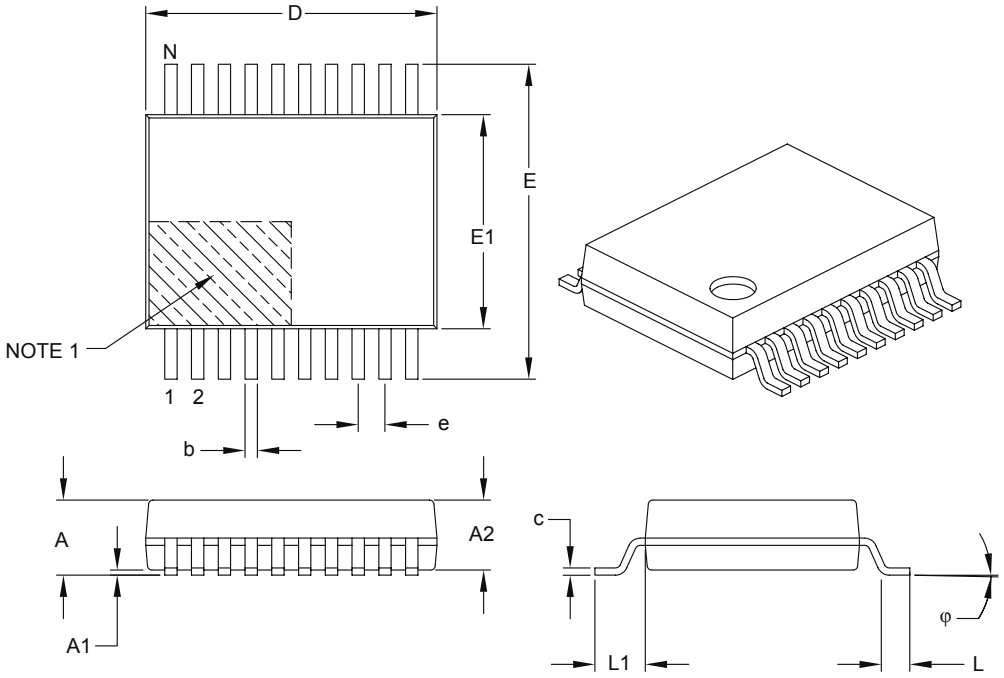
Figure 42-16. EUSART Synchronous Receive (Master/Slave) Timing



Note: Refer to Figure 42-4 for load conditions.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

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Quality Management System Certified by DNV

ISO/TS 16949

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