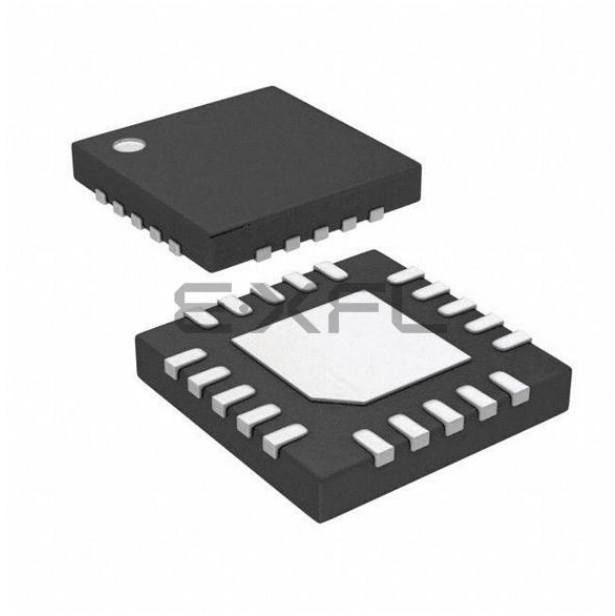

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18446-e-gz

7.8.3 PCL

Name: PCL
Address: 0x02 + n*0x80 [n=0..63]

Low byte of the Program Counter

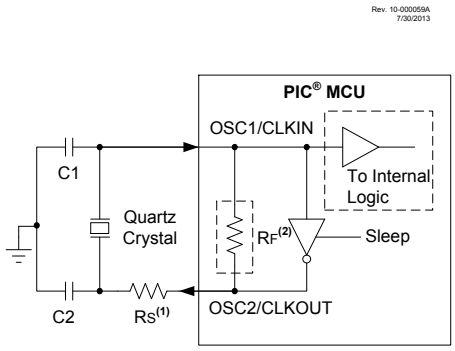
Bit	7	6	5	4	3	2	1	0
	PCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PCL[7:0]
Provides direct read and write access to the Program Counter

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require operating frequencies up to 20 MHz.

Figure 9-3 and Figure 9-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

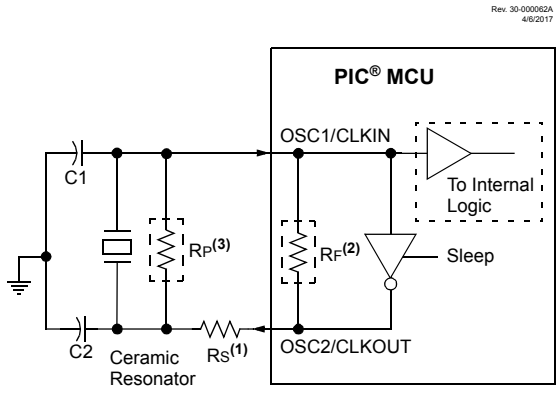
Figure 9-3. Quartz Crystal Operation (LP, XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for quartz crystals with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Figure 9-4. Ceramic Resonator Operation (XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for ceramic resonators with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).
3. An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation.

9.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR), or a wake-up from Sleep. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

10.7.5 PIE3

Name: PIE3
Address: 0x719

Peripheral Interrupt Enable Register 3

Bit	7	6	5	4	3	2	1	0
			RC1IE	TX1IE	BCL2IE	SSP2IE	BCL1IE	SSP1IE
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 5 – RCnIE EUSARTn Receive Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bit 4 – TXnIE EUSARTn Transmit Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bits 1, 3 – BCLnIE MSSPn Bus Collision Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Bits 0, 2 – SSPnIE Synchronous Serial Port ‘n’ Interrupt Enable bit

Value	Description
1	Enabled
0	Disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

14.5 Register Summary - Input/Output

Offset	Name	Bit Pos.								
0x0C	PORTA	7:0			RA5	RA4	RA3	RA2	RA1	RA0
0x0D	PORTB	7:0	RB7	RB6	RB5	RB4				
0x0E	PORTC	7:0	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
0x0F ... 0x11	Reserved									
0x12	TRISA	7:0			TRISA5	TRISA4		TRISA2	TRISA1	TRISA0
0x13	TRISB	7:0	TRISB7	TRISB6	TRISB5	TRISB4				
0x14	TRISC	7:0	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
0x15 ... 0x17	Reserved									
0x18	LATA	7:0			LATA5	LATA4		LATA2	LATA1	LATA0
0x19	LATB	7:0	LATB7	LATB6	LATB5	LATB4				
0x1A	LATC	7:0	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
0x1B ... 0x1F37	Reserved									
0x1F38	ANSELA	7:0			ANSELA5	ANSELA4		ANSELA2	ANSELA1	ANSELA0
0x1F39	WPUA	7:0			WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
0x1F3A	ODCONA	7:0			ODCA5	ODCA4		ODCA2	ODCA1	ODCA0
0x1F3B	SLRCONA	7:0			SLRA5	SLRA4		SLRA2	SLRA1	SLRA0
0x1F3C	INLVLA	7:0			INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
0x1F3D ... 0x1F42	Reserved									
0x1F43	ANSELB	7:0	ANSELB7	ANSELB6	ANSELB5	ANSELB4				
0x1F44	WPUB	7:0	WPUB7	WPUB6	WPUB5	WPUB4				
0x1F45	ODCONB	7:0	ODCB7	ODCB6	ODCB5	ODCB4				
0x1F46	SLRCONB	7:0	SLRB7	SLRB6	SLRB5	SLRB4				
0x1F47	INLVLB	7:0	INLVLB7	INLVLB6	INLVLB5	INLVLB4				
0x1F48 ... 0x1F4D	Reserved									
0x1F4E	ANSELC	7:0	ANSELC7	ANSELC6	ANSELC5	ANSELC4	ANSELC3	ANSELC2	ANSELC1	ANSELC0
0x1F4F	WPUC	7:0	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
0x1F50	ODCONC	7:0	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0
0x1F51	SLRCONC	7:0	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
0x1F52	INLVLC	7:0	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0

14.6 Register Definitions: Port Control

14.6.18 ODCONC

Name: ODCONC
Address: 0x1F50

Open-Drain Control Register

Bit	7	6	5	4	3	2	1	0
	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – ODCCn Open-Drain Configuration on RC Pins

Value	Description
1	Port pin operates as open-drain drive (sink current only)
0	Port pin operates as standard push-pull drive (source and sink current)

Note: Bits ODCC6 and ODCC7 available on 20-pin or higher pin-count devices only; Bits unimplemented for lower pin-count devices.

17.6.1 IOCAP

Name: IOCAP
Address: 0x1F3D

Interrupt-on-Change Positive Edge Register

Bit	7	6	5	4	3	2	1	0
			IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5 – IOCAPn Interrupt-on-Change Positive Edge Enable bits

Value	Description
1	Interrupt-on-Change enabled on the IOCA pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0	Interrupt-on-Change disabled for the associated pin.

Note:

1. IOCAP0 and IOCAP1 are not available for use if the debugger is enabled.
2. If MCLRE = `1` or LVP = `1`, port functionality is disabled and IOCAP3 is not available.

18.3 Register Summary - FVR

Offset	Name	Bit Pos.								
0x090C	FVRCON	7:0	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR[1:0]		ADFVR[1:0]	

18.4 Register Definitions: FVR Control

22.1 NCO Operation

The NCO operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCO output (NCO_overflow). This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See the following equation.

Equation 22-1. NCO Overflow Frequency

$$F_{OVERFLOW} = \frac{NCO\ Clock\ Frequency \times Increment\ Value}{2^{20}}$$

22.1.1 NCO Clock Sources

Clock sources available to the NCO are shown in the following table:

Table 22-1. NCO Clock Sources

CKS	Clock Source
1111-1011	Reserved
1010	CLC4_out
1001	CLC3_out
1000	CLC2_out
0111	CLC1_out
0110	CLKR
0101	SOSC
0100	MFINTOSC (32 kHz)
0011	MFINTOSC (500 kHz)
0010	LFINTOSC
0001	HFINTOSC
0000	F_{OSC}

The NCO clock source is selected by configuring the CKS bits.

Related Links

NCOxCLK

22.1.2 Accumulator

The accumulator is a 20-bit register. Read and write access to the accumulator is available through three registers:

- NCOxACCL
- NCOxACCH
- NCOxACCU

Related Links

NCOxACC

26.14.3 TMRxCLK

Name: TMRxCLK
Address: 0x211,0x217,0x21D

Timer Clock Source Selection Register

Bit	7	6	5	4	3	2	1	0
				CS[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – CS[4:0] Timer Clock Source Selection bits
Refer to the clock source selection table

Reset States: POR/BOR = 00000
All Other Resets = uuuuu

CS<3:0>	Clock Source		
	Timer2	Timer4	Timer6
0110	MFINTOSC(31.25 kHz)	MFINTOSC(31.25 kHz)	MFINTOSC(31.25 kHz)
0101	MFINTOSC(500 kHz)	MFINTOSC(500 kHz)	MFINTOSC(500 kHz)
0100	LFINTOSC	LFINTOSC	LFINTOSC
0011	HFINTOSC(32 MHz)	HFINTOSC(32 MHz)	HFINTOSC(32 MHz)
0010	F_{OSC}	F_{OSC}	F_{OSC}
0001	$F_{OSC}/4$	$F_{OSC}/4$	$F_{OSC}/4$
0000	T2CKIPPS	T4CKIPPS	T6CKIPPS

27.1 Timer2 Operation

Timer2 operates in three major modes:

- Free Running Period
- One-shot
- Monostable

Within each mode there are several options for starting, stopping, and reset. Table 27-3 lists the options.

In all modes, the T2TMR count register is incremented on the rising edge of the clock signal from the programmable prescaler. When T2TMR equals T2PR, a high level is output to the postscaler counter. T2TMR is cleared on the next clock input.

An external signal from hardware can also be configured to gate the timer operation or force a T2TMR count Reset. In Gate modes the counter stops when the gate is disabled and resumes when the gate is enabled. In Reset modes the T2TMR count is reset on either the level or edge from the external source.

The T2TMR and T2PR registers are both directly readable and writable. The T2TMR register is cleared and the T2PR register initializes to FFh on any device Reset. Both the prescaler and postscaler counters are cleared on the following events:

- A write to the T2TMR register
- A write to the T2CON register
- Any device Reset
- External Reset Source event that resets the timer.

Important: T2TMR is not cleared when T2CON is written.

27.1.1 Free Running Period Mode

The value of T2TMR is compared to that of the Period register, T2PR, on each clock cycle. When the two values match, the comparator resets the value of T2TMR to 00h on the next cycle and increments the output postscaler counter. When the postscaler count equals the value in the OUTPS bits of the T2CON

7. When TxTMR = TxPR, the next clock clears TxTMR, regardless of the operating mode.

30.11 Register Summary - Registers Associated with PWM

Offset	Name	Bit Pos.								
0x038C	PWM6DC	7:0	DCL[1:0]							
		15:8	DCH[7:0]							
0x038E	PWM6CON	7:0	EN		OUT	POL				
0x038F	Reserved									
0x0390	PWM7DC	7:0	DCL[1:0]							
		15:8	DCH[7:0]							
0x0392	PWM7CON	7:0	EN		OUT	POL				

30.12 Register Definitions: PWM Control

Long bit name prefixes for the PWM peripherals are shown in the table below. Refer to the *"Long Bit Names Section"* for more information.

Table 30-3. PWM Bit Name Prefixes

Peripheral	Bit Name Prefix
PWM6	PWM6
PWM7	PWM7

Related Links

Long Bit Names

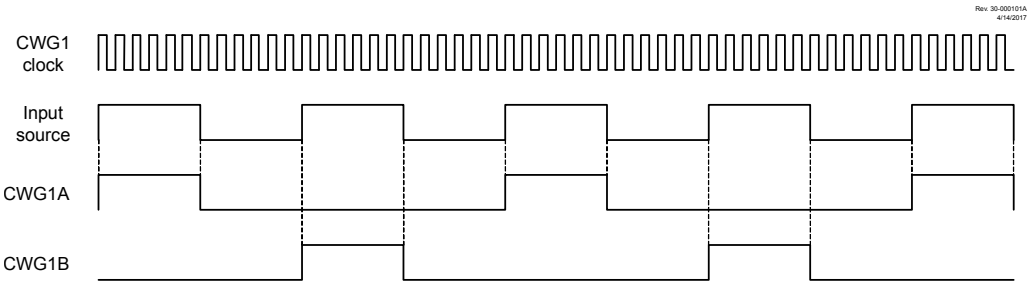
The CWG auto-shutdown operation also applies in Steering modes as described in Auto-Shutdown". An auto-shutdown event will only affect pins that have STRy = 1.

31.2.4.1 Synchronous Steering Mode

In Synchronous Steering mode (MODE = 001), changes to steering selection registers take effect on the next rising edge of the modulated data input (see figure below). In Synchronous Steering mode, the output will always produce a complete waveform.

Important: Only the STRx bits are synchronized; the OVRx bits are not synchronized.

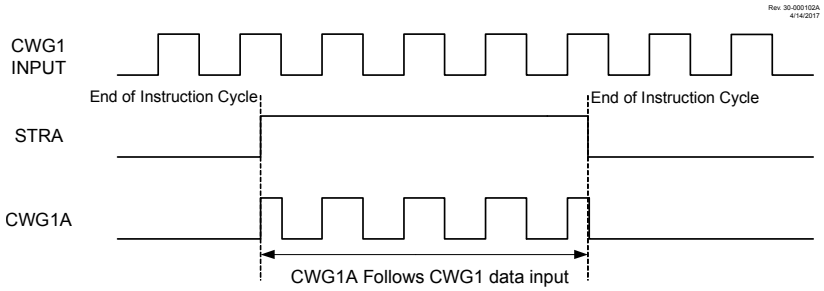
Figure 31-10. Example of Synchronous Steering (MODE = 001)



31.2.4.2 Asynchronous Steering Mode

In Asynchronous mode (MODE = 000), steering takes effect at the end of the instruction cycle that writes to STRx. In Asynchronous Steering mode, the output signal may be an incomplete waveform (see figure below). This operation may be useful when the user firmware needs to immediately remove a signal from the output pin.

Figure 31-11. Example of Asynchronous Steering (MODE = 000)



31.3 Start-up Considerations

The application hardware must use the proper external pull-up and/or pull-down resistors on the CWG output pins. This is required because all I/O pins are forced to high-impedance at Reset.

The polarity control bits (POLy) allow the user to choose whether the output signals are active-high or active-low.

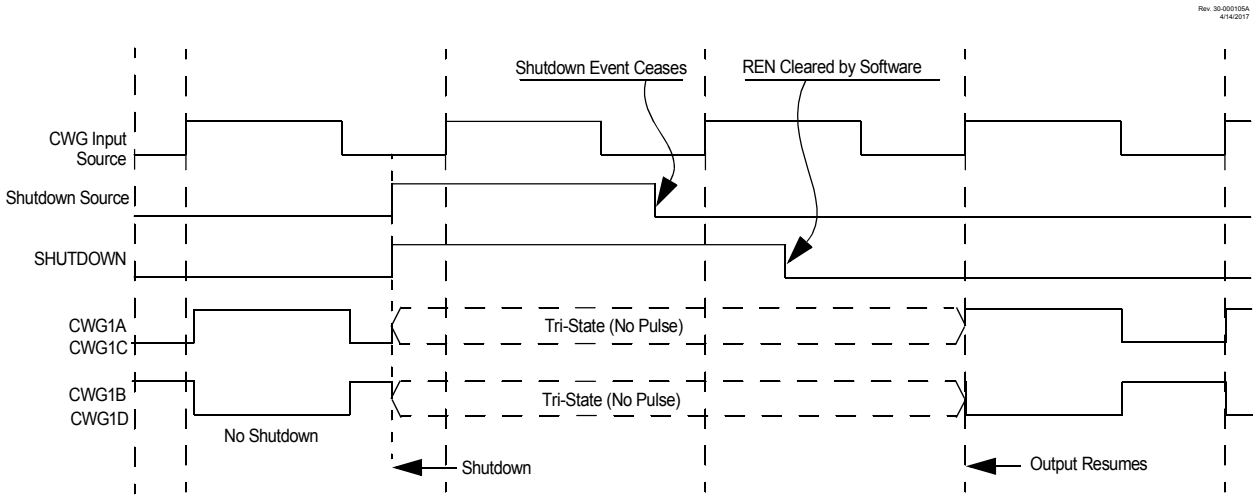
31.4 Clock Source

The clock source is used to drive the dead-band timing circuits. The CWG module allows the following clock sources to be selected:

Once all auto-shutdown sources are removed, the software must clear SHUTDOWN. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.

Important: The SHUTDOWN bit cannot be cleared in software if the auto-shutdown condition is still present.

Figure 31-17. SHUTDOWN FUNCTIONALITY, AUTO-RESTART DISABLED (REN = 0, LSAC = 01, LSBD = 01)



31.11.2.2 Auto-Restart

When the REN bit is set (REN = 1), the CWG module will restart from the shutdown state automatically.

Once all auto-shutdown conditions are removed, the hardware will automatically clear SHUTDOWN. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.

Important: The SHUTDOWN bit cannot be cleared in software if the auto-shutdown condition is still present.

31.15.8 CWGxDBR

Name: CWGxDBR
Address: 0x60E,0x618

CWG Rising Dead-Band Count Register

Bit	7	6	5	4	3	2	1	0
			DBR[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 5:0 – DBR[5:0] CWG Rising Edge Triggered Dead-Band Count bits
Reset States: POR/BOR = xxxxxx
All Other Resets = uuuuuu

Value	Description
n	Dead band is active no less than n, and no more than n+1, CWG clock periods after the rising edge
0	0 CWG clock periods. Dead-band generation is bypassed

33.8.10 CLCxGLS3

Name: CLCxGLS3
Address: 0x1E19,0x1E23,0x1E2D,0x1E37

CLCx Gate4 Logic Select Register

Bit	7	6	5	4	3	2	1	0
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 1, 3, 5, 7 – G4DyT
dyT: Gate4 Data 'y' True (non-inverted) bit
Reset States: Default = xxxx
POR/BOR = x
All Other Resets = u

Value	Description
1	dyT is gated into g4
0	dyT is not gated into g4

Bits 0, 2, 4, 6 – G4DyN
dyN: Gate4 Data 'y' Negated (inverted) bit
Reset States: Default = xxxx
POR/BOR = x
All Other Resets = u

Value	Description
1	dyN is gated into g4
0	dyN is not gated into g4

35. (MSSP) Master Synchronous Serial Port Module

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

The SPI interface supports the following modes and features:

- Master mode
- Slave mode
- Clock Parity
- Slave Select Synchronization (Slave mode only)
- Daisy-chain connection of slave devices

The I^2C interface supports the following modes and features:

- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- Limited multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking
- Clock stretching
- Bus collision detection
- General call address matching
- Address masking
- Address Hold and Data Hold modes
- Selectable SDA hold times

35.1 SPI Mode Overview

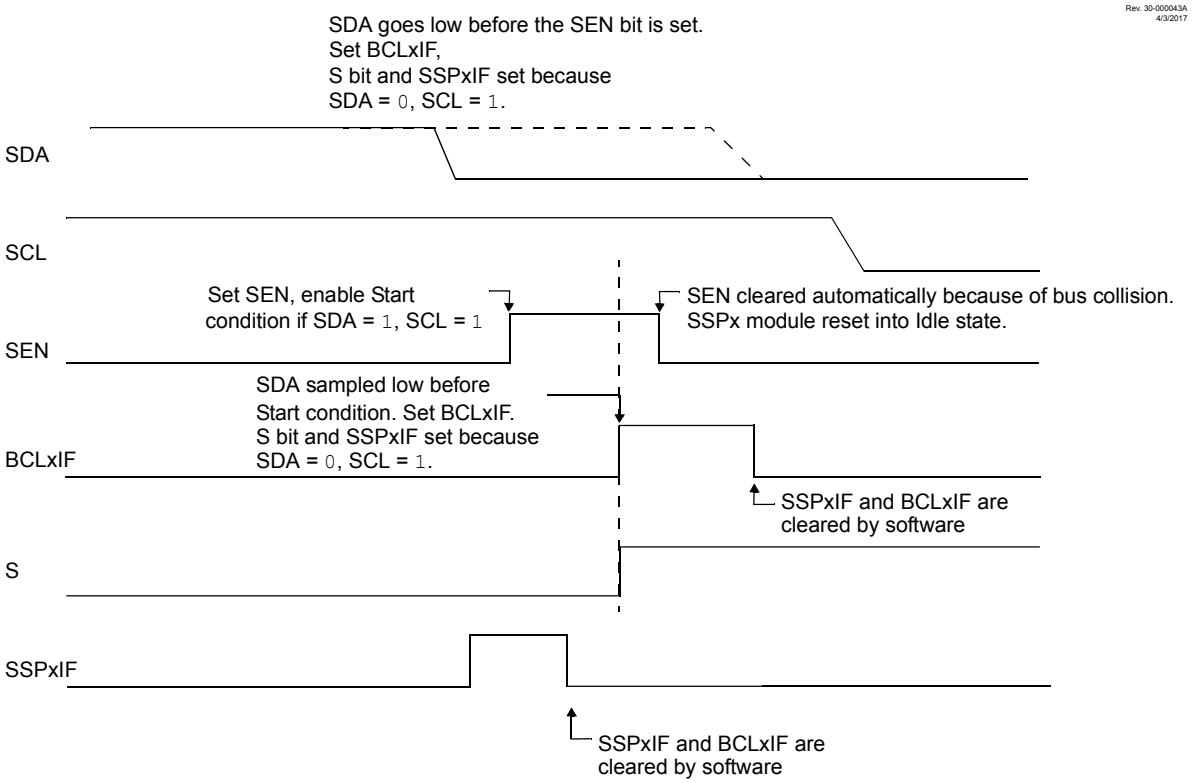
The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select ($\overline{SS}$)

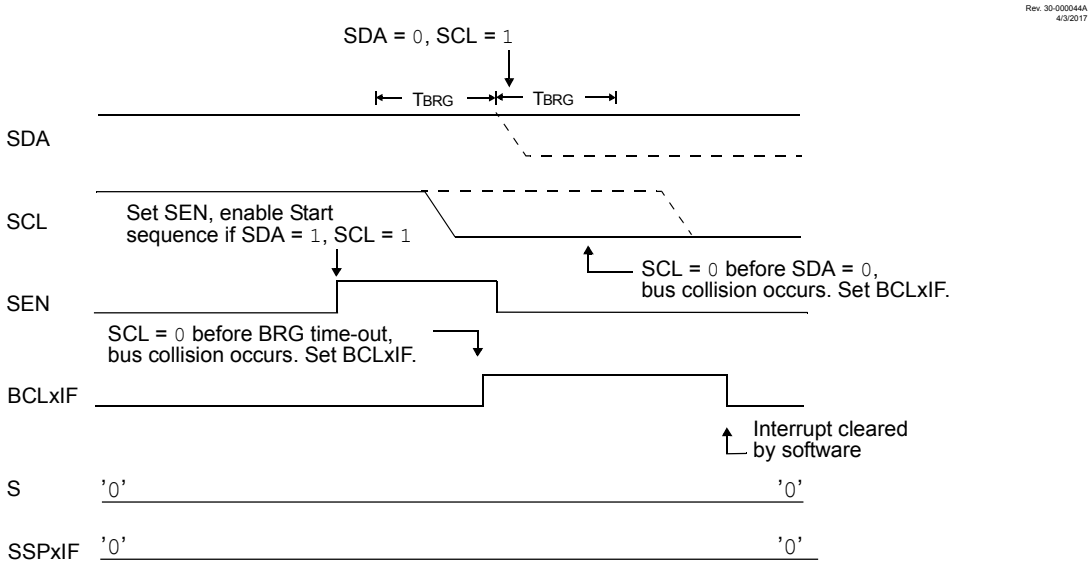
The following figure shows the block diagram of the MSSP module when operating in SPI mode.

Figure 35-33. Bus Collision During Start Condition (SDA Only)



The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

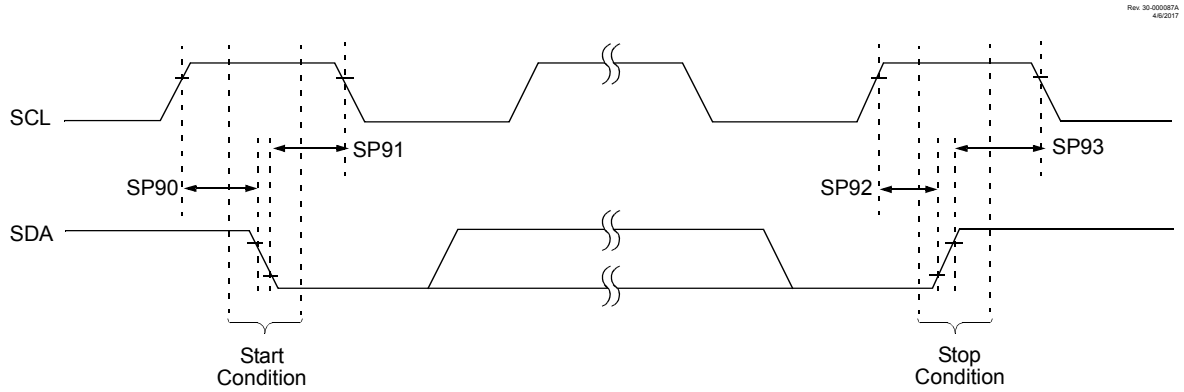
Figure 35-34. Bus Collision During Start Condition (SCL = 0)



Value	Condition	Description
1	SYNC=0	Auto-Baud Detect mode is enabled (clears when auto-baud is complete)
0	SYNC=0	Auto-Baud Detect is complete or mode is disabled
X	SYNC=1	Don't care

Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic		Min.	Typ. †	Max.	Units	Conditions
			400 kHz mode	600	—	—		
* - These parameters are characterized but not tested.								

Figure 42-21. I²C Bus Start/Stop Bits Timing



Note: Refer to Figure 42-4 for load conditions.

42.4.20 I²C Bus Data Requirements

Table 42-26.

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic		Min.	Max.	Units	Conditions
SP100*	T_{HIGH}	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	$1.5T_{CY}$	—		
SP101*	T_{LOW}	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz