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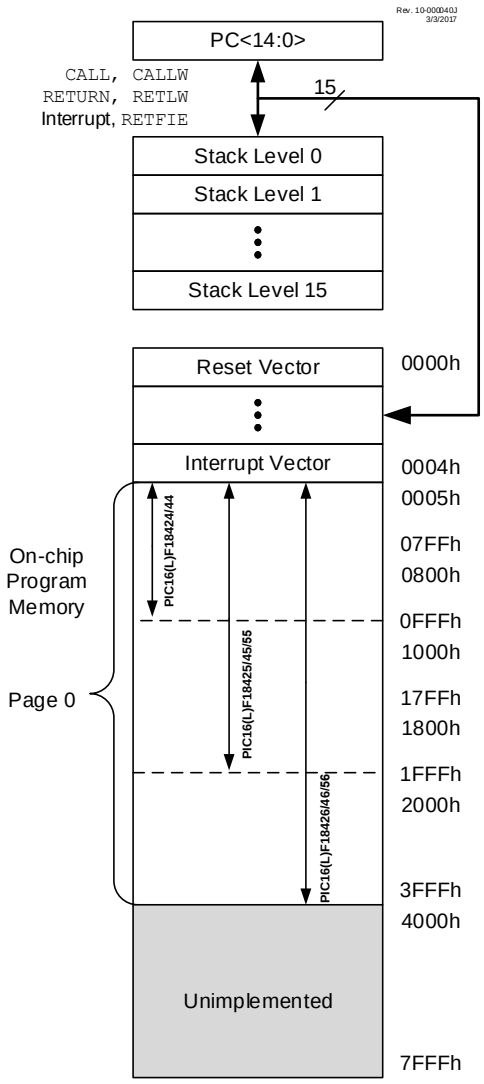
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18446-i-ss

Figure 7-1. Program Memory and Stack



Related Links

CONFIG5

Memory Violation

7.1.1 Reading Program Memory as Data

There are three methods of accessing constants in program memory. The first method is to use tables of `RETLW` instructions. The second method is to set an FSR to point to the program memory. The third method is to use the NVMREG interface to access the program memory.

Related Links

NVMREG Access

The Power-up Timer is controlled by the PWRTS bit field of the Configuration Words.

The Power-up Timer provides a nominal 64 ms timeout on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the V_{DD} to rise to an acceptable level. The Power-up Timer is enabled by setting a non-zero value in the PWRTS bit field, in Configuration Words.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00000607).

8.10 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for selected oscillator source).
3. $\overline{\text{MCLR}}$ must be released (if enabled).

The total time out will vary based on oscillator configuration and Power-up Timer configuration.

The Power-up Timer and oscillator start-up timer run independently of $\overline{\text{MCLR}}$ Reset. If $\overline{\text{MCLR}}$ is kept low long enough, the Power-up Timer and oscillator Start-up Timer will expire. Upon bringing $\overline{\text{MCLR}}$ high, the device will begin execution after 10 F_{OSC} cycles (see figure below). This is useful for testing purposes or to synchronize more than one device operating in parallel.

2x PLL

9.2.1 External Clock Sources

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the NOSC and NDIV bits to switch the system clock source.

Related Links

Clock Switching

9.2.1.1 EC Mode

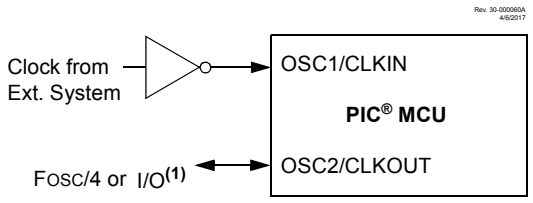
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the CLKIN/OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The following figure shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH – High power, ≤ 32 MHz
- ECM – Medium power, ≤ 8 MHz
- ECL – Low power, ≤ 0.1 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

Figure 9-2. External Clock (EC) Mode Operation



Note:

1. Output depends upon $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words (CONFIG1H).

9.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 9-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

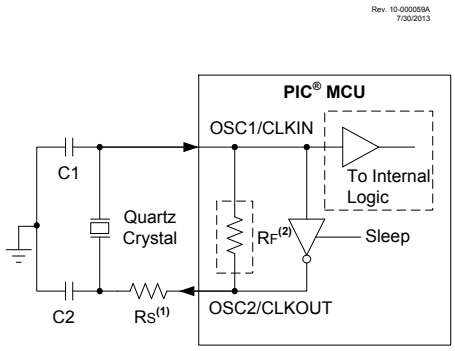
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals). but can operate up to 100 kHz.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive crystals and resonators with a frequency range up to 4 MHz.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require operating frequencies up to 20 MHz.

Figure 9-3 and Figure 9-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

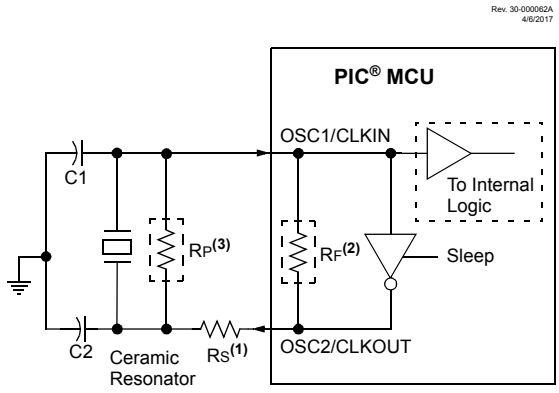
Figure 9-3. Quartz Crystal Operation (LP, XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for quartz crystals with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

Figure 9-4. Ceramic Resonator Operation (XT or HS Mode)



Note:

1. A series resistor (R_S) may be required for ceramic resonators with low drive level.
2. The value of R_F varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).
3. An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation.

9.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR), or a wake-up from Sleep. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

13.4.9 WRERR Bit

The WRERR bit can be used to determine if a write error occurred. WRERR will be set if one of the following conditions occurs:

- If WR is set while the NVMADRH:NMVADRL points to a write-protected address
- A Reset occurs while a self-write operation was in progress
- An unlock sequence was interrupted

The WRERR bit is normally set by hardware, but can be set by the user for test purposes. Once set, WRERR must be cleared in software.

Table 13-3. Actions for PFM When WR = 1

Free	LWLO	Actions for PFM when WR = 1	Comments
1	x	Erase the 32-word row of NVMADRH:NVMADRL location.	• If WP is enabled, WR is cleared and WRERR is set • All 32 words are erased • NVMDATH:NVMDATL is ignored
0	1	Copy NVMDATH:NVMDATL to the write latch corresponding to NVMADR LSBs.	• Write protection is ignored • No memory access occurs
0	0	Write the write-latch data to PFM row.	• If WP is enabled, WR is cleared and WRERR is set • Write latches are reset to 3FFh • NVMDATH:NVMDATL is ignored

Related Links

NVMREG Erase of Program Memory

16.5.5 PMD4

Name: PMD4
Address: 0x79A

PMD Control Register 4

Bit	7	6	5	4	3	2	1	0
		PWM7MD	PWM6MD		CCP4MD	CCP3MD	CCP2MD	CCP1MD
Access		R/W	R/W		R/W	R/W	R/W	R/W
Reset		0	0		0	0	0	0

Bit 6 – PWM7MD Disable Pulse-Width Modulator PWM7 bit

Value	Description
1	PWM7 module disabled
0	PWM7 module enabled

Bit 5 – PWM6MD Disable Pulse-Width Modulator PWM6 bit

Value	Description
1	PWM6 module disabled
0	PWM6 module enabled

Bit 3 – CCP4MD Disable Pulse-Width Modulator CCP4 bit

Value	Description
1	CCP4 module disabled
0	CCP4 module enabled

Bit 2 – CCP3MD Disable Pulse-Width Modulator CCP3 bit

Value	Description
1	CCP3 module disabled
0	CCP3 module enabled

Bit 1 – CCP2MD Disable Pulse-Width Modulator CCP2 bit

Value	Description
1	CCP2 module disabled
0	CCP2 module enabled

Bit 0 – CCP1MD Disable Pulse-Width Modulator CCP1 bit

Value	Description
1	CCP1 module disabled
0	CCP1 module enabled

21.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in the *"5-Bit DAC Specifications"* table from the *"Electrical Specifications"* chapter.

Related Links

5-Bit DAC Specifications

21.3 DAC Voltage Reference Output

The unbuffered DAC voltage can be output to the DACxOUTn pin(s) by setting the respective OEn bit(s). Selecting the DAC reference voltage for output on either DACxOUTn pin automatically overrides the digital output buffer, the weak pull-up and digital input threshold detector functions of that pin.

Reading the DACxOUTn pin when it has been configured for DAC reference voltage output will always return a '0'.

Important: The unbuffered DAC output (DACxOUTn) is not intended to drive an external load.

21.4 Operation During Sleep

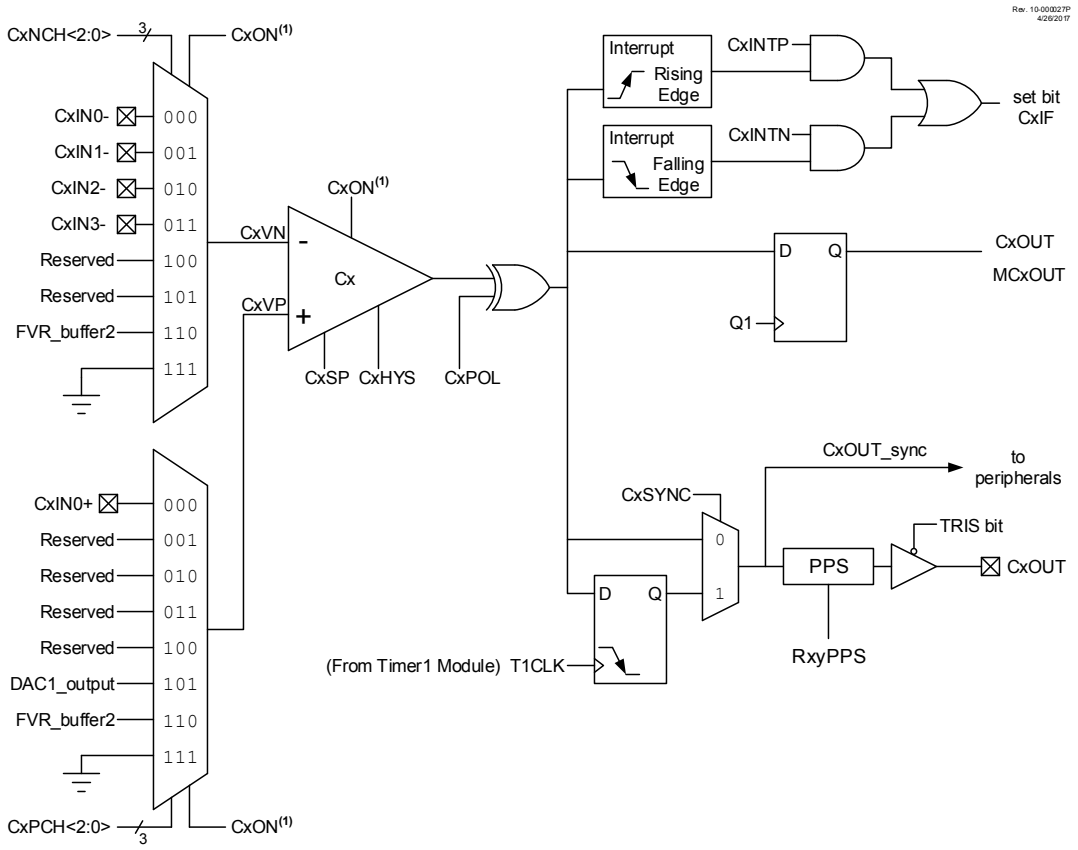
When the device wakes up from Sleep through an interrupt or a Windowed Watchdog Timer Time-out, the contents of the DACxCON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

21.5 Effects of a Reset

A device Reset affects the following:

- DACx is disabled.
- DACx output voltage is removed from the DACxOUTn pin(s).
- The DAC1R range select bits are cleared.

Figure 23-2. Comparator Module Simplified Block Diagram



Related Links

CMxNCH

CMxPCH

23.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register contains Control and Status bits for the following:

- Enable
- Output
- Output polarity
- Hysteresis enable
- Timer1 output synchronization

The CMxCON1 register contains Control bits for the following:

- Interrupt on positive/negative edge enables
- Positive input channel selection
- Negative input channel selection

26.11 CCP Special Event Trigger

When any of the CCPs are configured to trigger a special event, the trigger will clear the TMRxH:TMRxL register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPRxH:CCPRxL register pair becomes the period register for Timer1.

Timer1 should be synchronized and $F_{OSC}/4$ should be selected as the clock source in order to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMRxH or TMRxL coincides with a Special Event Trigger from the CCP, the write will take precedence.

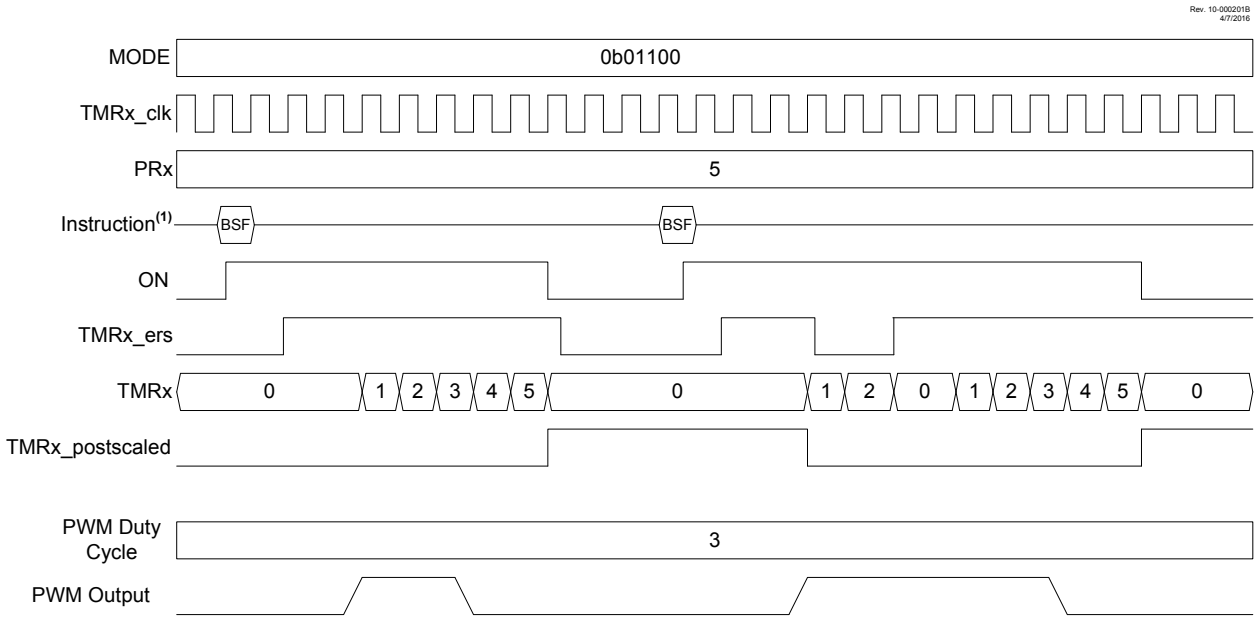
26.12 Peripheral Module Disable

When a peripheral is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module's clock source. The Module Disable bits for Timer1 (TMR1MD) are in the PMD1 register. See Peripheral Module Disable (PMD) chapter for more information.

Related Links

Register Summary - PMD

Figure 27-9. Edge-Triggered Hardware Limit One-Shot Mode Timing Diagram (MODE = 01100)



Note:

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

Related Links

PWM Overview

(PWM) Pulse-Width Modulation

27.6.8 Level Reset, Edge-Triggered Hardware Limit One-Shot Modes

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = 01110)
- High Reset level (MODE<4:0> = 01111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control, a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation, the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

Important: If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

The capture source is selected by configuring the CTS bits as shown in the following table:

Table 29-2. Capture Trigger Sources

CTS	Source
111	CLC4_out
110	CLC3_out
101	CLC2_out
100	CLC1_out
011	IOC_interrupt
010	C2_out
001	C1_out
000	Pin selected by CCPxPPS

29.2.2 Timer1 Mode Resource

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See section *"Timer1 Module with Gate Control"* for more information on configuring Timer1.

Related Links

Timer1 Module with Gate Control

29.2.3 Software Interrupt Mode

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE Interrupt Priority bit of the PIEx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in Operating mode.

Important: Clocking Timer1 from the system clock (F_{OSC}) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock ($F_{OSC}/4$) or from an external clock source.

29.2.4 CCP Prescaler

There are four prescaler settings specified by the MODE bits. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. The example below demonstrates the code to perform this function.

31.15.9 CWGxDBF

Name: CWGxDBF
Address: 0x60F,0x619

CWG Falling Dead-Band Count Register

Bit	7	6	5	4	3	2	1	0
			DBF[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

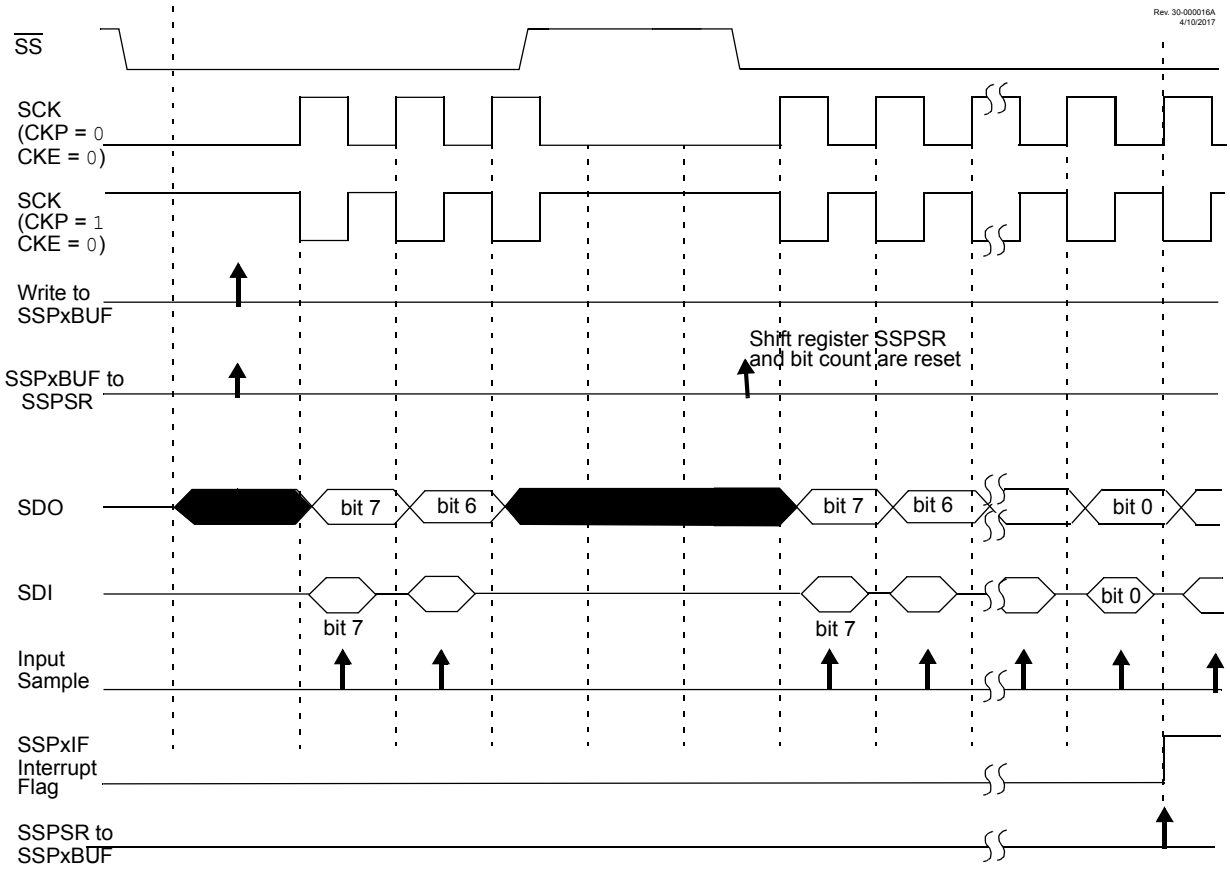
Bits 5:0 – DBF[5:0] CWG Falling Edge Triggered Dead-Band Count bits
Reset States: POR/BOR = xxxxxx
All Other Resets = uuuuuu

Value	Description
n	Dead band is active no less than n, and no more than n+1, CWG clock periods after the falling edge
0	0 CWG clock periods. Dead-band generation is bypassed

2. When the SPI is used in Slave mode with CKE set; the user must enable $\overline{SS}$ pin control.
3. While operated in SPI Slave mode the SMP bit must remain clear.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the $\overline{SS}$ pin to a high level or clearing the SSPEN bit.

Figure 35-6. Slave Select Synchronous Waveform



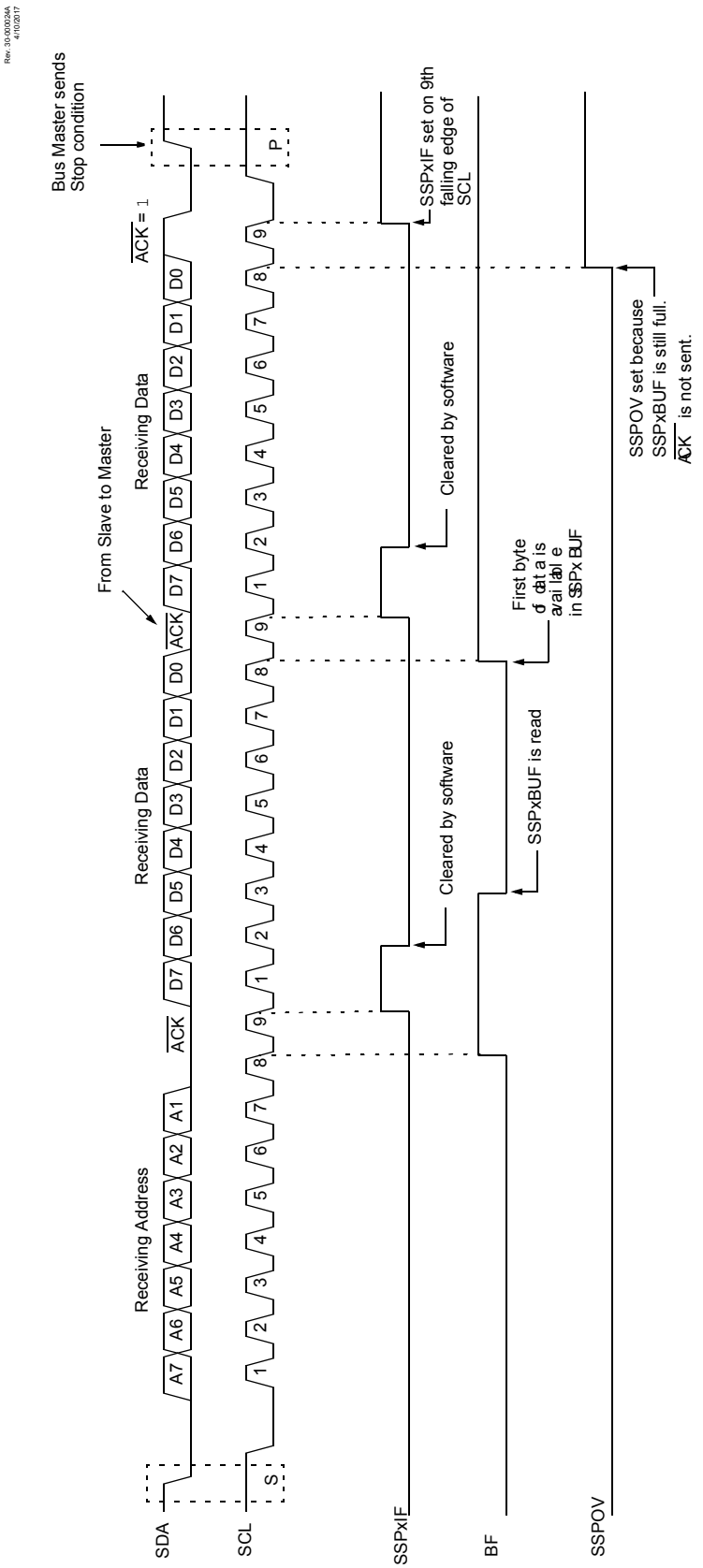


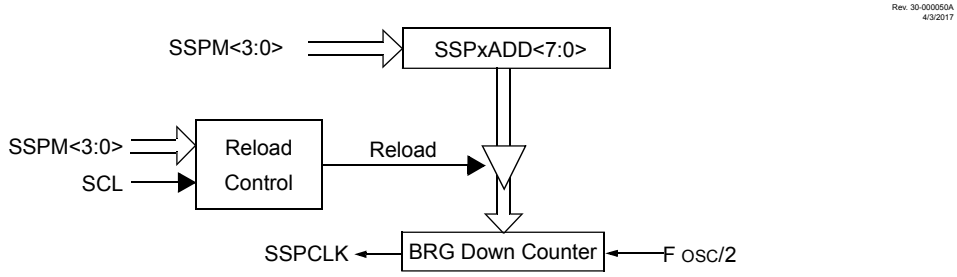
Figure 35-14. I²C Slave, 7-bit Address, Reception (SEN = 0, AHEN = 0, DHEN = 0)

Table 35-1 illustrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD.

MSSP Baud Rate Generator Frequency Equation

$$F_{CLOCK} = \frac{F_{OSC}}{4 \times (SSPxADD + 1`)}$$

Figure 35-40. Baud Rate Generator Block Diagram



Important: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I^2C. This is an implementation limitation.

Table 35-1. MSSP Clock Rate w/BRG

F_{OSC}	F_{CY}	BRG Value	Fclock (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical specifications in the electrical specifications section, Internal Oscillator Parameters, to ensure the system is designed to support Iol requirements.

35.8 Register Summary: MSSP Control

Offset	Name	Bit Pos.								
0x018C	SSP1BUF	7:0	BUF[7:0]							
0x018D	SSP1ADD	7:0	ADD[7:0]							
0x018E	SSP1MSK	7:0	MSK[6:0]							MSK0
0x018F	SSP1STAT	7:0	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
0x0190	SSP1CON1	7:0	WCOL	SSPOV	SSPEN	CKP	SSPM[3:0]			
0x0191	SSP1CON2	7:0	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
0x0192	SSP1CON3	7:0	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
0x0193 ... 0x0195	Reserved									
0x0196	SSP2BUF	7:0	BUF[7:0]							
0x0197	SSP2ADD	7:0	ADD[7:0]							
0x0198	SSP2MSK	7:0	MSK[6:0]							MSK0
0x0199	SSP2STAT	7:0	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
0x019A	SSP2CON1	7:0	WCOL	SSPOV	SSPEN	CKP	SSPM[3:0]			
0x019B	SSP2CON2	7:0	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
0x019C	SSP2CON3	7:0	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN

35.9 Register Definitions: MSSP Control

Value	Condition	Description
1	SYNC=0	Auto-Baud Detect mode is enabled (clears when auto-baud is complete)
0	SYNC=0	Auto-Baud Detect is complete or mode is disabled
X	SYNC=1	Don't care

PIC16LF18426/46 only									
Standard Operating Conditions (unless otherwise stated)									
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
								V_{DD}	**Note**
D202	I_{PD_SOSC}	Secondary Oscillator (S_{OSC})	—	0.6	5	11	µA	3.0V	
D203	I_{PD_FVR}	FVR	—	33	74	76	µA	3.0V	
D204	I_{PD_BOR}	Brown-out Reset (BOR)	—	10	17	19	µA	3.0V	
D205	I_{PD_LPBOR}	Low-Power Brown-out Reset (LPBOR)	—	0.5	3.0	10	µA	3.0V	
D207	I_{PD_ADCA}	ADC - Non-converting	—	0.06	2	9	µA	3.0V	ADC not converting (4)
D208	I_{PD_CMP}	Comparator	—	30	48	56	µA	3.0V	

† - Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. The peripheral current is the sum of the base I_{DD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD}current from this limit. Max. values should be used when calculating total current consumption.
2. The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to V_{SS}.
3. All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.
4. ADC clock source is FRC.

PIC16F18426/46 only									
Standard Operating Conditions (unless otherwise stated), VREGPM = 1									
Param. No.	**Sym.**	**Device Characteristics**	**Min.**	**Typ.†**	**Max. +85°C**	**Max. +125°C**	**Units**	**Conditions**	
								V_{DD}	**Note**
D200	I_{PD}	I_{PD} Base	—	0.4	4	12	µA	3.0V	
D200A			—	18	22	27	µA	3.0V	VREGPM = 0
D201	I_{PD_WDT}	Low-Frequency Internal Oscillator/WDT	—	0.9	6	14	µA	3.0V	

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
MEM11	I_{DDPGM}	Supply Current during Programming operation	—	—	10	mA	
Data EEPROM Memory Specifications							
MEM20	E_D	DataEE Byte Endurance	100k	—	—	E/W	-40°C≤T_A≤ +85°C
MEM21	T_{D_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM22	N_{D_REF}	Total Erase/Write Cycles before Refresh	—	—	100k	E/W	
MEM23	V_{D_RW}	V_{DD} for Read or Erase/Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM24	T_{D_BEW}	Byte Erase and Write Cycle Time	—	4.0	5.0	ms	
Program Flash Memory Specifications							
MEM30	E_P	Flash Memory Cell Endurance	10k	—	—	E/W	-40°C≤Ta≤ +85°C (**Note 1**)
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	V_{DD} for Read operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM34	V_{P_REW}	V_{DD} for Row Erase or Write operation	V_{DDMIN}	—	V_{DDMAX}	V	
MEM35	T_{P_REW}	Self-Timed Row Erase or Self-Timed Write	—	2.0	2.5	ms	

† - Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

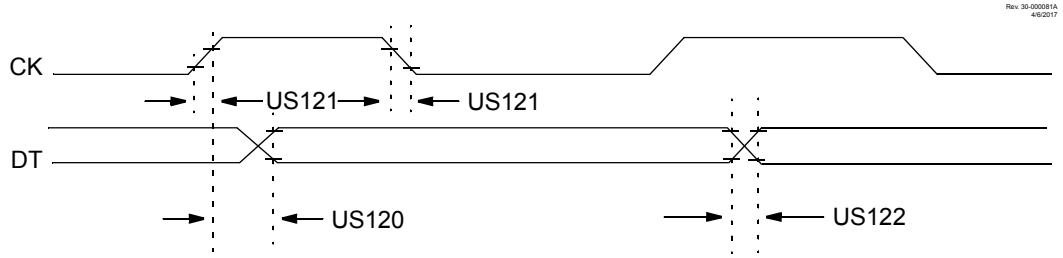
I/O and CLKOUT Timing Specifications

42.4.16 EUSART Synchronous Transmission Requirements

Table 42-22.

Standard Operating Conditions (unless otherwise stated)						
Param No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US120	$T_{CK}H2_{DT}V$	SYNC XMIT (Master and Slave)	—	80	ns	$3.0V \le V_{DD} \le 5.5V$
		Clock high to data-out valid	—	100	ns	$1.8V \le V_{DD} \le 5.5V$
US121	T_{CKRF}	Clock out rise time and fall time	—	45	ns	$3.0V \le V_{DD} \le 5.5V$
		(Master mode)	—	50	ns	$1.8V \le V_{DD} \le 5.5V$
US122	T_{DTRF}	Data-out rise time and fall time	—	45	ns	$3.0V \le V_{DD} \le 5.5V$
			—	50	ns	$1.8V \le V_{DD} \le 5.5V$

Figure 42-15. EUSART Synchronous Transmission (Master/Slave) Timing



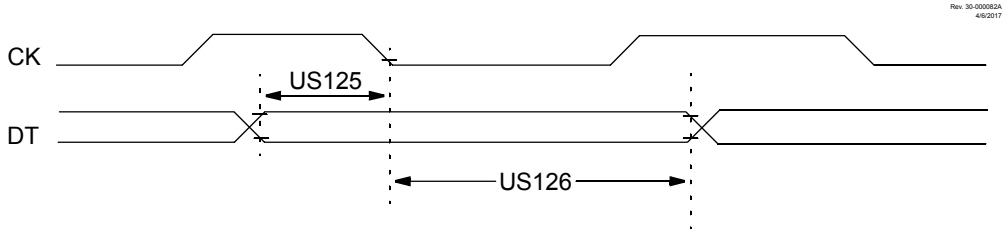
Note: Refer to Figure 42-4 for load conditions.

42.4.17 EUSART Synchronous Receive Requirements

Table 42-23.

Standard Operating Conditions (unless otherwise stated)						
Param No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US125	$T_{DT}V2_{CKL}$	SYNC RCV (Master and Slave)	10	—	ns	
		Data-setup before CK ↓ (DT hold time)				
US126	$T_{CK}L2_{DTL}$	Data-hold after CK ↓ (DT hold time)	15	—	ns	

Figure 42-16. EUSART Synchronous Receive (Master/Slave) Timing



Note: Refer to Figure 42-4 for load conditions.