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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18446t-i-so

Features	PIC16(L)F18426	PIC16(L)F18446
Packages	14 - PDIP 14 - SOIC (3.9 mm) 14 - TSSOP 16 - uQFN (4x4)	20 - PDIP 20 - SOIC (7.5 mm) 20 - SSOP 20 - uQFN (4x4)
I/O Ports	A, C	A, B, C
Capture/Compare/PWM Modules (CCP)	4	4
Configurable Logic Cell (CLC)	4	4
10-Bit Pulse-Width Modulator (PWM)	2	2
12-Bit Analog-to-Digital Module (ADC ²) with Computation Accelerator	11 channels	17 channels
5-Bit Digital-to-Analog Module (DAC)	1	1
Comparators	2	2
Numerical Contolled Oscillator (NCO)	1	1
Interrupt Sources	40	40
Timers (16-/8-bit)	4	4
Serial Communications	2 MSSP 1 EUSART	2 MSSP 1 EUSART
Complementary Waveform Generator (CWG)	2	2
Zero-Cross Detect (ZCD)	1	1
Data Signal Modulator (DSM)	1	1
Reference Clock Output Module	1	1
Peripheral Pin Select (PPS)	YES	YES
Peripheral Module Disable (PMD)	YES	YES
Programmable Brown-out Reset (BOR)	YES	YES
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT
Instruction Set	50 instructions	50 instructions

8.1 Power-on Reset (POR)

The POR circuit holds the device in Reset until V_{DD} has reached an acceptable level for minimum operation. Slow rising V_{DD} , fast operating speeds or analog performance may require greater than minimum V_{DD} . The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

Related Links

[BOR Controlled by Software](#)

8.2 Brown-out Reset (BOR)

The BOR circuit holds the device in Reset when V_{DD} reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to “BOR Operating Conditions” table for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV<1:0> bits in Configuration Words.

A V_{DD} noise rejection filter prevents the BOR from triggering on small events. If V_{DD} falls below V_{BOR} for a duration greater than parameter T_{BORDC} , the device will reset.

8.2.1 BOR is Always On

When the BOREN bits of Configuration Words are programmed to ‘11’, the BOR is always on. The device start-up will be delayed until the BOR is ready and V_{DD} is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

8.2.2 BOR is OFF in Sleep

When the BOREN bits of Configuration Words are programmed to ‘10’, the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and V_{DD} is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

8.2.3 BOR Controlled by Software

When the BOREN bits of Configuration Words are programmed to ‘01’, the BOR is controlled by the [SBOREN](#) bit. The device start-up is not delayed by the BOR ready condition or the V_{DD} level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the [BORRDY](#) bit.

BOR protection is unchanged by Sleep.

Related Links

[OSCSTAT](#)

[OSCEN](#)

9.2.2.8 HFOR and MFOR Bits

The [HFOR](#) and [MFOR](#) bits indicate that the HFINTOSC and MFINTOSC is ready. These clocks are always valid for use at all times, but only accurate after they are ready.

When a new value is loaded into the OSCFRQ register, the HFOR and MFOR bits will clear, and set again when the oscillator is ready. During pending OSCFRQ changes the MFINTOSC clock will stall at a high or a low state, until the HFINTOSC resumes operation.

9.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the New Oscillator Source ([NOSC](#)) and New Divider selection request ([NDIV](#)) bits. The following clock sources can be selected:

- External Oscillator (EXTOSC)
- High-Frequency Internal Oscillator (HFINTOSC)
- Low-Frequency Internal Oscillator (LFINTOSC)
- Secondary Oscillator (SOSC)
- EXTOSC with 4x PLL
- HFINTOSC with 2x PLL

9.3.1 New Oscillator Source (NOSC) and New Divider Selection Request (NDIV) Bits

The New Oscillator Source (NOSC) and New Divider Selection Request (NDIV) bits select the system clock source and frequency that are used for the CPU and peripherals.

When new values of NOSC and NDIV are written to OSCCON1, the current oscillator selection will continue to operate while waiting for the new clock source to indicate that it is stable and ready. In some cases, the newly requested source may already be in use, and is ready immediately. In the case of a divider-only change, the new and old sources are the same, so the old source will be ready immediately. The device may enter Sleep while waiting for the switch.

When the new oscillator is ready, the New Oscillator Ready (NOSCR) bit is set and also the Clock Switch Interrupt Flag (CSWIF) bit of PIR1 sets. If Clock Switch Interrupts are enabled (CSWIE = 1), an interrupt will be generated at that time. The Oscillator Ready (ORDY) bit of OSCCON3 can also be polled to determine when the oscillator is ready in lieu of an interrupt.

If the Clock Switch Hold (CSWHOLD) bit is clear, the oscillator switch will occur when the New Oscillator is READY bit (NOSCR) is set, and the interrupt (if enabled) will be serviced at the new oscillator setting.

If CSWHOLD is set, the oscillator switch is suspended, while execution continues using the current (old) clock source. When the NOSCR bit is set, software should:

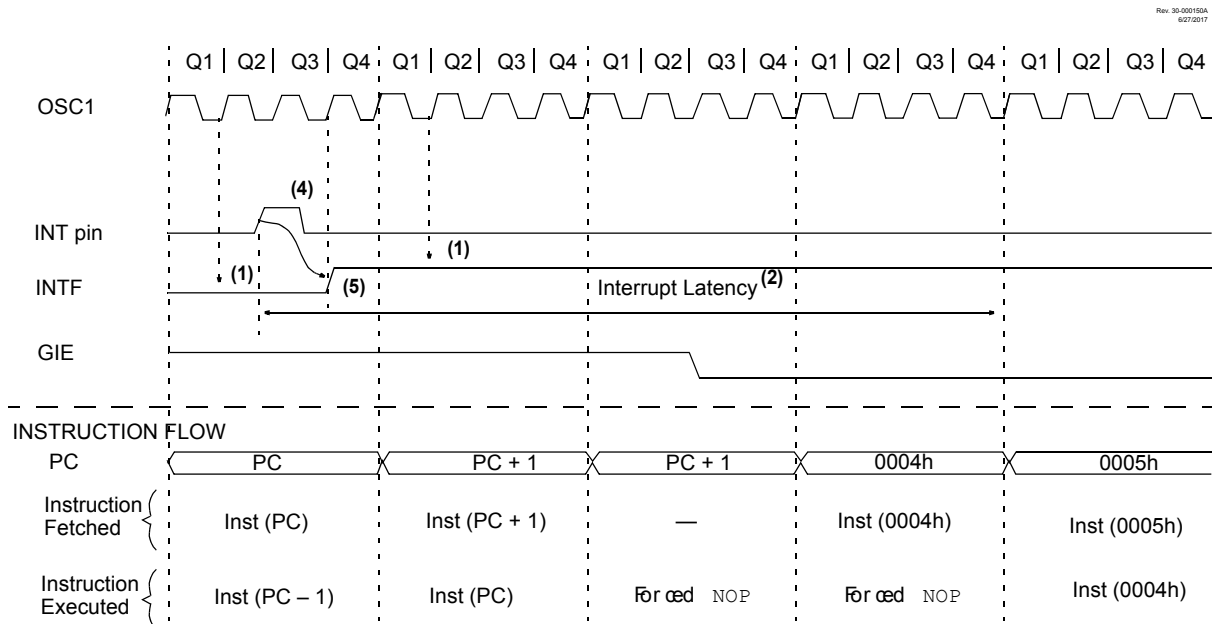
- Set CSWHOLD = 0 so the switch can complete, or
- Copy COSC into NOSC to abandon the switch.

If DOZE is in effect, the switch occurs on the next clock cycle, whether or not the CPU is operating during that cycle.

Changing the clock post-divider without changing the clock source (i.e., changing F_{OSC} from 1 MHz to 2 MHz) is handled in the same manner as a clock source change, as described previously. The clock

1. An interrupt may occur at any time during the interrupt window.
2. Since an interrupt may occur any time during the interrupt window, the actual latency can vary.

Figure 10-3. INT Pin Interrupt Timing



Note:

1. INTF flag is sampled here (every Q1).
2. Asynchronous interrupt latency = 3-5 T_{CY} . Synchronous latency = 3-4 T_{CY} , where T_{CY} = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3. For minimum width of INT pulse, refer to AC specifications in the “Electrical Specifications” section.
4. INTF may be set any time during the Q4-Q1 cycles.

10.3 Interrupts During Sleep

Interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the `SLEEP` instruction. The instruction directly after the `SLEEP` instruction will always be executed before branching to the ISR.

Related Links

[Power-Saving Operation Modes](#)

10.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. Refer to [Figure 10-3](#). This interrupt is enabled by setting the INTE bit of the PIE0 register. The INTEDG bit of the INTCON register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF

11.5.2 CPUDOZE

Name: CPUDOZE

Address: 0x88C

Doze and Idle Register

Bit	7	6	5	4	3	2	1	0
	IDLEN	DOZEN	ROI	DOE		DOZE[2:0]		
Access	R/W	R/W/HC/HS	R/W	R/W/HC/HS		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit 7 – IDLEN Idle Enable bit

Value	Description
1	A SLEEP instruction places device into IDLE mode
0	A SLEEP instruction places the device into Sleep mode

Bit 6 – DOZEN Doze Enable bit⁽¹⁾

Value	Description
1	Places devices into DOZE setting
0	Places devices into Normal mode

Bit 5 – ROI Recover-On-Interrupt bit⁽¹⁾

Value	Description
1	Entering the Interrupt Service Routine (ISR) makes DOZEN = 0
0	Entering the Interrupt Service Routine (ISR) does not change DOZEN

Bit 4 – DOE Doze-On-Exit bit⁽¹⁾

Value	Description
1	Executing the ISR makes DOZEN = 1
0	Exiting the ISR does not change DOZEN

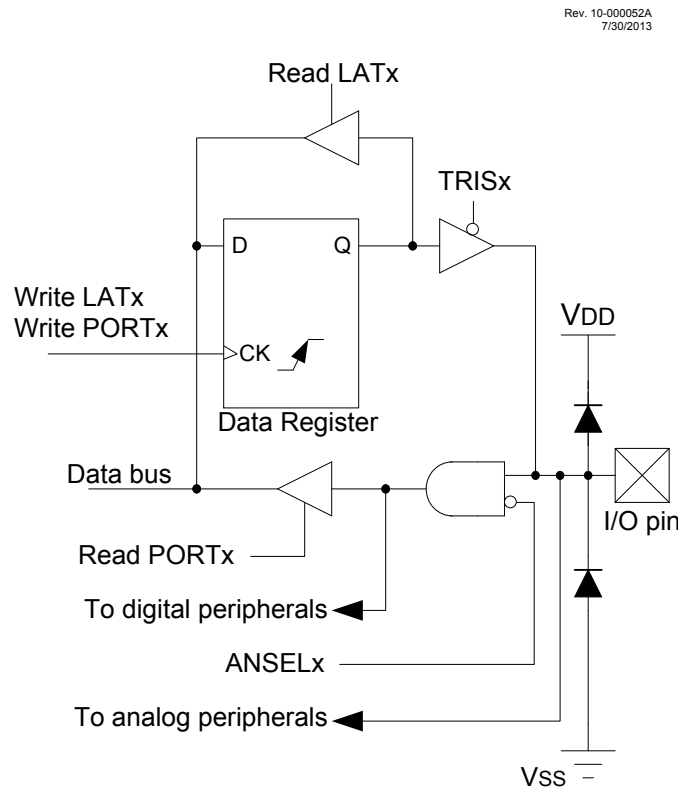
Bits 2:0 – DOZE[2:0] Ratio of CPU Instruction Cycles to Peripheral Instruction Cycles

Value	Description
111	1:256
110	1:128
101	1:64
100	1:32
011	1:16
010	1:8
001	1:4
000	1:2

Note:

1. See the link below for more details.

Figure 14-1. Generic I/O Port Operation



14.3 I/O Priorities

Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See “*Peripheral Pin Select (PPS) Module*” for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over digital outputs and force the digital output driver into a high-impedance state.

The pin function priorities are as follows:

1. Configuration bits
2. Analog outputs (disable the input buffers)
3. Analog inputs
4. Port inputs and outputs from PPS

Related Links

[\(PPS\) Peripheral Pin Select Module](#)

14.4 PORTx Registers

In this section the generic names such as PORTx, LATx, TRISx, etc. can be associated with PORTA, PORTB, PORTC, etc, depending on availability per device (see related link below).

14.6.22 INLVLA**Name:** INLVLA**Address:** 0x1F3C

Input Level Control Register

Bit	7	6	5	4	3	2	1	0
			INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 0, 1, 2, 3, 4, 5 – INLVLA_n Input Level Select on RA Pins

Value	Description
1	ST input used for port reads and interrupt-on-change
0	TTL input used for port reads and interrupt-on-change

16.5.3 PMD2

Name: PMD2

Address: 0x798

PMD Control Register 2

Bit	7	6	5	4	3	2	1	0
	NCO1MD							
Access	R/W							
Reset	0							

Bit 7 – NCO1MD Disable Numerically Control Oscillator bit

Value	Description
1	NCO1 module disabled
0	NCO1 module enabled

16.5.4 PMD3

Name: PMD3

Address: 0x799

PMD Control Register 3

Bit	7	6	5	4	3	2	1	0
		DAC1MD	ADCMD			C2MD	C1MD	ZCDMD
Access		R/W	R/W			R/W	R/W	R/W
Reset		0	0			0	0	0

Bit 6 – DAC1MD Disable DAC1 bit

Value	Description
1	DAC module disabled
0	DAC module enabled

Bit 5 – ADCMD Disable ADC bit

Value	Description
1	ADC module disabled
0	ADC module enabled

Bit 2 – C2MD Disable Comparator C2 bit

Value	Description
1	C2 module disabled
0	C2 module enabled

Bit 1 – C1MD Disable Comparator C1 bit

Value	Description
1	C1 module disabled
0	C1 module enabled

Bit 0 – ZCDMD Disable Zero-Cross Detect module bit

Value	Description
1	ZCD module disabled
0	ZCD module enabled

17.6.9 IOCCF

Name: IOCCF
Address: 0x1F55

PORTC Interrupt-on-Change Flag Register

Bit	7	6	5	4	3	2	1	0
	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
Access	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS	R/W/HS
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – IOCCFn Interrupt-on-Change Flag bits

Value	Condition	Description
1	IOCCP[n]=1	A positive edge was detected on the RC[n] pin
1	IOCCN[n]=1	A negative edge was detected on the RC[n] pin
0	IOCCP[n]=x and IOCCN[n]=x	No change was detected, or the user cleared the detected change

Note: IOCCF6 and IOCCF7 are available on 20-pin or higher pin-count devices only.

20.8.5 ADSTAT

Name: ADSTAT

Address: 0x115

ADC Status Register

Bit	7	6	5	4	3	2	1	0
	OV	UTHR	LTHR	MATH		STAT[2:0]		
Access	RO	RO	RO	R/HS/HC		RO	RO	RO
Reset	0	0	0	0		0	0	0

Bit 7 – OV ADC Accumulator Overflow bit

Value	Description
1	ADC accumulator or ERR calculation have overflowed
0	ADC accumulator and ERR calculation have not overflowed

Bit 6 – UTHR ADC Module Greater-than Upper Threshold Flag bit

Value	Description
1	ERR > UTH
0	ERR ≤ UTH

Bit 5 – LTHR ADC Module Less-than Lower Threshold Flag bit

Value	Description
1	ERR < LTH
0	ERR ≥ LTH

Bit 4 – MATH ADC Module Computation Status bit

Value	Description
1	Registers ADACC, ADFLTR, ADUTH, ADLTH and the OV bit are updating or have already updated
0	Associated registers/bits have not changed since this bit was last cleared

Bits 2:0 – STAT[2:0] ADC Module Cycle Multistage Status bits⁽¹⁾

Value	Description
111	ADC module is in 2 nd conversion stage
110	ADC module is in 2 nd acquisition stage
101	ADC module is in 2 nd precharge stage
100	Not used
011	ADC module is in 1 st conversion stage
010	ADC module is in 1 st acquisition stage
001	ADC module is in 1 st precharge stage
000	ADC module is not converting

Note:

1. If CS = 1, and F_{OSC} < FRC, these bits may be invalid.

C = series capacitor

R = series resistor

V_C = Peak capacitor voltage

Φ = Capacitor induced zero crossing phase advance in radians

T_Φ = Time ZC event occurs before actual zero crossing

$$Z = \frac{V_{PEAK}}{3 \times 10^{-4}}$$

$$X_C = \frac{1}{2\pi fC}$$

$$R = \sqrt{Z^2 - X_C^2}$$

$$V_C = X_C(3 \times 10^{-4})$$

$$\Phi = \tan^{-1}\theta\left(\frac{X_C}{R}\right)$$

$$T_\Phi = \frac{\Phi}{2\pi f}$$

Equation 24-3. R-C Calculation Example

$$V_{rms} = 120$$

$$V_{PEAK} = V_{rms} \times \sqrt{2} = 169.7$$

$$f = 60 \text{ Hz}$$

$$C = 0.1 \mu F$$

$$Z = \frac{V_{PEAK}}{3 \times 10^{-4}} = \frac{169.7}{3 \times 10^{-4}} = 565.7 \text{ k}\Omega$$

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 60 \times 10^{-7}} = 26.53 \text{ k}\Omega$$

$$R = \sqrt{Z^2 - X_C^2} = 565.1 \text{ k}\Omega \text{ (computed)}$$

$$R_a = 560 \text{ k}\Omega \text{ (used)}$$

$$Z_R = \sqrt{R_a^2 + X_C^2} = 560.6 \text{ k}\Omega$$

$$I_{PEAK} = \frac{V_{PEAK}}{Z_R} = 302.7 \times 10^{-6} \text{ A}$$

$$V_C = X_C \times I_{PEAK} = 8.0 \text{ V}$$

$$\Phi = \tan^{-1}\theta\left(\frac{X_C}{R}\right) = 0.047 \text{ radians}$$

T0CS	Clock Source
001	Pin selected by T0CKIPPS (Inverted)
000	Pin selected by T0CKIPPS (Noninverted)

25.2.2 Synchronous Mode

When the [T0ASYNC](#) bit is clear, Timer0 clock is synchronized to the system clock ($F_{OSC}/4$). When operating in Synchronous mode, Timer0 clock frequency cannot exceed $F_{OSC}/4$. During Sleep mode system clock is not available and Timer0 cannot operate.

25.2.3 Asynchronous Mode

When the [T0ASYNC](#) bit is set, Timer0 increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows Timer0 to continue operation during Sleep mode provided the selected clock source is available.

25.2.4 Programmable Prescaler

Timer0 has 16 programmable input prescaler options ranging from 1:1 to 1:32768. The prescaler values are selected using the [T0CKPS](#) bits.

The prescaler counter is not directly readable or writable. The prescaler counter is cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset

Related Links

[Resets](#)

25.3 Timer0 Output and Interrupt

25.3.1 Programmable Postscaler

Timer0 has 16 programmable output postscaler options ranging from 1:1 to 1:16. The postscaler values are selected using the [T0OUTPS](#) bits. The postscaler divides the output of Timer0 by the selected ratio.

The postscaler counter is not directly readable or writable. The postscaler counter is cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset

25.3.2 Timer0 Output

TMR0_out is the output of the postscaler. TMR0_out toggles on every match between TMR0L and TMR0H in 8-bit mode, or when TMR0H:TMR0L rolls over in 16-bit mode. If the output postscaler is used, the output is scaled by the ratio selected.

The Timer0 output can be routed to an I/O pin via the RxyPPS output selection register. The Timer0 output can be monitored through software via the [T0OUT](#) output bit.

Related Links

25.5 Register Summary - Timer0

Offset	Name	Bit Pos.							
0x059C	TMR0L	7:0	TMR0L[7:0]						
0x059D	TMR0H	7:0	TMR0H[7:0]						
0x059E	T0CON0	7:0	T0EN		T0OUT	T016BIT	T0OUTPS[3:0]		
0x059F	T0CON1	7:0	T0CS[2:0]			T0ASYNC	T0CKPS[3:0]		

25.6 Register Definitions: Timer0 Control

PIC16(L)F18426/46

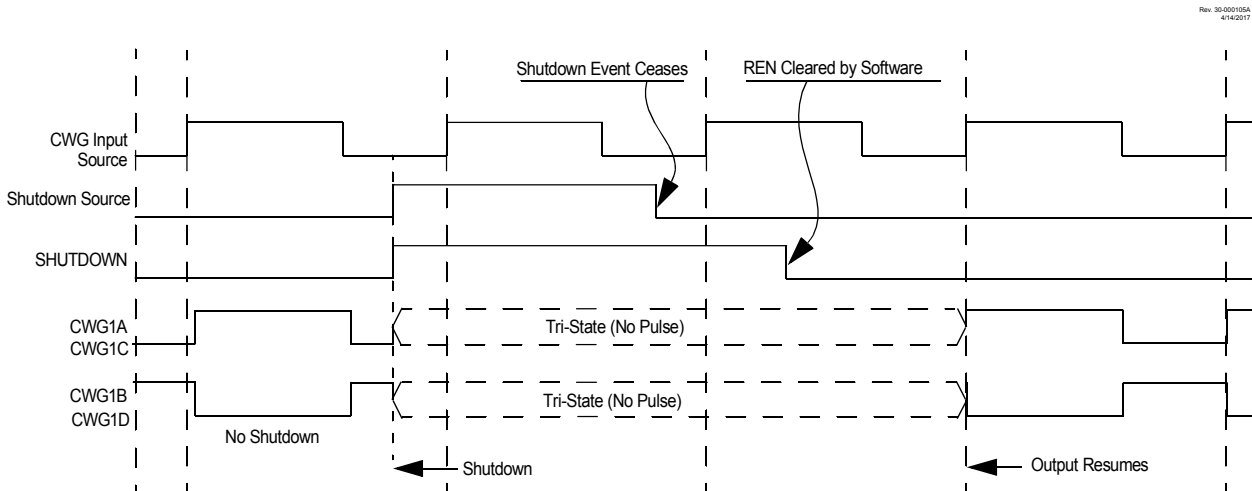
(CWG) Complementary Waveform Generator Modul...

Once all auto-shutdown sources are removed, the software must clear SHUTDOWN. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.



Important: The SHUTDOWN bit cannot be cleared in software if the auto-shutdown condition is still present.

Figure 31-17. SHUTDOWN FUNCTIONALITY, AUTO-RESTART DISABLED (REN = 0, LSAC = 01, LSBD = 01)



31.11.2.2 Auto-Restart

When the REN bit is set (REN = 1), the CWG module will restart from the shutdown state automatically.

Once all auto-shutdown conditions are removed, the hardware will automatically clear SHUTDOWN. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.



Important: The SHUTDOWN bit cannot be cleared in software if the auto-shutdown condition is still present.

31.15.9 CWGxDBF

Name: CWGxDBF
Address: 0x60F,0x619

CWG Falling Dead-Band Count Register

Bit	7	6	5	4	3	2	1	0
			DBF[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x

Bits 5:0 – DBF[5:0] CWG Falling Edge Triggered Dead-Band Count bits
 Reset States: POR/BOR = xxxxxx
 All Other Resets = uuuuuu

Value	Description
n	Dead band is active no less than n, and no more than n+1, CWG clock periods after the falling edge
0	0 CWG clock periods. Dead-band generation is bypassed

35.4.2 Arbitration

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.

35.4.3 Byte Format

All communication in I²C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

35.4.4 Definition of I²C Terminology

There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I²C specification.

TERM	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.

36.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

36.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCxSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCxIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

36.1.2.8 Asynchronous Reception Setup

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see the [EUSART Baud Rate Generator \(BRG\)](#) section).
2. Set the RXxPPS register to select the RXx/DTx input pin.
3. Clear the ANSEL bit for the RXx pin (if applicable).
4. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
5. If interrupts are desired, set the RCxIE bit of the PEx register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set the RX9 bit.
7. Enable reception by setting the CREN bit.
8. The RCxIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit was also set.
9. Read the RCxSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

36.1.2.9 9-Bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable follow these steps:

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see the [EUSART Baud Rate Generator \(BRG\)](#) section).
2. Set the RXxPPS register to select the RXx input pin.
3. Clear the ANSEL bit for the RXx pin (if applicable).
4. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.

PIC16F18426/46 only								
Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Device Characteristics	Min.	Typ.†	Max.	Units	Conditions	
							V _{DD}	Note
D102	I _{DDHFOPLL}	HFINTOSC = 32 MHz	—	3.7	5.6	mA	3.0V	
D103	I _{DDHSPLL32}	HS+PLL = 32 MHz	—	3.7	5.7	mA	3.0V	
D104	I _{DDIDLE}	IDLE mode, HFINTOSC = 16 MHz	—	1.8	2.1	mA	3.0V	
D105	I _{DDDOZE} ⁽³⁾	DOZE mode, HFINTOSC = 16 MHz, Doze Ratio = 16	—	1.6	—	mA	3.0V	

† - Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:

1. The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins are outputs driven low; $\overline{\text{MCLR}} = \text{V}_{\text{DD}}$; WDT disabled.
2. The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
3. $I_{\text{DDDOZE}} = [I_{\text{DDIDLE}} * (\text{N}-1)/\text{N}] + I_{\text{DDHFO}} / 16$ where N = DOZE Ratio (see CPUDOZE register).
4. PMD bits are all in the default state, no modules are disabled.

Related Links

[CPUDOZE](#)

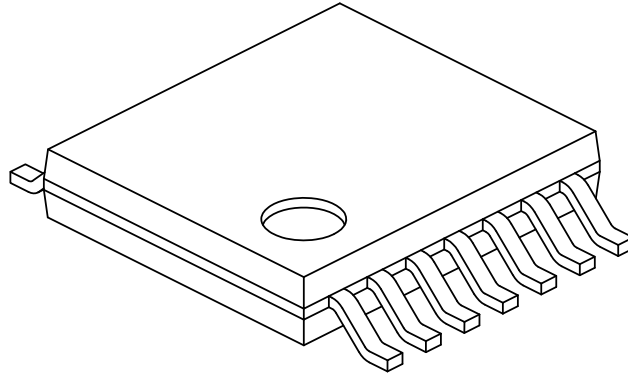
42.3.3 Power-Down Current (I_{PD})^(1,2)

Table 42-3.

PIC16LF18426/46 only									
Standard Operating Conditions (unless otherwise stated)									
Param. No.	Sym.	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions	
								V _{DD}	Note
D200	I _{PD}	I _{PD} Base	—	0.06	2	9	μA	3.0V	
D201	I _{PD_WDT}	Low-Frequency Internal Oscillator/WDT	—	0.8	4.0	11	μA	3.0V	

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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