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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18446t-i-ss

10.7.11 PIR0

Name: PIR0
Address: 0x70C

Peripheral Interrupt Request (Flag) Register 0

Bit	7	6	5	4	3	2	1	0
			TMR0IF	IOCIF				INTF
Access			R/W/HS	RO				R/W/HS
Reset			0	0				0

Bit 5 – TMR0IF Timer0 Interrupt Flag bit

Value	Description
1	TMR0 register has overflowed (must be cleared by software)
0	TMR0 register has not overflowed

Bit 4 – IOCIF Interrupt-on-Change Flag bit(2)

Value	Description
1	One or more of the IOCAF-IOCEF register bits are currently set, indicating an enabled edge was detected by the IOC module.
0	None of the IOCAF-IOCEF register bits are currently set

Bit 0 – INTF External Interrupt Flag bit(1)

Value	Description
1	External Interrupt has occurred
0	External Interrupt has not occurred

Note:

1. The External Interrupt INT pin is selected by INTPPS.
2. The IOCIF bit is the logical OR of all the IOCAF-IOCEF flags. Therefore, to clear the IOCIF flag, application firmware must clear all of the lower level IOCAF-IOCEF register bits.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON appropriate interrupt flag bits are clear prior to enabling an interrupt.

Related Links

xxxPPS

Value	Condition	Description
1	PWM mode	Output trailing edge occurred (must be cleared in software)
0	PWM mode	Output trailing edge did not occur

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON appropriate interrupt flag bits are clear prior to enabling an interrupt.

```
BANKSEL     NVMADRL
MOVF        ADDRL,W
MOVWF       NVMADRL           ; Load lower 8 bits of erase address boundary
MOVF        ADDRH,W
MOVWF       NVMADRH           ; Load upper 6 bits of erase address boundary
BCF         NVMCON1,NVMREGS   ; Choose PFM memory area
BSF         NVMCON1,FREE      ; Specify an erase operation
BSF         NVMCON1,WREN      ; Enable writes
BCF         INTCON,GIE        ; Disable interrupts during unlock sequence

; ---------------------REQUIRED UNLOCK SEQUENCE:--------------------

MOVLW       55h               ; Load 55h to get ready for unlock sequence
MOVWF       NVMCON2           ; First step is to load 55h into NVMCON2
MOVLW       AAh               ; Second step is to load AAh into W
MOVWF       NVMCON2           ; Third step is to load AAh into NVMCON2
BSF         NVMCON1,WR        ; Final step is to set WR bit

; ---------------------------------------------------------------------

BSF         INTCON,GIE        ; Re-enable interrupts, erase is complete
BCF         NVMCON1,WREN      ; Disable writes
```

Table 13-1. NVM Organization and Access Information

Master Values				NVMREG Access			FSR Access	
Memory Function	Memory Type	Program Counter (PC)	ICSP Address	NVMREGS bit (NVMCON1)	NVMADR<14:0>	Allowed Operations	FSR Address	FSR Programming Access
RESET VECTOR	Program Flash Memory	0000h	0000h	0	0000h	READ/ WRITE	8000h	READ ONLY
USER MEMORY		0001h	0001h	0	0001h		8001h	
		0003h	0003h		0003h		8003h	
INT VECTOR		0004h	0004h	0	0004h		8004h	
USER MEMORY		0005h	0005h	0	0005h		8005h	
		7FFFh(1)	7FFFh(1)		7FFFh(1)		FFFFh	
USER ID	Program Flash Memory	NO PC ACCESS	8000h	1	0000h	READ	NO ACCESS	
			8003h		0003h			
Reserved	—		—	—	0004h	—		
REV ID	HC		8005h	1	0005h	READ		
DEVICE ID			8006h	1	0006h			
CONFIG1	FUSE		8007h	1	0007h	READ/ WRITE		
CONFIG2			8008h	1	0008h			
CONFIG3			8009h	1	0009h			
CONFIG4			800Ah	1	000Ah			
CONFIG5			800Bh	1	000Bh			
DIA and DCI	PFM		8100h	1	0100h	READ		
			82FFh	1	02FFh			
USER MEMORY	EEPROM		F000h	1	7000h	READ/ WRITE	7000h	READ ONLY
			F0FFh		70FFh		70FFh	

16.5.3 PMD2

Name: PMD2
Address: 0x798

PMD Control Register 2

Bit	7	6	5	4	3	2	1	0
	NCO1MD							
Access	R/W							
Reset	0							

Bit 7 – NCO1MD Disable Numerically Control Oscillator bit

Value	Description
1	NCO1 module disabled
0	NCO1 module enabled

20.8.17 ADACC

Name: ADACC
Address: 0x096

ADC Accumulator Register
See Computation Modes for more details.

Bit	23	22	21	20	19	18	17	16
							ACCU[1:0]	
Access							R/W	R/W
Reset							x	x

Bit	15	14	13	12	11	10	9	8
	ACCH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	ACCL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 17:16 – ACCU[1:0]
ADC Accumulator MSB. Upper two bits of accumulator value.

Bits 15:8 – ACCH[7:0]
ADC Accumulator middle bits. Higher eight bits of accumulator value.

Bits 7:0 – ACCL[7:0]
ADC Accumulator LSB. Lower eight bits of accumulator value.

23.2.1 Comparator Enable

Setting the EN bit enables the comparator for operation. Clearing the CxEN bit disables the comparator, resulting in minimum current consumption.

23.2.2 Comparator Output

The output of the comparator can be monitored by reading either the CxOUT bit or the MCxOUT bit.

The comparator output can also be routed to an external pin through the RxyPPS register. The corresponding TRIS bit must be clear to enable the pin as an output.

Note:

1. The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

Related Links

RxyPPS

23.2.3 Comparator Output Polarity

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit. Clearing the CxPOL bit results in a non-inverted output.

Table 23-1 shows the output state versus input conditions, including polarity control.

Table 23-1. Comparator Output State vs. Input Conditions

Input Condition	CxPOL	CxOUT
CxVn > CxVp	0	0
CxVn < CxVp	0	1
CxVn > CxVp	1	1
CxVn < CxVp	1	0

23.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit.

See Comparator Specifications for more information.

Related Links

Comparator Specifications

23.4 Operation With Timer1 Gate

The output resulting from a comparator operation can be used as a source for gate control of the odd numbered timers (Timer1, Timer3, etc.). See the timer gate section for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to the timer by setting the SYNC bit. This ensures that the timer does not increment while a change in the comparator is occurring. However,

23.15.3 CMxNCH

Name: CMxNCH
Address: 0x992,0x996

Comparator x Inverting Channel Select Register

Bit	7	6	5	4	3	2	1	0
						NCH[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – NCH[2:0] Comparator Inverting Input Channel Select bits

NCH	Negative Input Sources
111	CxV_N connects to AV_{SS}
110	CxV_N connects to FVR Buffer 2
101	CxV_N not connected
100	CxV_N not connected
011	CxV_N connects to CxIN3- pin
010	CxV_N connects to CxIN2- pin
001	CxV_N connects to CxIN1- pin
000	CxV_N connects to CxIN0- pin

25.1 Timer0 Operation

Timer0 can operate as either an 8-bit or 16-bit timer. The mode is selected with the T016BIT bit.

25.1.1 8-bit Mode

In this mode Timer0 increments on the rising edge of the selected clock source. A prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS).

In this mode as shown in the 8-bit TMR0 Body Diagram, a buffered version of TMR0H is maintained. This is compared with the value of TMR0L on each cycle of the selected clock source. When the two values match, the following events occur:

- TMR0L is reset
- The contents of TMR0H are copied to the TMR0H buffer for next comparison

25.1.2 16-Bit Mode

In this mode Timer0 increments on the rising edge of the selected clock source. A prescaler on the clock input gives several prescale options (see prescaler control bits, T0CKPS).

In this mode TMR0H:TMR0L form the 16-bit timer value. As shown in the 16-bit TMR0 Body Diagram, read and write of the TMR0H register are buffered. TMR0H register is updated with the contents of the high byte of Timer0 during a read of TMR0L register. Similarly, a write to the high byte of Timer0 takes place through the TMR0H buffer register. The high byte is updated with the contents of TMR0H register when a write occurs to TMR0L register. This allows all 16 bits of Timer0 to be read and written at the same time.

Timer 0 rolls over to 0x0000 on incrementing past 0xFFFF. This makes the timer free running. TMR0L/H registers cannot be reloaded in this mode once started.

25.2 Clock Selection

Timer0 has several options for clock source selections, option to operate synchronously/asynchronously and a programmable prescaler.

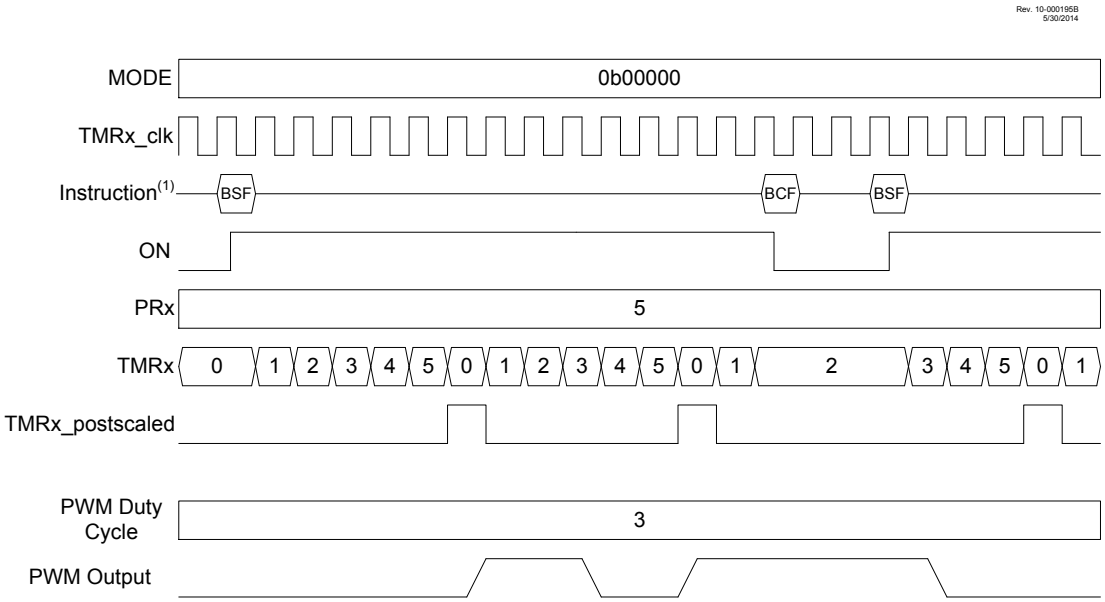
25.2.1 Clock Source Selection

The T0CS bits are used to select the clock source for Timer0. The possible clock sources are listed in the table below.

Table 25-1. Timer0 Clock Source Selections

T0CS	Clock Source
111	CLC1_out
110	SOSC
101	MFINTOSC(500 kHz)
100	LFINTOSC
011	HFINTOSC
010	$F_{OSC}/4$

Figure 27-3. Software Gate Mode Timing Diagram (MODE = 00000)



Note:

1. BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

Related Links

PWM Overview

(PWM) Pulse-Width Modulation

27.6.2 Hardware Gate Mode

The Hardware Gate modes operate the same as the Software Gate mode except the TMRx_ers external signal can also gate the timer. When used with the CCP, the gating extends the PWM period. If the timer is stopped when the PWM output is high, then the duty cycle is also extended.

When MODE<4:0> = `00001` then the timer is stopped when the external signal is high. When MODE<4:0> = `00010`, then the timer is stopped when the external signal is low.

Figure 27-4 illustrates the Hardware Gating mode for MODE<4:0> = `00001` in which a high input level starts the counter.

28. CCP/PWM Timer Resource Selection

Each CCP/PWM module has an independent timer selection which can be accessed using the CxTSEL or PxTSEL bits in the CCPTMRS0 and/or CCPTMRS1 registers. The default timer selection is TMR1 when using Capture/Compare mode and T2TMR when using PWM mode in the CCPx module. The default timer selection for the PWM module is always T2TMR.

6. Enable PWM output pin:
   – Wait until the Timer overflows and the TMR2IF bit of the PIRx register is set. See Note below.
   – Enable the CCPx pin output driver by clearing the associated TRIS bit.

Important: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

Related Links

TxCON

29.4.3 Timer2 Timer Resource

The PWM standard mode makes use of the 8-bit Timer2 timer resources to specify the PWM period.

29.4.4 PWM Period

The PWM period is specified by the T2PR register of Timer2. The PWM period can be calculated using the formula in the equation below.

Equation 29-1. PWM Period

$$PWMPeriod = [(T2PR + 1)] \bullet 4 \bullet T_{OSC} \bullet \left(TMR2\mathrm{Pr}escaleValue\right)$$

where $T_{OSC} = 1/F_{OSC}$

When T2TMR is equal to T2PR, the following three events occur on the next increment cycle:

- T2TMR is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is transferred from the CCPRx register into a 10-bit buffer.

Important: The Timer postscaler (see *"Timer2 Interrupt"*) is not used in the determination of the PWM frequency.

Related Links

Timer2 Interrupt

29.4.5 PWM Duty Cycle

The PWM duty cycle is specified by writing a 10-bit value to the CCPRx register. The alignment of the 10-bit value is determined by the FMT bit (see Figure 29-6). The CCPRx register can be written to at any time. However, the duty cycle value is not latched into the 10-bit buffer until after a match between T2PR and T2TMR.

The equations below are used to calculate the PWM pulse width and the PWM duty cycle ratio.

32.12.2 MDxCON1

Name: MDxCON1
Address: 0x0898

Modulation Control Register 1

Bit	7	6	5	4	3	2	1	0
			CHPOL	CHSYNC			CLPOL	CLSYNC
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit 5 – CHPOL Modulator High Carrier Polarity Select bit

Value	Description
1	Selected high carrier signal is inverted
0	Selected high carrier signal is not inverted

Bit 4 – CHSYNC Modulator High Carrier Synchronization Enable bit

Value	Description
1	Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
0	Modulator output is not synchronized to the high time carrier signal

Bit 1 – CLPOL Modulator Low Carrier Polarity Select bit

Value	Description
1	Selected low carrier signal is inverted
0	Selected low carrier signal is not inverted

Bit 0 – CLSYNC Modulator Low Carrier Synchronization Enable bit

Value	Description
1	Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier
0	Modulator output is not synchronized to the low time carrier signal

Note:

1. Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

34. Reference Clock Output Module

The reference clock output module provides the ability to send a clock signal to the clock reference output pin (CLKR). The reference clock output can also be routed internally as a signal for other peripherals, such as the Data Signal Modulator (DSM), Memory Scanner, and Timer module.

The reference clock output module has the following features:

- Selectable clock source using the CLKRCLK register
- Programmable clock divider
- Selectable duty cycle

Figure 34-1. Clock Reference Block Diagram

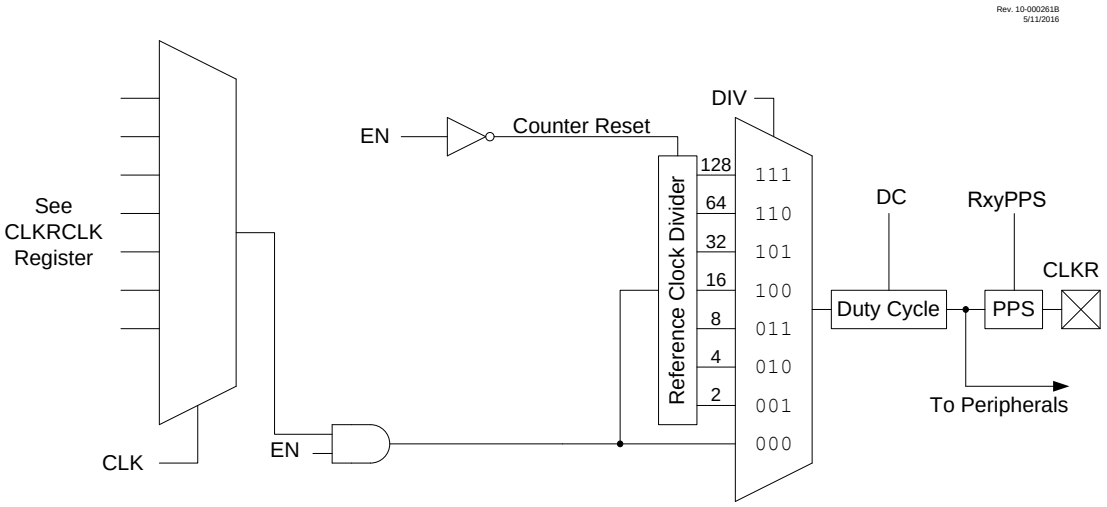
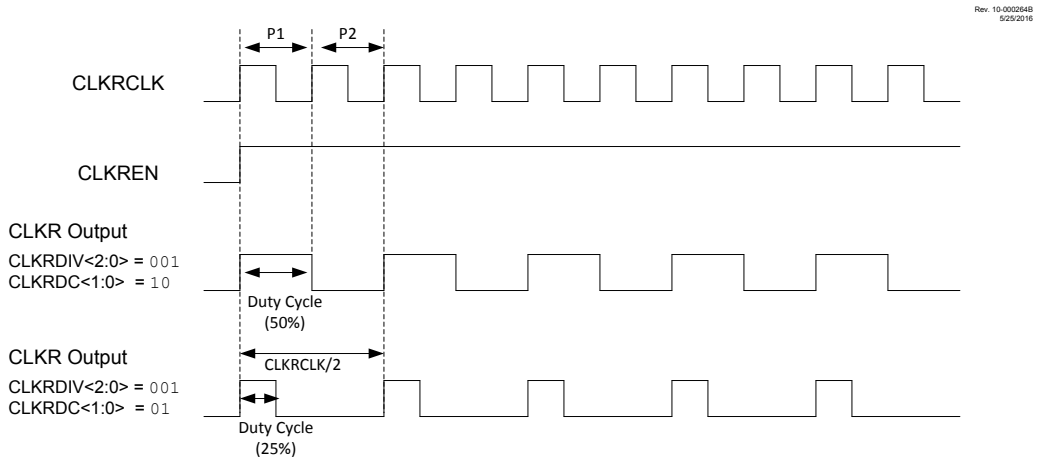


Figure 34-2. Clock Reference Timing



mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

35.3.1 Register Definitions: I²C Mode

The MSSPx module has seven registers for I²C operation.

These are:

- MSSP Status Register (SSPxSTAT)
- MSSP Control Register 1 (SSPxCON1)
- MSSP Control Register 2 (SSPxCON2)
- MSSP Control Register 3 (SSPxCON3)
- Serial Receive/Transmit Buffer Register (SSPxBUF)
- MSSP Address Register (SSPxADD)
- I²C Slave Address Mask Register (SSPxMSK)
- MSSP Shift Register (SSPSR) – not directly accessible

SSPxCON1, SSPxCON2, SSPxCON3 and SSPxSTAT are the Control and Status registers in I²C mode operation. The SSPxCON1, SSPxCON2, and SSPxCON3 registers are readable and writable. The lower six bits of the SSPxSTAT are read-only. The upper two bits of the SSPxSTAT are read/write. SSPSR is the Shift register used for shifting data in or out. SSPxBUF is the buffer register to which data bytes are written to or read from. SSPxADD contains the slave device address when the MSSP is configured in I²C Slave mode. When the MSSP is configured in Master mode, the lower seven bits of SSPxADD act as the Baud Rate Generator reload value.

SSPxMSK holds the slave address mask value when the module is configured for 7-Bit Address Masking mode. While it is a separate register, it shares the same SFR address as SSPxADD; it is only accessible when the SSPM<3:0> bits are specifically set to permit access. In receive operations, SSPSR and SSPxBUF together, create a double-buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPxBUF and the SSPxIF interrupt is set. During transmission, the SSPxBUF is not double-buffered. A write to SSPxBUF will write to both SSPxBUF and SSPSR.

35.4 I²C Mode Operation

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC® microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

35.4.1 Clock Stretching

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

Figure 35-29. I²C Master Mode Waveform (Reception, 7-bit Address)

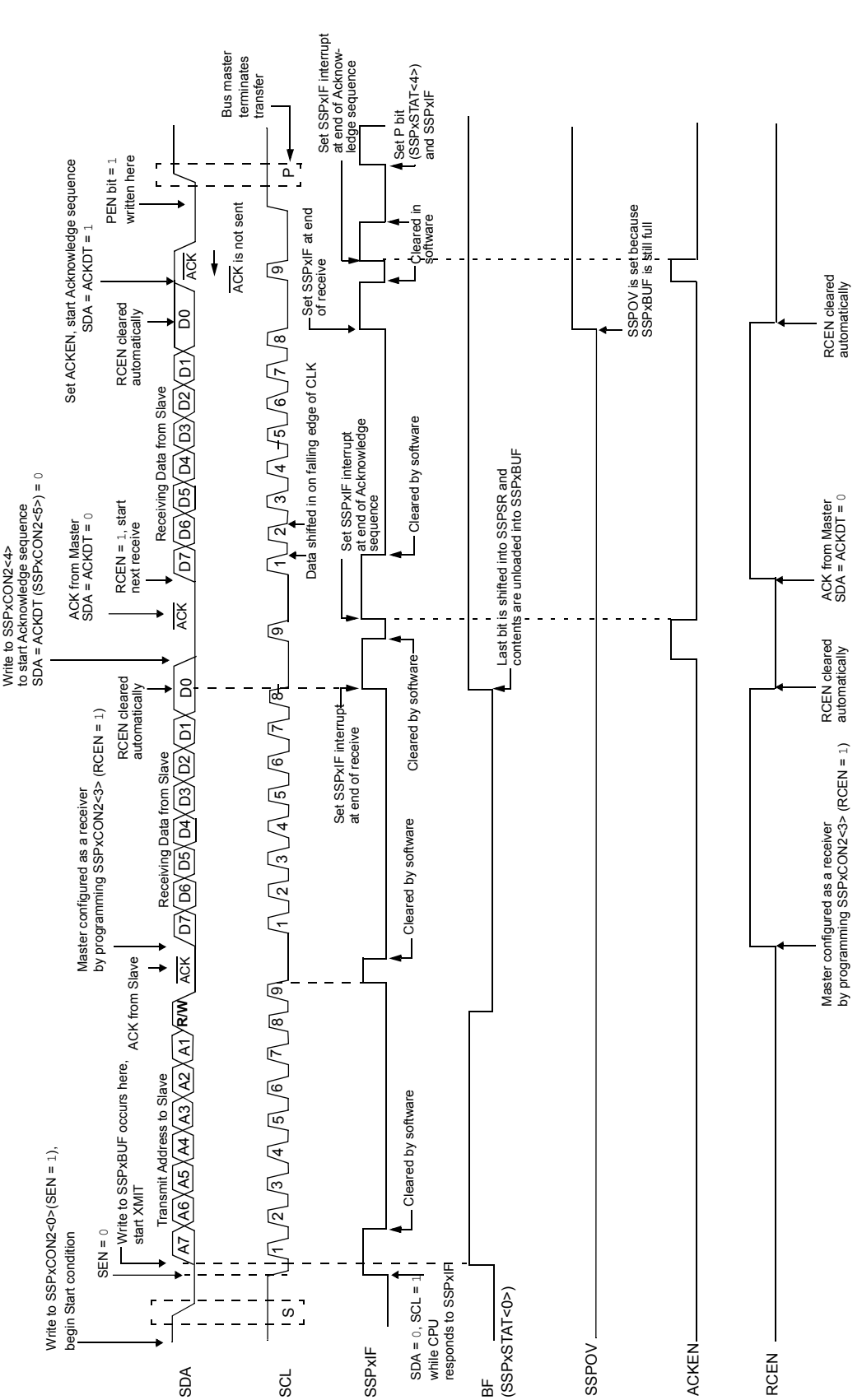


Figure 37-7. High and Low Measurement Mode, Repeat Acquisition Timing Diagram

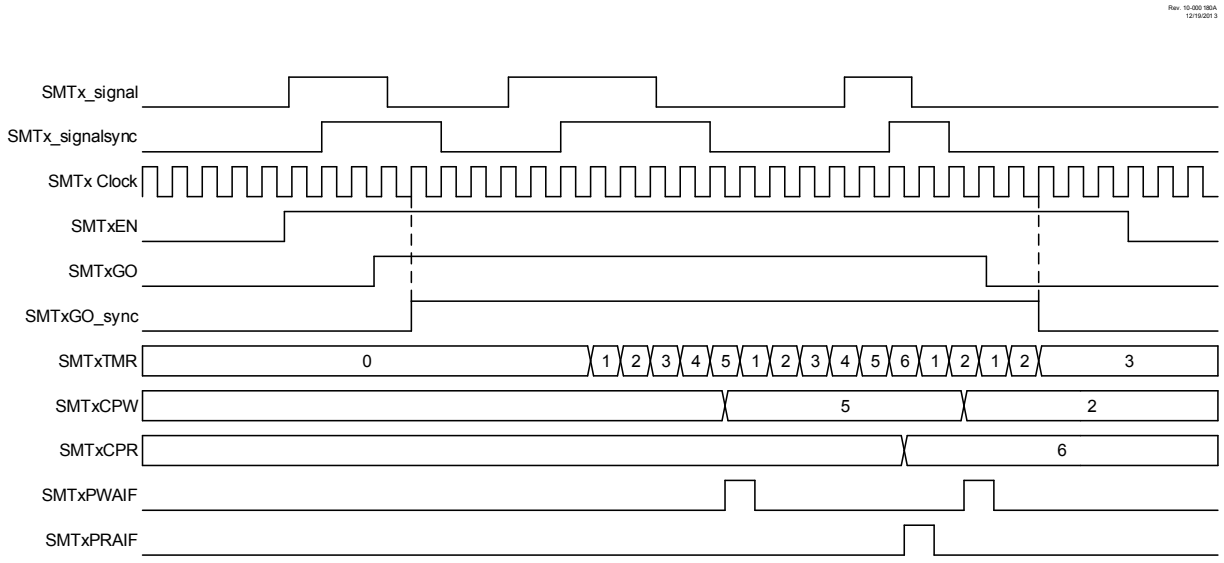
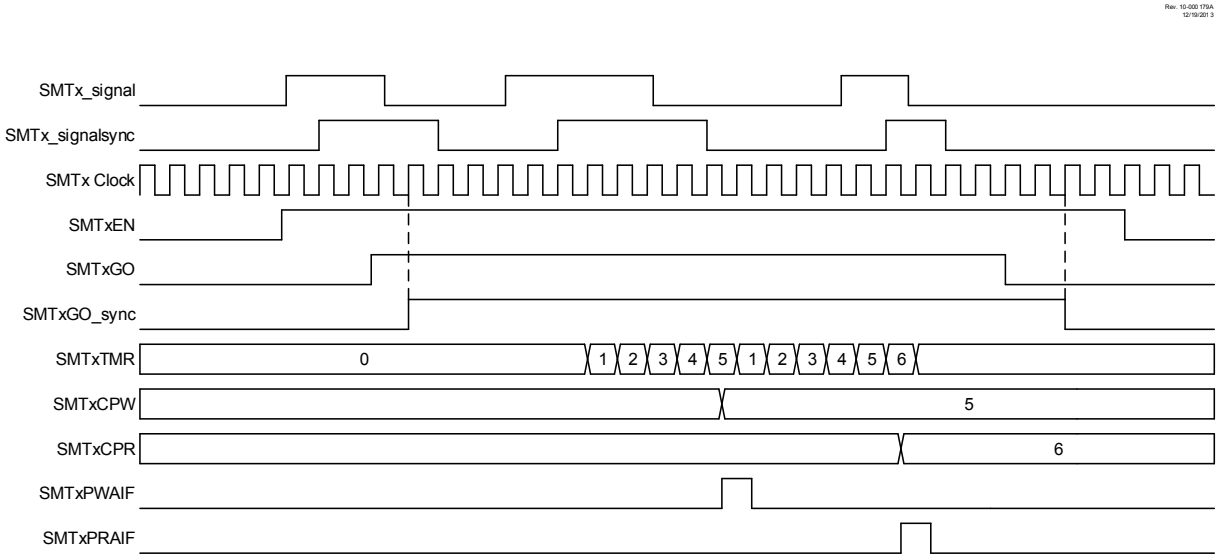


Figure 37-8. High and Low Measurement Mode, Single Acquisition Timing Diagram



37.1.6.5 Windowed Measurement Mode

This mode measures the duration of the window input (WSEL) to the SMT. It begins incrementing the timer on a rising edge of the window input and updates the SMTxCPR register with the value of the timer and resets the timer on a second rising edge. See figures below.

37.3.2 SMTxCON1

Name: SMTxCON1
Address: 0x0499

SMT Control Register 1

Bit	7	6	5	4	3	2	1	0
	GO	REPEAT			MODE[3:0]			
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit 7 – GO SMT GO Data Acquisition Bit

Value	Description
1	Incrementing, acquiring data is enabled
0	Incrementing, acquiring data is disabled

Bit 6 – REPEAT SMT Repeat Acquisition Enable Bit

Value	Description
1	Repeat Data Acquisition mode is enabled
0	Single Acquisition mode is enabled

Bits 3:0 – MODE[3:0] SMT Operation Mode Select bits

Value	Description
1111	Reserved
1110	Reserved
1101	Reserved
1100	Reserved
1011	Reserved
1010	Windowed counter
1001	Gated counter
1000	Counter
0111	Capture
0110	Time of flight
0101	Gated windowed measurement
0100	Windowed measurement
0011	High and low time measurement
0010	Period and Duty-Cycle Acquisition
0001	Gated Timer
0000	Timer

38. Register Summary

Offset	Name	Bit Pos.								
0x00	INDF0	7:0	INDF0[7:0]							
0x01	INDF1	7:0	INDF1[7:0]							
0x02	PCL	7:0	PCL[7:0]							
0x03	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x04	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x06	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x08	BSR	7:0			BSR[5:0]					
0x09	WREG	7:0	WREG[7:0]							
0x0A	PCLATH	7:0		PCLATH[6:0]						
0x0B	INTCON	7:0	GIE	PEIE						INTEDG
0x0C	PORTA	7:0			RA5	RA4	RA3	RA2	RA1	RA0
0x0D	PORTB	7:0	RB7	RB6	RB5	RB4				
0x0E	PORTC	7:0	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
0x0F ... 0x11	Reserved									
0x12	TRISA	7:0			TRISA5	TRISA4		TRISA2	TRISA1	TRISA0
0x13	TRISB	7:0	TRISB7	TRISB6	TRISB5	TRISB4				
0x14	TRISC	7:0	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
0x15 ... 0x17	Reserved									
0x18	LATA	7:0			LATA5	LATA4		LATA2	LATA1	LATA0
0x19	LATB	7:0	LATB7	LATB6	LATB5	LATB4				
0x1A	LATC	7:0	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
0x1B ... 0x7F	Reserved									
0x80	INDF0	7:0	INDF0[7:0]							
0x81	INDF1	7:0	INDF1[7:0]							
0x82	PCL	7:0	PCL[7:0]							
0x83	STATUS	7:0				$\overline{TO}$	$\overline{PD}$	Z	DC	C
0x84	FSR0	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x86	FSR1	7:0	FSRL[7:0]							
		15:8	FSRH[7:0]							
0x88	BSR	7:0			BSR[5:0]					
0x89	WREG	7:0	WREG[7:0]							
0x8A	PCLATH	7:0		PCLATH[6:0]						
0x8B	INTCON	7:0	GIE	PEIE						INTEDG
0x8C	ADLTH	7:0	LTHL[7:0]							

Field	Description
n	FSR or INDF number. (0-1)
mm	Prepost increment-decrement mode selection

Table 40-2. Abbreviation Descriptions

Field	Description
PC	Program Counter
$\overline{TO}$	Time-Out bit
C	Carry bit
DC	Digit Carry bit
Z	Zero bit
$\overline{PD}$	Power-Down bit

40.2 Standard Instruction Set

Table 40-3. Instruction Set

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED OPERATIONS									
ADDWF	f, d	Add WREG and f	1	00	0111	dfff	ffff	C, DC, Z	2
ADDWFC	f, d	Add WREG and CARRY bit to f	1	11	1101	dfff	ffff	C, DC, Z	2
ANDWF	f, d	AND WREG with f	1	00	0101	dfff	ffff	Z	2
ASRF	f, d	Arithmetic Right Shift	1	11	0111	dfff	ffff	C, Z	2
LSLF	f, d	Logical Left Shift	1	11	0101	dfff	ffff	C, Z	2
LSRF	f, d	Logical Right Shift	1	11	0110	dfff	ffff	C, Z	2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	–	Clear WREG	1	00	0001	0000	00xx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	2
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	2

RLF	Rotate Left f through Carry			
	(C) → dest<0>			
Status Affected:	C			
Encoding:	0011	01da	ffff	ffff
Description:	The contents of register ‘f’ are rotated one bit to the left through the CARRY flag. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’ (default). 			
Words:	1			
Cycles:	1			

Example:	RLF	REG1, 0
Before Instruction REG1 = 1110 0110 C = 0 After Instruction REG = 1110 0110 W = 1100 1100 C = 1		

RRF	Rotate Right f through Carry
Syntax:	[*label*] RRF f, d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f<n>) → dest<n – 1>, (f<0>) → C, (C) → dest<7>
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the right through the CARRY flag. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is placed back in register ‘f’ (default).