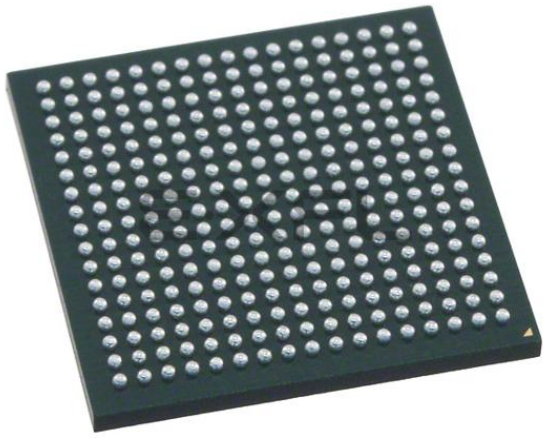

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; C3
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TC)
Security Features	Cryptography
Package / Case	289-LFBGA
Supplier Device Package	289-LFBGA
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spear320-2

List of tables

Main features:

- Supports SPI-compatible Flash and EEPROM devices
- Acts always as a SPI master and up to 2 SPI slave memory devices are supported (with separate chip select signals), with up to 16 MB address space each
- SMI clock signal (SMICLK) is generated by SMI (and input to all slaves) using a clock provided by the AHB bus
- SMICLK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by a programmable 7-bit prescaler allowing up to 127 different clock frequencies.

3.5 External memory interface (EMI)

The EMI Controller provides a simple external memory interface that can be used for example to connect to NOR Flash memory or FPGA devices.

Main features:

- EMI bus master
- 16 and 8-bit transfers
- Can access 4 different peripherals using CS#, one at a time.
- Supports single asynchronous transfers.
- Supports peripherals which use Byte Lane procedure

3.6 SDIO controller/MMC card interface

The SDIO host controller conforms to the SD host Controller Standard Specification Version 2.0. It handles SDIO/SD Protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit and checking for transaction format correctness. The host controller provides programmed I/O and DMA data transfer method.

Main features:

- Meets the following specifications:
  - SD Host Controller Standard Specification Version 2.0
  - SDIO card specification version 2.0
  - SD Memory Card Specification Draft version 2.0
  - SD Memory Card Security Specification version 1.01
  - MMC Specification version 3.31 and 4.2
- Supports both DMA and Non-DMA mode of operation
- Supports MMC Plus and MMC Mobile
- Card Detection (Insertion / Removal)
- Card password protection
- Host clock rate variable between 0 and 48 MHz
- Supports 1 bit, 4 bit and 8 bit SD modes and SPI mode
- Supports Multi Media Card Interrupt mode
- Allows card to interrupt host in 1 bit, 4 bit, 8 bit SD modes and SPI mode.
- Up to 100 Mbits per second data rate using 4 parallel data lines (SD4 bit mode)

- Up to 416 Mbits per second data rate using 8 bit parallel data lines (SD8 bit mode)
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity
- Designed to work with I/O cards, Read-only cards and Read/Write cards
- Error Correction Code (ECC) support for MMC4.2 cards
- Supports Read wait Control, Suspend/Resume operation
- Supports FIFO Overrun and Underrun condition by stopping SD clock

3.7 Flexible static memory controller (FSMC)

SPEAr320 provides a Flexible Static Memory Controller (FSMC) which interfaces to external parallel NAND Flash memories.

Main features:

- 8/16-bit wide data path
- FSMC performs only one access at a time and only one external device is accessed
- Supports little-endian and big-endian memory architectures
- AHB burst transfer handling to reduce access time to external devices
- Supplies an independent configuration for each memory bank
- Programmable timings to support a wide range of devices
  - Programmable wait states (up to 31)
  - Programmable bus turnaround cycles (up to 15)
  - Programmable output enable and write enable delays (up to 15)
- Independent chip select control for each memory bank
- Shares the address bus and the data bus with all the external peripherals
- Only chips selects are unique for each peripheral
- External asynchronous wait control
- Boot memory bank configurable at reset using external control pins

3.8 Multichannel DMA controller

Within its basic subsystem, SPEAr320 provides a DMA controller (DMAC) able to service up to 8 independent DMA channels for serial data transfers between single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).

Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

3.10 CAN controller

SPEAr320 has two CAN controllers for interfacing CAN 2.0 networks.

Main features:

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 16 message objects(136 X 16 message RAM)
- Each message object has its own identifier mask
- Maskable interrupt
- Programmable loop-back mode for self-test operation
- Disabled automatic retransmission mode for time triggered CAN applications

3.11 USB2 Host controller

SPEAr320 has two fully independent USB 2.0 Hosts. Each consists of 5 major blocks:

- EHCI capable of managing high-speed transfers (HS mode, 480 Mbps)
- OHCI that manages the full and the low speed transfers (12 and 1.5 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

Both Hosts can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

One Host controller at time can perform high speed transfer.

3.12 USB2 Device controller

Main features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, configurable as different logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared among all the endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug (UPD) detects the connection of a cable.

3.13 CLCD controller

SPEAr320 has a color liquid crystal display controller (CLCDC) that provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

Main features:

- Resolution programmable up to 1024 x 768
- 16-bpp true-color non-palletized, for color STN and TFT
- 24-bpp true-color non-palletized, for color TFT
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palletized displays for mono STN
- 1, 2, 4 or 8-bpp palletized color displays for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little and big-endian

3.14 GPIOs

A maximum of 102 GPIOs (PL_GPIOs) are available when part of the embedded IPs are not needed (see *Section 4.3: Shared I/O pins (PL_GPIOs)*).

Within its basic subsystem, SPEAr320 provides a base General Purpose Input/Output (GPIO) block (basGPIO). The base GPIO block provides 6 programmable inputs or outputs. Each input/output can be controlled in two distinct modes:

- Software mode, through an APB interface.
- Hardware mode, through a hardware control interface.

Main features of the base GPIO block are:

- Six individually programmable input/output pins (default to input at reset)
- An APB slave acting as control interface in "software mode"
- Programmable interrupt generation capability on any number of pins.
- Hardware control capability of GPIO lines for different system configurations.
- Bit masking in both read and write operation through address lines.

Other GPIO blocks are present in the reconfigurable array subsystem.

3.21 8-channel ADC

Main features:

- Successive approximation conversion method
- 10-bit resolution @1 Msps
- Hardware supporting up to 13.5 bits resolution at 8 ksps by oversampling and accumulation
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- INL ± 1 LSB, DNL ± 1 LSB
- Programmable conversion speed, (min. conversion time is 1 µs)
- Programmable averaging of results from 1 (No averaging) up to 128
- Programmable auto scan for all the eight channels.

3.22 System controller

The System Controller provides an interface for controlling the operation of the overall system.

Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable

3.22.1 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr320 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode**: In this mode the system clocks, HCLK and CLK, are disabled and the System Controller clock SCLK is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.
- **DOZE mode**: In this mode the system clocks, HCLK and CLK, and the System Controller clock SCLK are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode**: During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode**: In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

Two different modes of operation are available :

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

3.25 PWM timers

SPEAr320 provides 4 PWM timers.

Main features:

- Prescaler to define the input clock frequency to each timer
- Programmable duty cycle from 0% to 100%
- Programmable pulse length
- APB slave interface for register programming

3.26 Watchdog timer

The ARM watchdog module consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

3.27 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

Main features:

- Time-of-day clock in 24 hour mode
- Calendar
- Alarm capability
- Isolation mode, allowing RTC to work even if power is not supplied to the rest of the device.

Table 4. Power supply pin description (continued)

Group	Signal name	Ball	Value
ANALOG GROUND	RTC_GND	F2	0 V
	DITH_PLL_VSS_ANA	G1	
	USB_HOST1_VSSA	J2	
	USB_HOST0_VSSA	L1	
	USB_COMMON_VSSAC	L3	
	USB_DEVICE_VSSA	N2	
	DITH_VSS2V5	N4	
	MCLK_GND	P3	
	MCLK_GNDSUB	R3	
	ADC_AGND	N12	
I/O	DIGITAL_VDDE3V3	F5 F6 F7 F10 F11 F12 G5 J12 K12 L12 M12	3.3 V
CORE	VDD	F8 F9 G12 H5 H12 J5 L11 M6 M7 M11	1.2 V
USB HOST0 PHY	USB_HOST0_VDD2V5	L2	2.5 V
	USB_HOST0_VDD3V3	K4	3.3 V
USB HOST1 PHY	USB_HOST1_VDD2V5	K3	2.5 V
	USB_HOST1_VDD3V3	J1	3.3 V
USB DEVICE PHY	USB_DEVICE_VDD2V5	N1	2.5 V
	USB_DEVICE_VDD3V3	N3	3.3 V
	USB_HOST1_HOST0_DEVICE_DVDD1V2	M3	1.2 V
OSCI (master clock)	MCLK_VDD	R1	1.2 V
	MCLK_VDD2V5	R2	2.5 V
PLL1	DITH_PLL_VDD_ANA	G2	2.5 V
PLL2	DITH_VDD_2V5	M4	2.5 V
DDR I/O	DDR_VDDE1V8	M5 N5 N6 N7 N8 N9 N10 N11	1.8 V
ADC	ADC_AVDD	N13	2.5 V
OSCI RTC	RTC_VDD1V5	F1	1.5 V

Note: All the VDD 2V5 power supplies are analog VDD.

Table 7. USB pin description (continued)

Group	Signal name	Ball	Direction	Function	Pin type
USB Host	USB_HOST1_DP	H1	I/O	USB HOST1 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST1_DM	H2		USB HOST1 D-	
	USB_HOST1_VBUS	H3	Out	USBHOST1 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST1_OVERCUR	J4	In	USB Host1 Over-Current	TTL input buffer 3.3 V tolerant, PD
	USB_HOST0_DP	K1	I/O	USB HOST0 D+	Bidirectional analog buffer 5 V tolerant
	USB_HOST0_DM	K2		USB HOST0 D-	
	USB_HOST0_VBUS	J3	Out	USB HOST0 VBUS	TTL output buffer 3.3 V capable, 4 mA
	USB_HOST0_OVERCUR	H4	In	USB Host0 Over-current	TTL Input Buffer 3.3 V tolerant, PD
USB	USB_TXRTUNE	K5	Out	Reference resistor	Analog
	USB_ANALOG_TEST	L4	Out	Analog Test Output	Analog

Table 8. ADC pin description

Signal name	Ball	Direction	Function	Pin type
AIN_0	N16	In	ADC analog input channel	Analog buffer 2.5 V tolerant
AIN_1	N15			
AIN_2	P17			
AIN_3	P16			
AIN_4	P15			
AIN_5	R17			
AIN_6	R16			
AIN_7	R15			
ADC_VREFN	N14		ADC negative voltage reference	
ADC_VREFP	P14		ADC positive voltage reference	

4.3 Shared I/O pins (PL_GPIOs)

The 98 PL_GPIO and 4 PL_CLK pins have the following characteristics:

- Output buffer: TTL 3.3 V capable up to 10 mA
- Input buffer: TTL, 3.3 V tolerant, selectable internal pull up/pull down (PU/PD)

The PL_GPIOs can be configured in different modes. This allows SPEAr320 to be tailored for use in various applications like:

- Metering concentrators
- Large power supply controllers
- Small printers

4.3.1 PL_GPIO pin description

Table 10. PL_GPIO pin description

Group	Signal name	Ball	Direction	Function	Pin type
PL_GPIOs	PL_GPIO_97... PL_GPIO_0	(see the *Table 11*)	I/O	General purpose I/O or multiplexed pins (see *Table 11*)	(see the introduction of the *Section 4.3* here above)
	PL_CLK1... PL_CLK4			programmable logic external clocks	

4.3.2 Configuration modes

This section describes the main operating modes created by using a selection of the embedded IPs.

The following modes can be selected by programming some control registers present in the reconfigurable array subsystem.

- Mode 1: SMII automation networking mode
- Mode 2: MII automation networking mode
- Mode 3: Expanded automation mode
- Mode 4: Printer mode

Table 11: PL_GPIO multiplexing scheme shows all the I/O functions available in each mode.

Mode 1 is the default mode for SPEAr320.

Printer mode

The “printer” operating mode mainly provides:

- NAND Flash interface (8 bits, 4 chip selects)
- Up to 4 PWM outputs
- 2 SMII interfaces
- 3 UARTs
  - 1 with hardware flow control (up to 3 Mbps)
  - 1 with hardware flow control (baud rate up to 7 Mbps)
  - 1 with software flow control (baud rate up to 7 Mbps)
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- Standard Parallel Port (SPP device implementation)
- 2 independent SSP Synchronous Serial Ports (SPI, Microwire or TI protocol)
- GPIOs with interrupt capabilities
-

4.3.3 Alternate functions

Other peripheral functions are listed in the Alternate Functions column of *Table 11: PL_GPIO multiplexing scheme* and can be individually enabled/disabled configuring the bits of a dedicated control register.

4.3.4 Boot pins

The status of the boot pins is read at startup by the BootROM.

4.3.5 GPIOs

The PL_GPIO pins can be used as software controlled general purpose I/Os (GPIOs) if they are not used by the I/O functions of the SPEAr320 IPs.

To configure any PL_GPIO pin as GPIO, set the corresponding bit in the GPIO_Select(0 ..3) registers that are 102 bits write registers that select GPIO versus some IPs.

4.3.6 Multiplexing scheme

To provide the best I/O multiplexing flexibility and the higher number of GPIOs for ARM controlled input-output function, the following hierarchical multiplexing scheme has been implemented.

Figure 3. Hierarchical multiplexing scheme

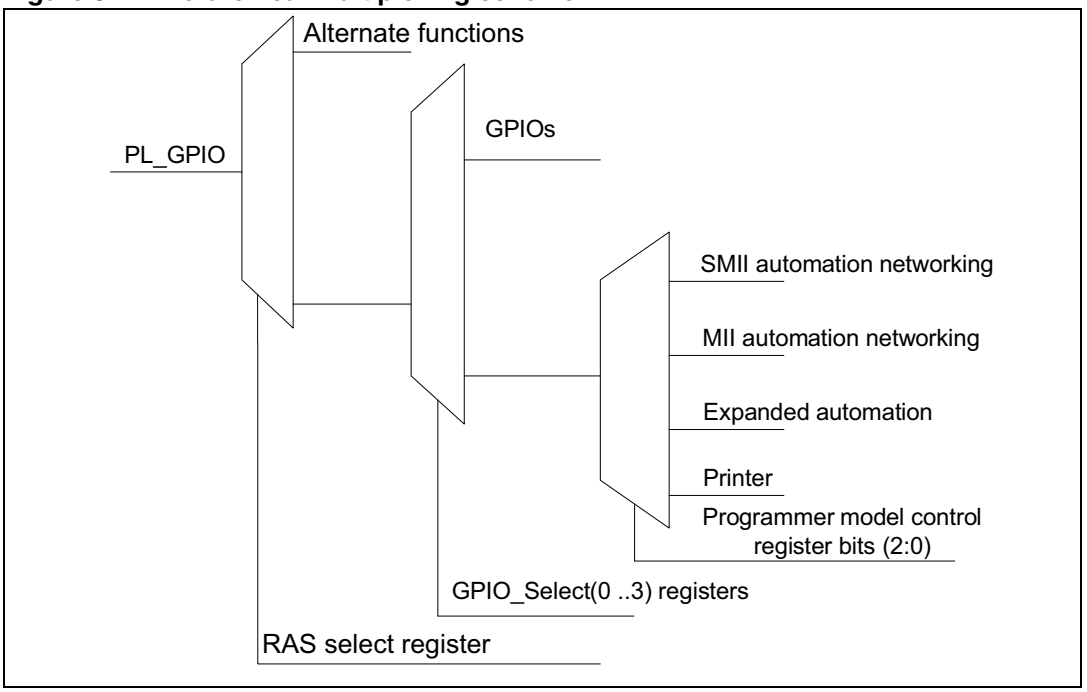


Table 11. PL_GPIO multiplexing scheme

PL_GPIO_# / ball number	Configuration mode (enabled by Programmer model control register bits (2:0))				Alternate function (enabled by RAS select register)	Boot pins	Function in GPIO alternative mode
	1	2	3	4			
PL_GPIO_97/H16	CLD0	MII1_TXCLK	EMI_A0	0			GPIO_97
PL_GPIO_96/H15	CLD1	MII1_TXD0	EMI_A1	0			GPIO_96
PL_GPIO_95/H14	CLD2	MII1_TXD1	EMI_A2	0			GPIO_95
PL_GPIO_94/H13	CLD3	MII1_TXD2	EMI_A3	0			GPIO_94
PL_GPIO_93/G17	CLD4	MII1_TXD3	EMI_A4	0			GPIO_93
PL_GPIO_92/G16	CLD5	MII1_TXEN	EMI_A5	0			GPIO_92
PL_GPIO_91/G15	CLD6	MII1_TXER	EMI_A6	0			GPIO_91
PL_GPIO_90/G14	CLD7	MII1_RXCLK	EMI_A7	0			GPIO_90
PL_GPIO_89/F17	CLD8	MII1_RXDV	EMI_A8	0			GPIO_89
PL_GPIO_88/F16	CLD9	MII1_RXER	EMI_A9	0			GPIO_88
PL_GPIO_87/G13	CLD10	MII1_RXD0	EMI_A10	0			GPIO_87

6.5 3.3V I/O characteristics

The 3.3 V I/Os are compliant with JEDEC standard JESD8b.

Table 20. Low voltage TTL DC input specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Low level input voltage		0.8	V
V_{IH}	High level input voltage	2		V
V_{hyst}	Schmitt trigger hysteresis	300	800	mV

Table 21. Low voltage TTL DC output specification (3 V< V_{DD} <3.6 V)

Symbol	Parameter	Test condition	Min	Max	Unit
V_{OL}	Low level output voltage	I_{OL}= X mA (1)		0.3	V
V_{OH}	High level output voltage	I_{OH}= -X mA (1)	V_{DD} - 0.3		V

1. Maximum current load (IOL) = 10 mA for PL_GPIO and PL_CLK pins. For the IOL max value of dedicated pins, refer to *Chapter 4: Pin description*.

Table 22. Pull-up and pull-down characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_I = 0 V	29	67	kΩ
R_{PD}	Equivalent pull-down resistance	V_I = V_{DDE}3V3	29	103	kΩ

6.6 LPDDR and DDR2 pin characteristics

Table 23. DC characteristics

Symbol	Parameter	Test condition	Min	Max	Unit
V_{IL}	Low level input voltage	SSTL18	-0.3	V_{REF}-0.125	V
V_{IH}	High level input voltage	SSTL18	V_{REF}+0.125	V_{DDE}1V8+0.3	V
V_{hyst}	Input voltage hysteresis		200		mV

Table 24. Driver characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_O	Output impedance		45		Ω

7.4 CLCD timing characteristics

The characterization timing is done considering an output load of 10 pF on all the outputs.

The CLCD has a wide variety of configurations and setting and the parameters change accordingly. *Figure 9* and *Table 32* specify the clock to output delay.

Figure 9. CLCD waveform

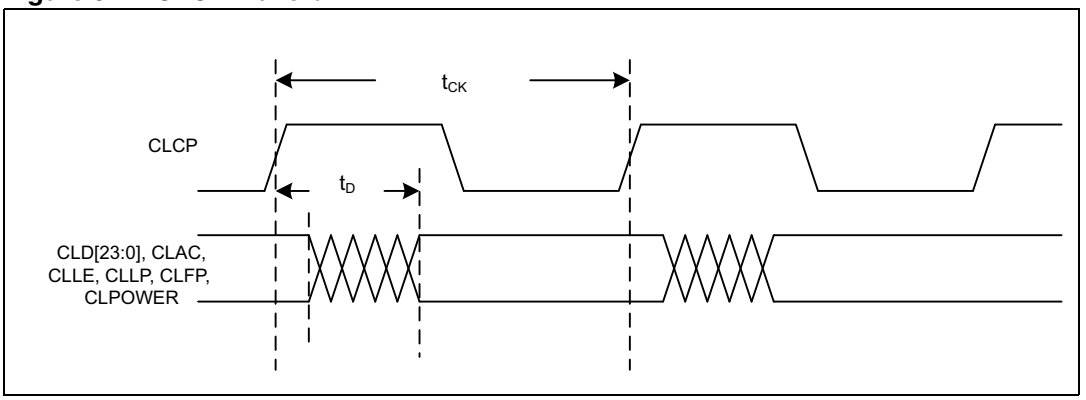


Table 32. CLCD timings

Symbol	Description	Min	Max	Unit
t_{CK}	CLCP clock period	20.83	41.66	ns
t_D	CLCP to CLCD output data delay	0.97	3.74	ns

7.9 MII Ethernet MAC 10/100 Mbps timing characteristics

The characterization timing is given for an output load of 5 pF on the MII TX clock and 10 pF on the other pads.

7.9.1 MII transmit timing specifications

Figure 19. MII TX waveforms

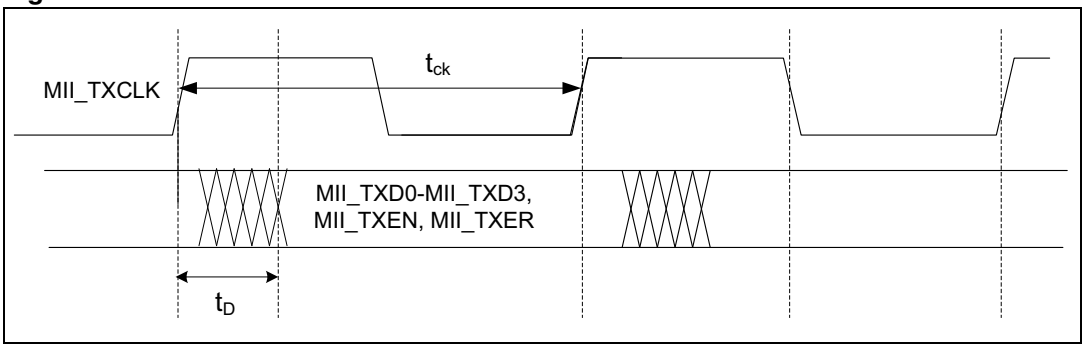


Table 40. MII TX timings

Symbol	Description	Min	Max	Unit
t_{CK}	MII_TXCLK clock period	40	40	ns
t_D	MII_TXCLK to MII output data delay	-1	8.9	

Note: To calculate the t_{SETUP} value for the PHY you have to consider the next t_{CLK} rising edge, so you have to apply the following formula: $t_{SETUP} = t_{CLK} - t_{max}$

7.9.2 MII receive timing specifications

Figure 20. MII RX waveforms

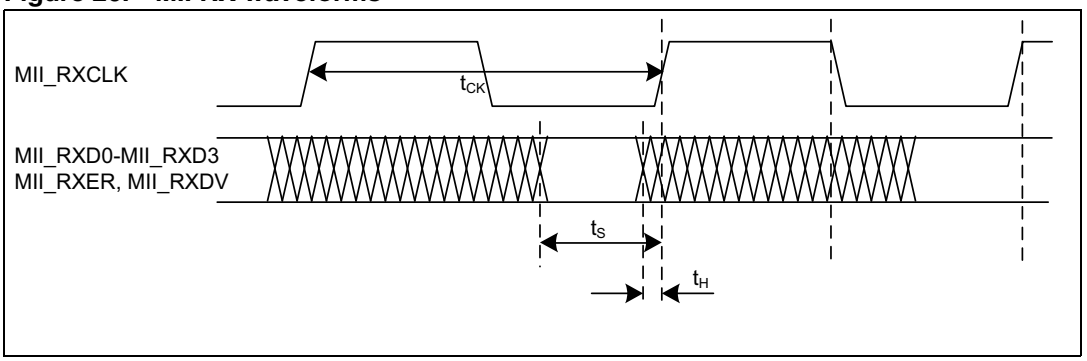


Table 41. MII RX timings

Symbol	Description	Min	Max	Unit
t_{CK}	MII_TXCLK clock period	40	40	ns
t_S	Setup time requirement for MII receive data	1.6		
t_H	Hold time requirement for MII receive data	0.7		

7.12 SSP timing characteristics

This module provides a programmable length shift register which allows serial communication with other SSP devices through a 3 or 4 wire interface (SSP_CLK, SSP_MISO, SSP_MOSI and SSP_CSn). The SSP supports the following features:

- Master/Slave mode operations
- Chip-selects for interfacing to multiple slave SPI devices.
- 3 or 4 wire interface (SSP_SCK, SSP_MISO, SSP_MOSI and SSP_CSn)
- Single interrupt
- Separate DMA events for SPI Receive and Transmit
- 16-bit shift register
- Receive buffer register
- Programmable character length (2 to 16 bits)
- Programmable SSP clock frequency range
- 8-bit clock pre-scaler
- Programmable clock phase (delay or no delay)
- Programmable clock polarity

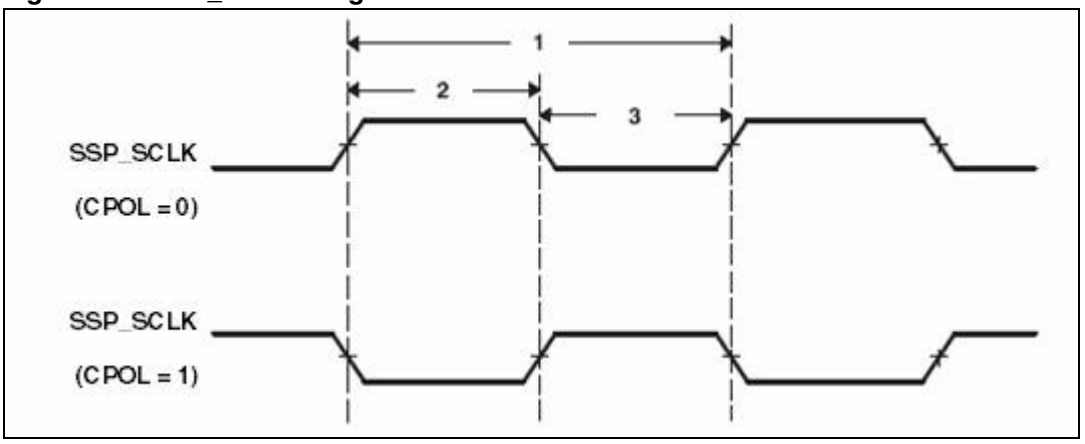
Note: The following tables and figures show the characterization of the SSP using the SPI protocol.

Table 45. Timing requirements for SSP (all modes)

No.	parameters		Min	Max	Unit
1	$T_{c(CLK)}$	Cycle time, SSP_CLK	24	–	ns
2	$T_{w(CLKH)}$	Pulse duration, SSP_CLK high	0.49*To	0.51*To	ns
3	$T_{w(CLKL)}$	Pulse duration, SSP_CLK low	0.49*To	0.51*To	ns

T = Tc(CLK) = SSP_CLK period is equal to the SSP module master clock divided by a configurable divider.

Figure 24. SSP_CLK timings



7.12.1 SPI master mode timings (clock phase = 0)

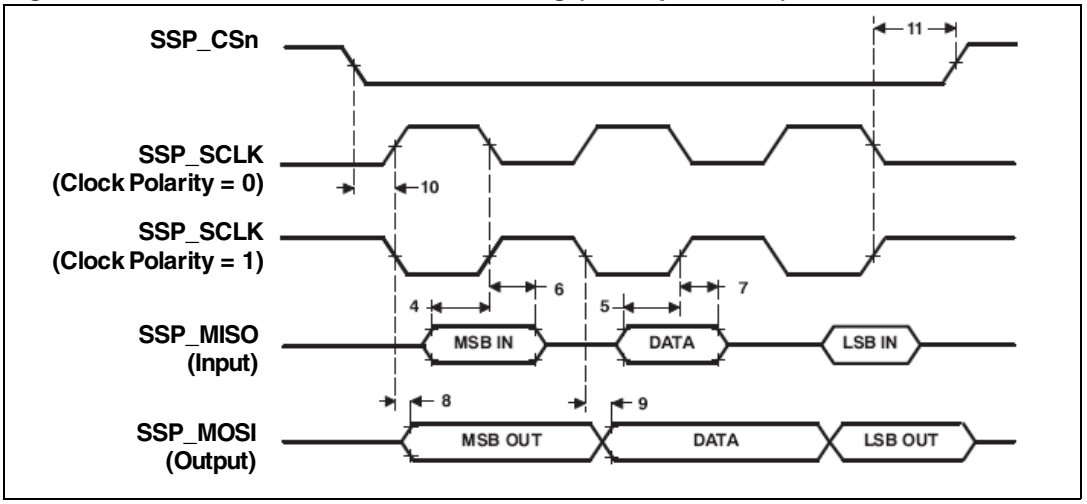
Table 46. Timing requirements for SPI master mode (clock phase = 0)

No.	Parameters			Min	Max	Unit
4	$t_{su(DIV-CLKL)}$	Setup time, MISO (input) valid before SSP_CLK (output) falling edge	Clock polarity = 0	-0.4	-0.3	ns
5	$t_{su(DIV-CLKH)}$	Setup time, MISO (input) valid before SSP_CLK (output) rising edge	Clock polarity = 1	-0.4	-0.3	ns
6	$t_{h(CLKL-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) falling edge	Clock polarity = 0	0.9	1.7	ns
7	$t_{h(CLKH-DIV)}$	Hold time, MISO (input) valid after SSP_CLK (output) rising edge	Clock polarity = 1	0.9	1.7	ns

Table 47. Switching characteristics over recommended operating conditions for SPI master mode (clock phase =0)

No.	Parameters			Min	Max	Unit
8	$t_{d(CLKH-DOV)}$	Delay time, SSP_CLK (output) rising edge to MOSI (output) transition	Clock Polarity = 0	-3.1	2.2	ns
9	$t_{d(CLKL-DOV)}$	Delay time, SSP_CLK (output) falling edge to MOSI (output) transition	Clock Polarity = 1	-3.1	2.2	ns
10	$t_{d(ENL-CLKH/L)}$	Delay time, SSP_CSn (output) falling edge to first SSP_CLK (output) rising or falling edge		T		ns
11	$td_{(CLKH/L-ENH)}$	Delay time, SSP_CLK (output) rising or falling edge to SSP_CSn (output) rising edge		T/2		ns

Figure 25. SPI master mode external timing (clock phase = 0)



7.13 UART timing characteristics

Figure 27. UART transmit and receive timings

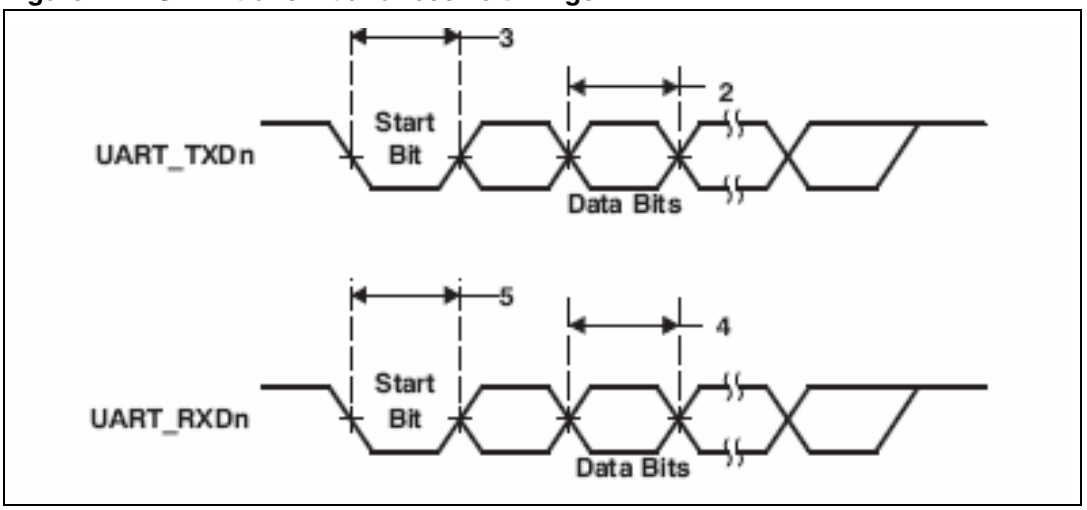


Table 50. UART transmit timing characteristics

S.No.	Parameters	Min	Max	Unit
1	UART0 Maximum Baud Rate		3	Mbps
	UART1/UART2 Maximum Baud Rate		7	
2	UART Pulse Duration Transmit Data (TxD)	$0.99B_{(1)}$	$B_{(1)}$	ns
3	UART Transmit Start Bit	$0.99B_{(1)}$	$B_{(1)}$	ns

Table 51. UART receive timing characteristics

S.No.	Parameters	Min	Max	Units
4	UART Pulse Duration Receive Data (RxD)	$0.97B_{(1)}$	$1.06B_{(1)}$	ns
5	UART Receive Start Bit	$0.97B_{(1)}$	$1.06B_{(1)}$	ns

where (1) B = UART baud rate

Figure 28. LFBGA289 package dimensions

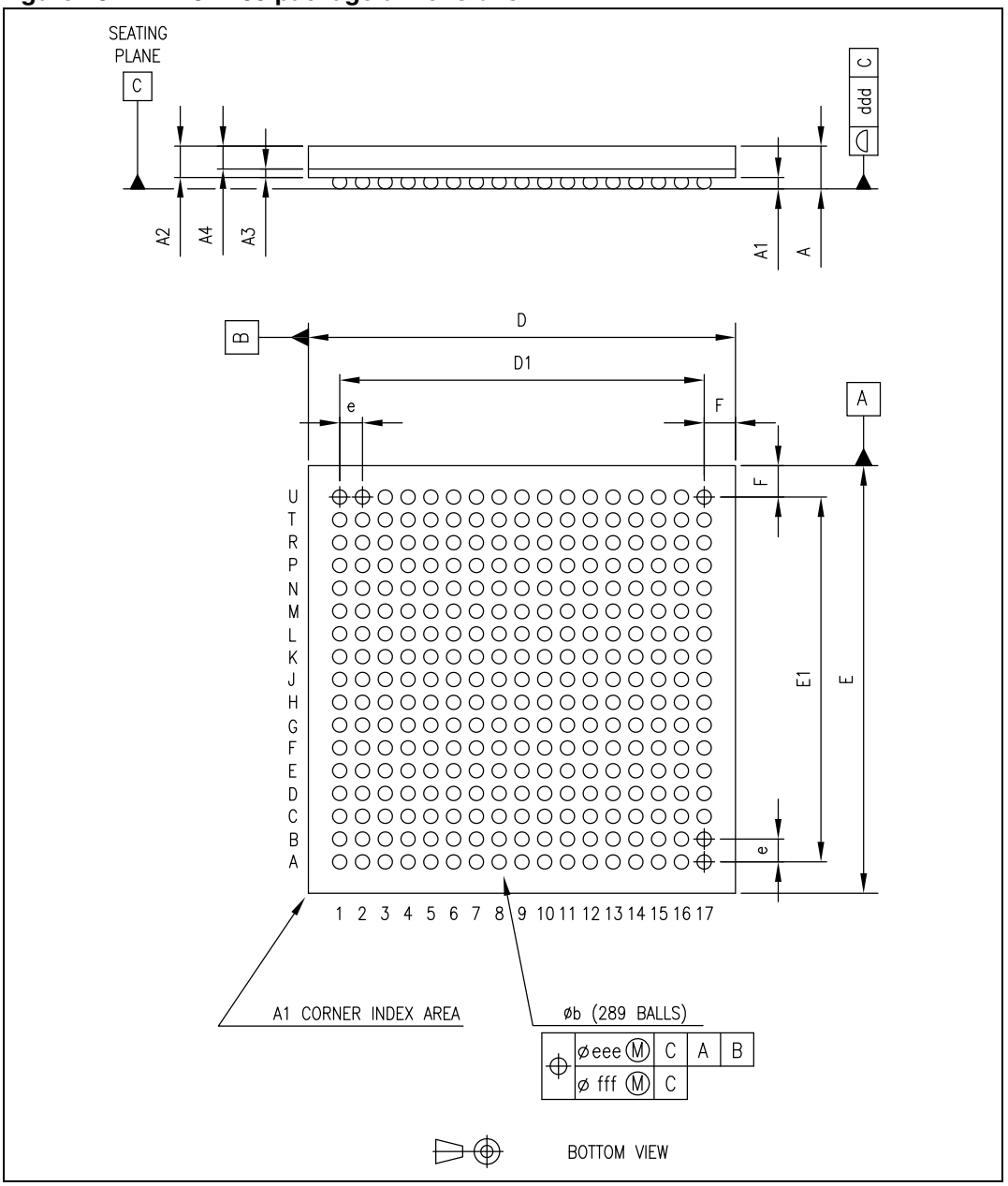


Table 54. Thermal resistance characteristics

package	Θ_{JC} (°C/W)	Θ_{JB} (°C/W)	Θ_{JA}(°C/W)(1)
LFBGA289	18.5	24.5	33

1. Measured on JESD51 2s2p test board.

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