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Embedded - FPGAs (Field Programmable Gate Array) with Microcontrollers: Enhancing Flexibility and Performance

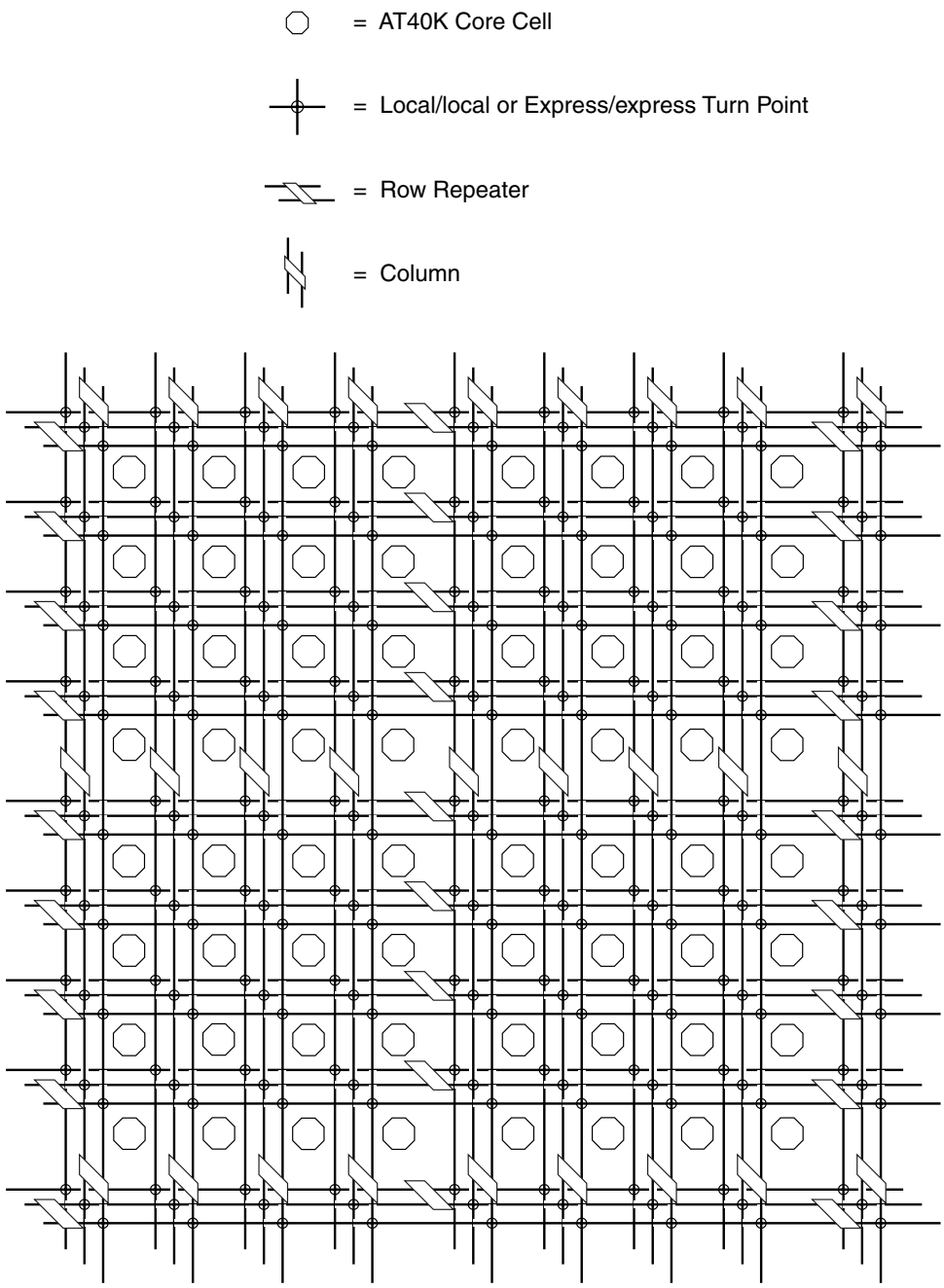
Embedded - FPGAs (Field Programmable Gate Arrays) with Microcontrollers represent a cutting-edge category of electronic components that combine the flexibility of FPGA technology with the processing power of integrated microcontrollers. This hybrid approach offers a versatile solution for designing and implementing complex digital systems that require both programmable logic and embedded processing capabilities.

What Are Embedded - FPGAs with Microcontrollers?

At their core, **FPGAs** are semiconductor devices that can

Details	
Product Status	Obsolete
Core Type	8-Bit AVR
Speed	25 MHz
Interface	I²C, UART
Program SRAM Bytes	4K-16K
FPGA SRAM	2kb
EEPROM Size	-
Data SRAM Bytes	4K ~ 16K
FPGA Core Cells	256
FPGA Gates	5K
FPGA Registers	436
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at94k05al-25aji

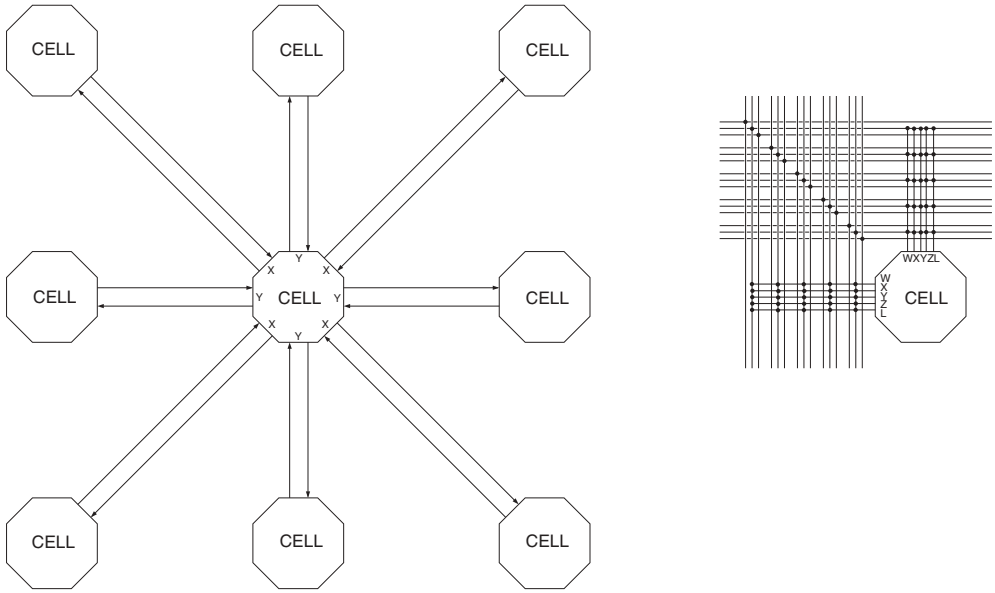
Figure 4. Busing Plane (One of Five)



Cell Connections

Figure 5(a) depicts direct connections between an FPGA cell and its eight nearest neighbors. Figure 5(b) shows the connections between a cell five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane).

Figure 5. Cell Connections



(a) Cell-to-Cell Connections

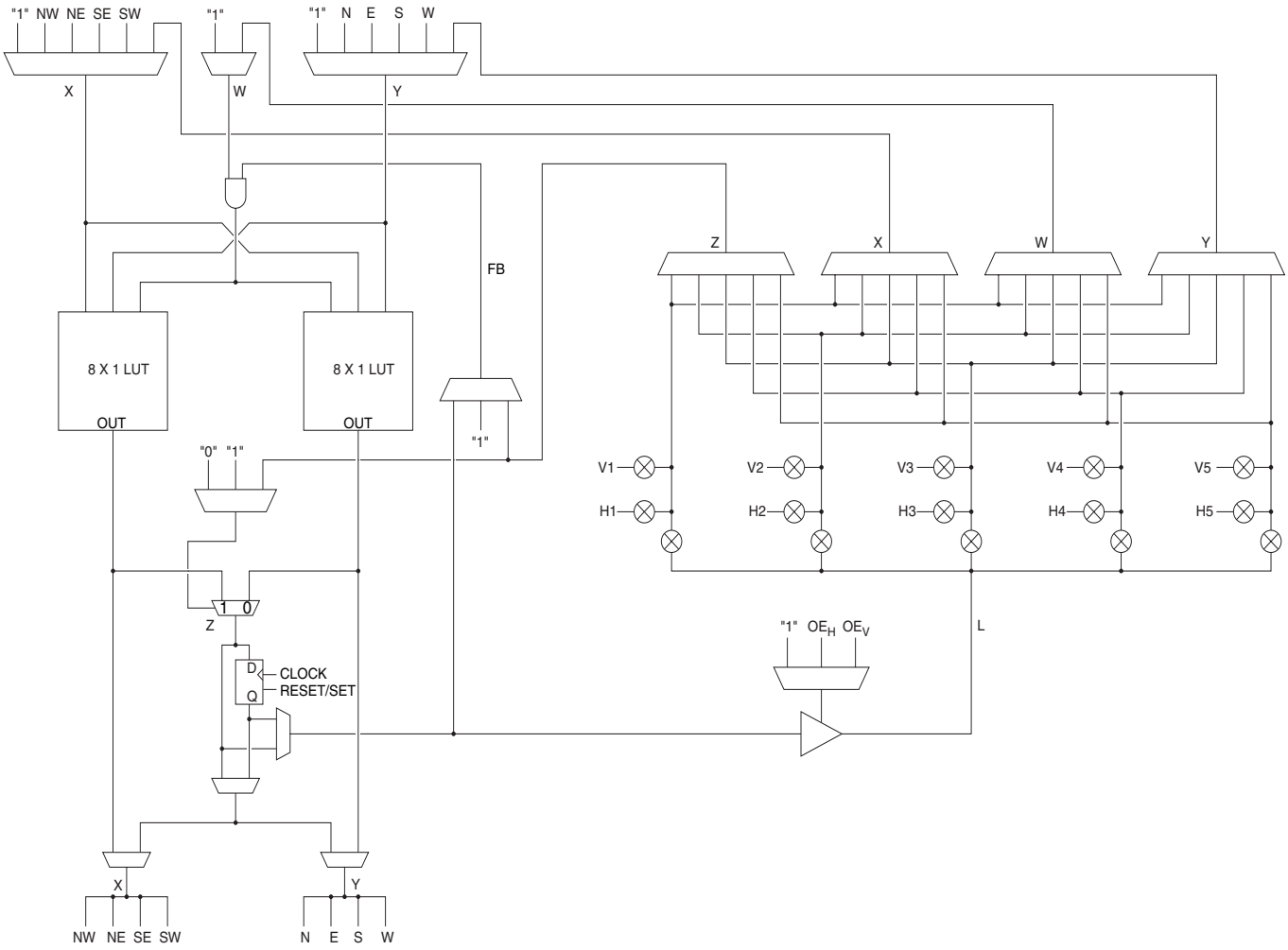
(b) Cell-to-Bus Connections

The Cell

Figure 6 depicts the AT40K FPGA embedded core logic cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. Vn is connected to the vertical local bus in plane n. Hn is connected to the horizontal local bus in plane n. A local/local turn in plane n is achieved by turning on the two pass gates connected to Vn and Hn. Up to five simultaneous local/local turns are possible.

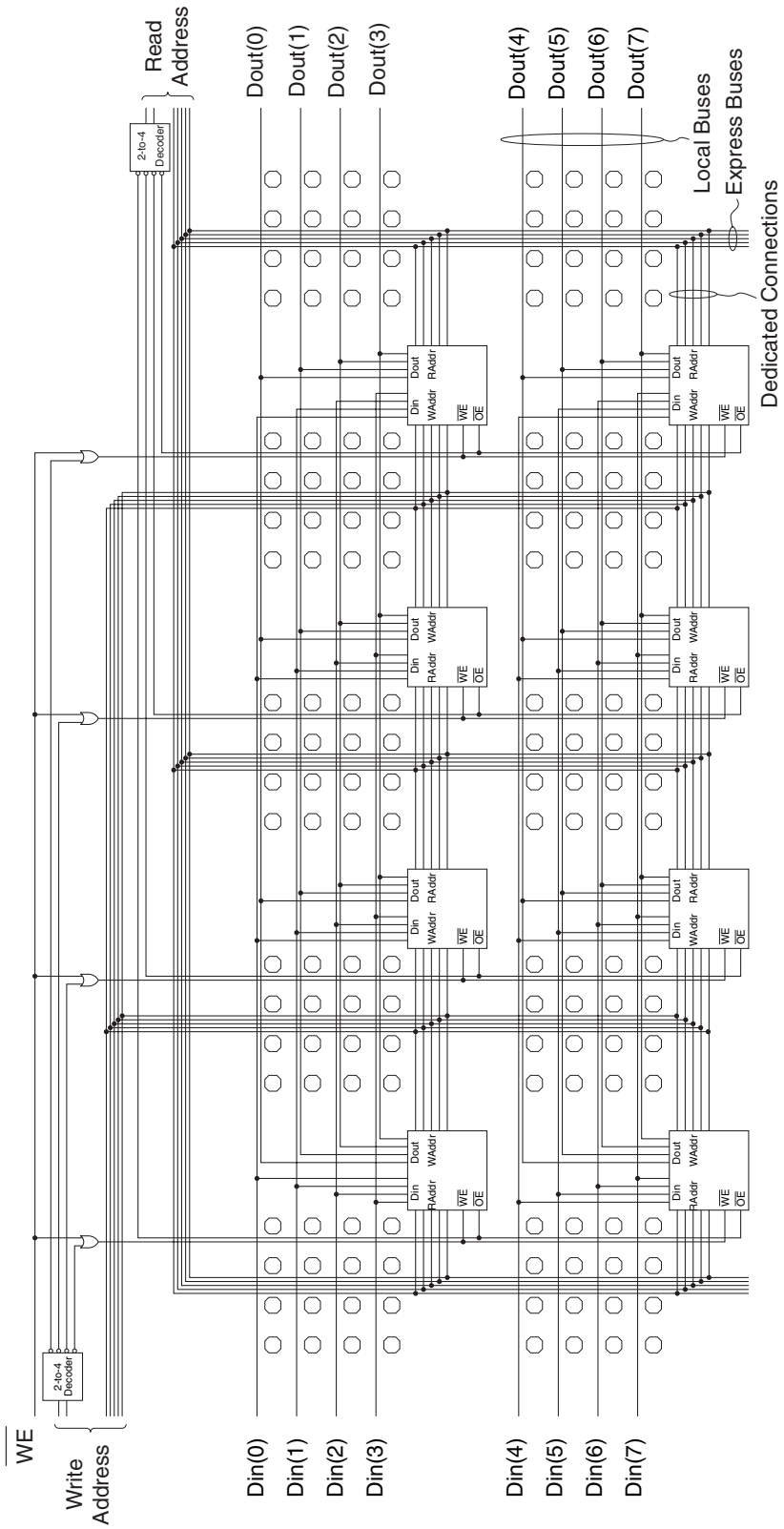
The logic cell can be configured in several “modes”. The logic cell flexibility makes the FPGA architecture well suited to all digital design application areas, see Figure 7. The IDS layout tool automatically optimizes designs to utilize the cell flexibility.

Figure 6. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Figure 10. FreeRAM Example: 128 x 8 Dual-ported RAM (Asynchronous)[1]



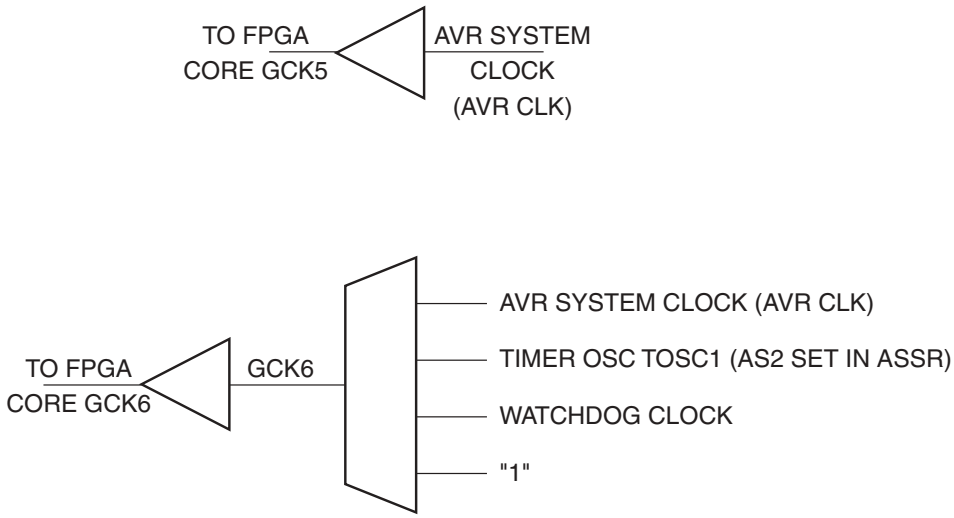
Note: 1. These layouts can be generated automatically using the Macro Generators.

Clocking and Set/Reset

Six of the eight dedicated Global Clock buses (1, 2, 3, 4, 7 and 8) are connected to a dual-use Global Clock pin. In addition, two Global Clock buses (5 and 6) are driven from clock signals generated within the AVR microcontroller core, see Figure 11.

An FPGA core internal signal can be placed on any Global Clock bus by routing that signal to a Global Clock access point in the corners of the embedded core. Each column of the array has a Column Clock selected from one of the eight Global Clock buses. The left edge Column Clock mux has two additional inputs from dual-use pins FCK1, see Figure 8, and FCK2 to provide fast clocking to left-side I/O. Each sector column of four cells can be clocked from a (Plane 4) express bus or from the Column Clock. Clocking to the 4 cells of a sector can be disabled. The Plane 4 express bus used for clocking is half length at the array edge. The clock provided to each sector column of four cells can be either inverted or not inverted. The register in each cell is triggered on a rising clock edge. On power-up, constant “0” is provided to each register’s clock pins. A dedicated Global Set/Reset bus, see Figure 9, can be driven by any USER I/O pad, except those used for clocking, Global or Fast. An internal signal can be placed on the Global Set/Reset bus by routing that signal to the pad programmed as the Global Set/Reset input. Global Set/Reset is distributed to each column of the array. Each sector column of four cells can be Set/Reset by a (Plane 5) express bus or by the Global Set/Reset. The Plane 5 express bus used for Set/Reset is half length at array edge. The Set/Reset provided to each sector column of four cells can be either inverted or not inverted. The function of the Set/Reset input of a register (either Set or Reset) is determined by a configuration bit for each cell. The Set/Reset input of a register is Active Low (logic 0). Setting or resetting of a register is asynchronous. On power-up, a logic 1 (High) is provided by each register, i.e., all registers are set at power-up.

Figure 11. FPGA Clocks from AVR



Data Indirect

Operand address is the contents of the X-, Y- or the Z-register.

Data Indirect with Pre-decrement

The X-, Y- or the Z-register is decremented before the operation. Operand address is the decremented contents of the X, Y or the Z-register.

Data Indirect with Post-increment

The X-, Y- or the Z-register is incremented after the operation. The operand address is the content of the X-, Y- or the Z-register prior to incrementing.

Direct Program Address, JMP and CALL

Program execution continues at the address immediate in the instruction words.

Indirect Program Addressing, IJMP and ICALL

Program execution continues at address contained by the Z-register (i.e., the PC is loaded with the contents of the Z-register).

Relative Program Addressing, RJMP and RCALL

Program execution continues at address PC + k + 1. The relative address k is -2048 to 2047.

Memory Access Times and Instruction Execution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The AVR CPU is driven by the XTAL1 input directly generated from the external clock crystal for the chip. No internal clock division is used.

Figure 29 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access register file concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks and functions per power-unit.

Figure 29. The Parallel Instruction Fetches and Instruction Executions

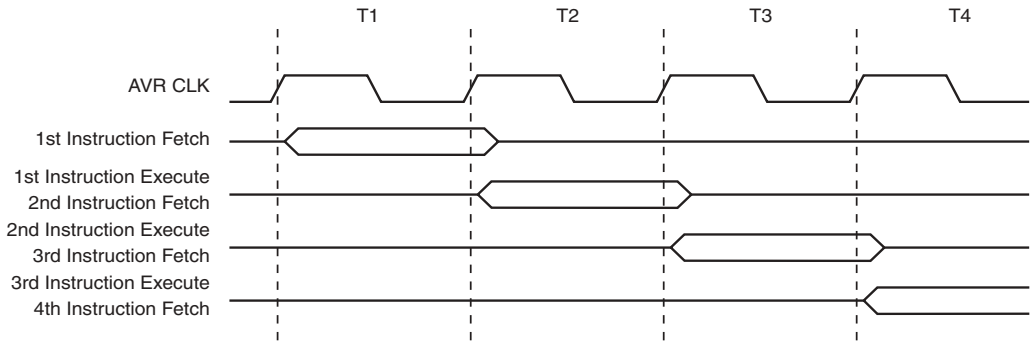
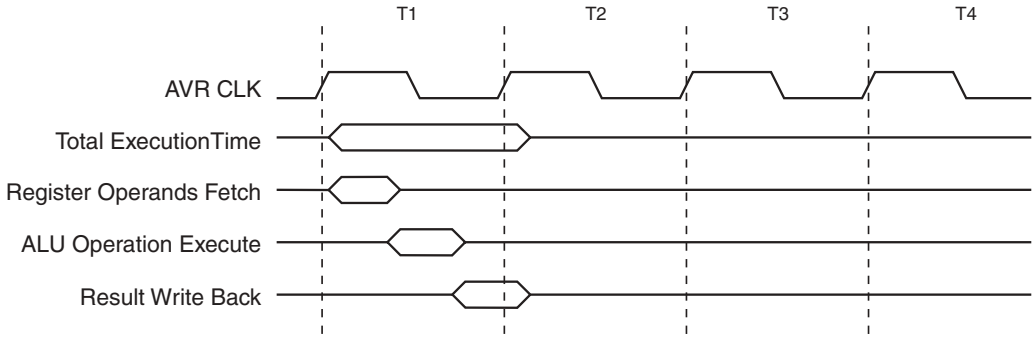


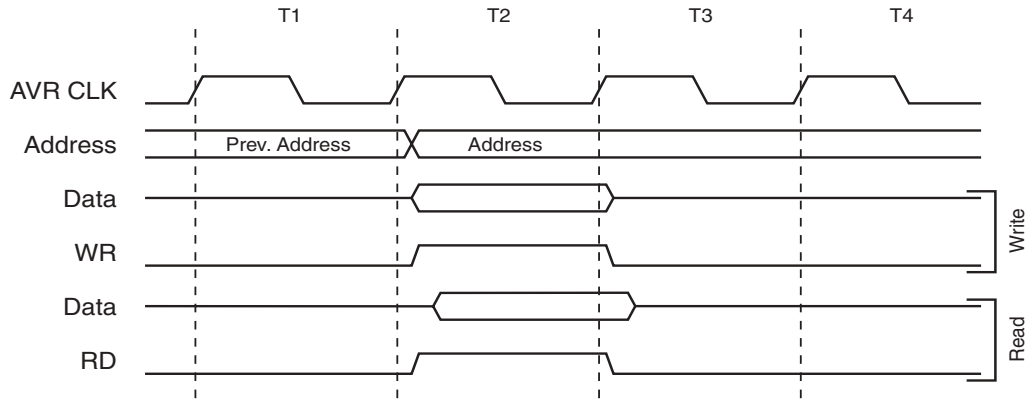
Figure 30 shows the internal timing concept for the register file. In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

Figure 30. Single Cycle ALU Operation



The internal data SRAM access is performed in two system clock cycles as described in Figure 31.

Figure 31. On-chip Data SRAM Access Cycles



Assuming Run-Test/Idle is the present state, a typical scenario for using the JTAG interface is

- At the TMS input, apply the sequence 1, 1, 0, 0 at the rising edges of TCK to enter the Shift Instruction Register - Shift-IR state. While TMS is Low, shift the 4 bit JTAG instructions into the JTAG instruction register from the TDI input at the rising edge of TCK, while the captured IR-state 0x01 is shifts out on the TDO pin. The JTAG Instruction selects a particular Data Register as path between TDI and TDO and controls the circuitry surrounding the selected Data Register.
- Apply the TMS sequence 1, 1, 0 to re-enter the Run-Test/Idle state. The instruction is latched onto the parallel output from the shift register path in the Update-IR state. The Exit-IR, Pause-IR, and Exit2-IR states are only used for navigating the state machine.
- At the TMS input, apply the sequence 1, 0, 0 at the rising edges of TCK to enter the Shift Data Register - Shift-DR state. While TMS is Low, upload the selected Data Register (selected by the present JTAG instruction in the JTAG Instruction Register) from the TDI input at the rising edge of TCK. At the same time, the parallel inputs to the Data Register captured in the Capture-DR state shifts out on the TDO pin.
- Apply the TMS sequence 1, 1, 0 to re-enter the Run-Test/Idle state. If the selected Data Register has a latched parallel-output, the latching takes place in the Update-DR state. The Exit-DR, Pause-DR, and Exit2-DR states are only used for navigating the state machine.

As shown in Figure 40 on page 70, the Run-Test/Idle[1] state need not be entered between selecting JTAG instruction and using Data Registers, and some JTAG instructions may select certain functions to be performed in the Run-Test/Idle, making it unsuitable as an Idle state.

Note: 1. Independent of the initial state of the TAP Controller, the Test-Logic-Reset state can always be entered by holding TMS High for 5 TCK clock periods.

Using the Boundary-scan Chain

A complete description of the Boundary-Scan capabilities are given in the section “IEEE 1149.1 (JTAG) Boundary-scan” on page 73.

Using the On-chip Debug System

As shown in Figure 39, the hardware support for On-Chip Debugging consists mainly of

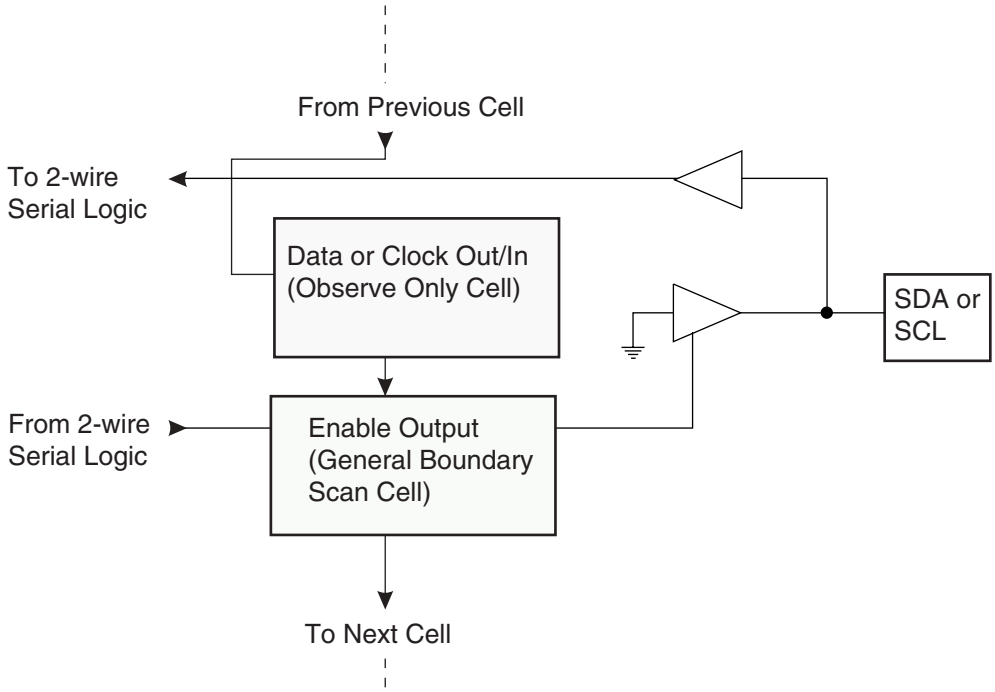
- A scan chain on the interface between the internal AVR CPU and the internal peripheral units
- A breakpoint unit
- A communication interface between the CPU and JTAG system
- A scan chain on the interface between the internal AVR CPU and the FPGA
- A scan chain on the interface between the internal Program/Data SRAM and the FPGA

All read or modify/write operations needed for implementing the Debugger are done by applying AVR instructions via the internal AVR CPU Scan Chain. The CPU sends the result to an I/O memory mapped location which is part of the communication interface between the CPU and the JTAG system.

Scanning 2-wire Serial

The SCL and SDA pins are open drain, bi-directional and enabled separately. The “Enable Output” bits (active High) in the scan chain are supported by general boundary-scan cells. Enabling the output will drive the pin Low from a tri-state. External pull-ups on the 2-wire bus are required to pull the pins High if the output is disabled. The “Data Out/In” and “Clock Out/In” bits in the scan chain are observe-only cells. Figure 46 shows how each pin is connected in the scan chain.

Figure 46. Boundary-scan Cells for 2-wire Serial



Scanning the Clock Pins

Figure 47 shows how each oscillator with external connection is supported in the scan chain. The Enable signal is supported with a general boundary-scan cell, while the oscillator/clock output is attached to an observe-only cell. In addition to the main clock, the timer oscillator is scanned in the same way. The output from the internal RC-Oscillator is not scanned, as this oscillator does not have external connections.

Figure 47. Boundary-scan Cells for Oscillators and Clock Options

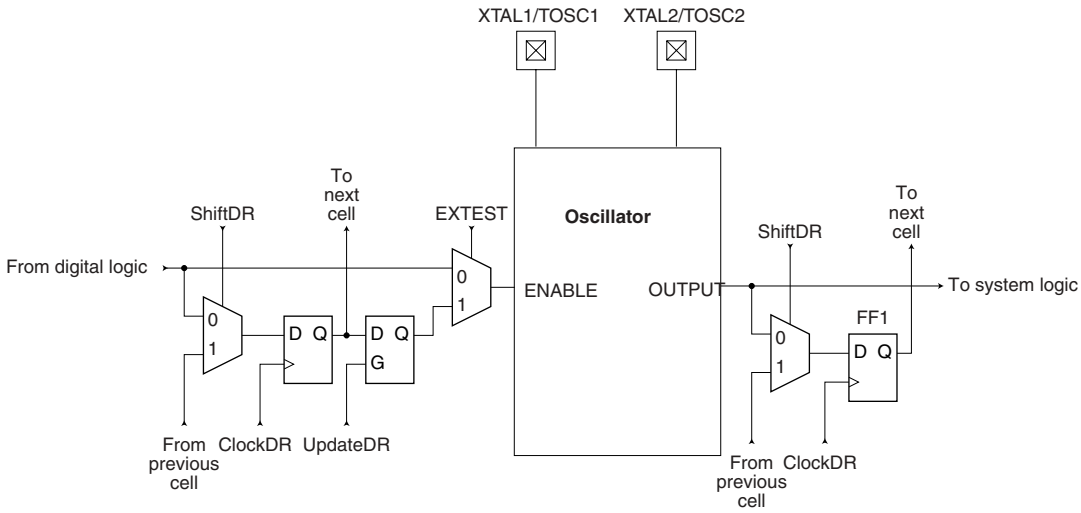
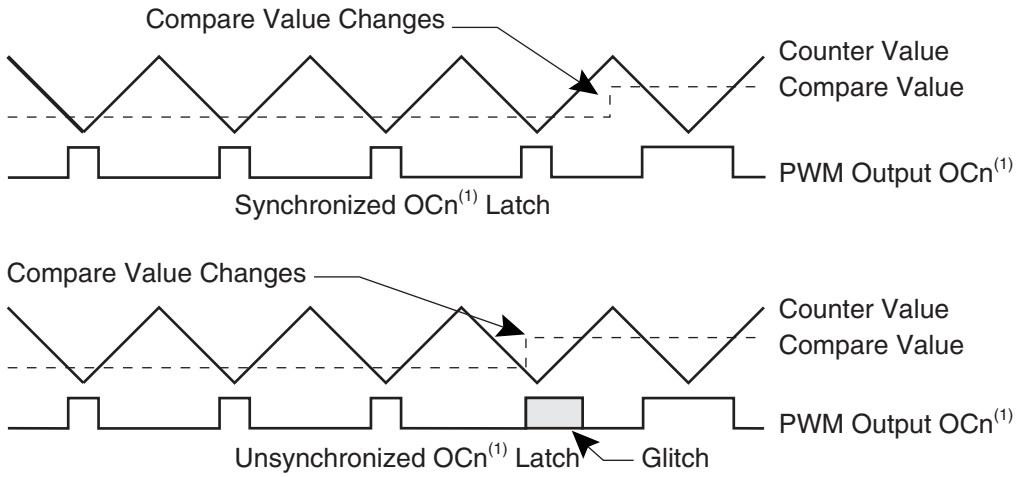
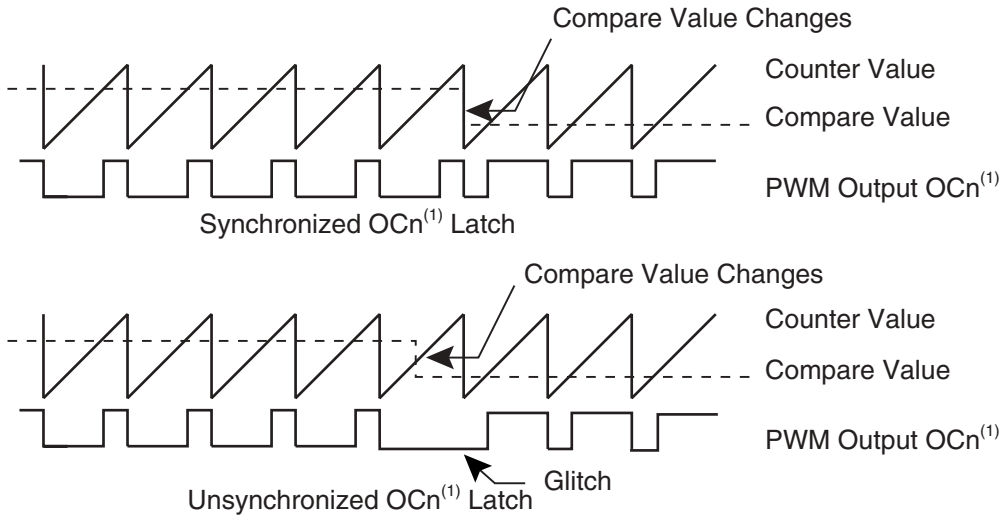


Figure 52. Effects of Unsynchronized OCR Latching in Up/Down Mode



Note: 1. n = 0 or 2

Figure 53. Effects of Unsynchronized OCR Latching in Overflow Mode.

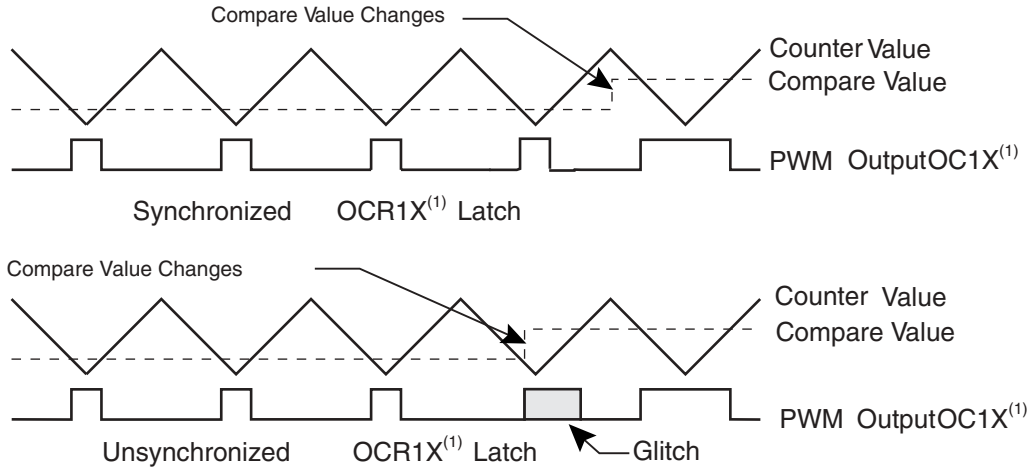


Note: 1. n = 0 or 2

During the time between the write and the latch operation, a read from the Output Compare Registers will read the contents of the temporary location. This means that the most recently written value always will read out of OCR0 and OCR2.

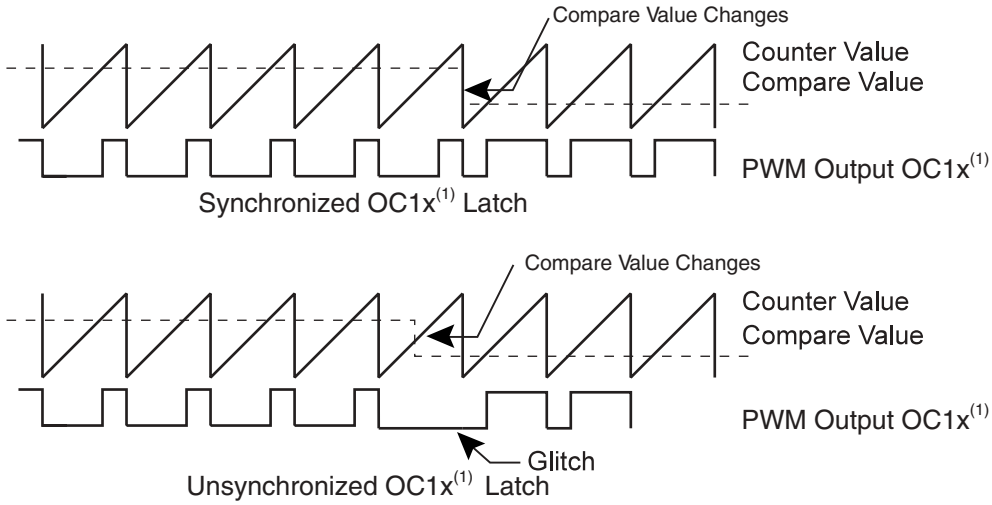
When the Output Compare Register contains $00 or $FF, and the up/down PWM mode is selected, the output PE1(OC0/PWM0)/PE3(OC2/PWM2) is updated to Low or High on the next compare match according to the settings of COMn1/COMn0. This is shown in Table 26. In overflow PWM mode, the output PE1(OC0/PWM0)/PE3(OC2/PWM2) is held Low or High only when the Output Compare Register contains $FF.

Figure 56. Effects on Unsynchronized OCR1 Latching



Note: 1. X = A or B

Figure 57. Effects of Unsynchronized OCR1 Latching in Overflow Mode



Note: 1. X = A or B

During the time between the write and the latch operation, a read from OCR1A or OCR1B will read the contents of the temporary location. This means that the most recently written value always will read out of OCR1A/B.

When the OCR1X contains $0000 or TOP, and the up/down PWM mode is selected, the output OC1A/OC1B is updated to Low or High on the next compare match according to the settings of COM1A1/COM1A0 or COM1B1/COM1B0. This is shown in Table 32. In overflow PWM mode, the output OC1A/OC1B is held Low or High only when the Output Compare Register contains TOP.

Watchdog Timer Control Register – WDTCR

Bit	7	6	5	4	3	2	1	0	
$21 ($41)	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..5 - Res: Reserved Bits**

These bits are reserved bits in the FPSLIC and will always read as zero.

- **Bit 4 - WDTOE: Watchdog Turn-off Enable**

This bit must be set (one) when the WDE bit is cleared. Otherwise, the watchdog will not be disabled. Once set, the hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit below for a watchdog disable procedure.

- **Bit 3 - WDE: Watchdog Enable**

When the WDE is set (one) the Watchdog Timer is enabled, but if the WDE is cleared (zero), the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit is set (one). To disable an enabled Watchdog Timer, the following procedure must be followed:

1. In the same operation, write a logic 1 to WDTOE and WDE. A logic 1 must be written to WDE even though it is set to one before the disable operation starts.
2. Within the next four clock cycles, write a logic 0 to WDE. This disables the watchdog.

- **Bits 2..0 - WDP2, WDP1, WDP0: Watchdog Timer Prescaler 2, 1 and 0**

The WDP2, WDP1 and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding Time-out periods are shown in Table 33.

Table 33. Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles(1)	Typical Time-out at V_{CC} = 3.0V
0	0	0	16K	15 ms
0	0	1	32K	30 ms
0	1	0	64K	60 ms
0	1	1	128K	0.12s
1	0	0	256K	0.24s
1	0	1	512K	0.49s
1	1	0	1,024K	0.97s
1	1	1	2,048K	1.9s

Note: 1. The frequency of the watchdog oscillator is voltage dependent as shown in the Electrical Characteristics section. The WDR (watchdog reset) instruction should always be executed before the Watchdog Timer is enabled. This ensures that the reset period will be in accordance with the Watchdog Timer prescale settings. If the Watchdog Timer is enabled without reset, the Watchdog Timer may not start counting from zero.

fmuls16x16_32

Description

Signed fractional multiply of two 16-bit numbers with a 32-bit result.

Usage

R19:R18:R17:R16 = (R23:R22 • R21:R20) << 1

Statistics

Cycles: 20 + ret

Words: 16 + ret

Register usage: R0 to R2 and R16 to R23 (11 registers)[1]

Note: 1. The routine is non-destructive to the operands.

```
fmuls16x16_32:
   clr   r2
   fmuls r23, r21             ; ( (signed)ah * (signed)bh ) << 1
   movw  r19:r18, r1:r0
   fmul  r22, r20             ; ( al * bl ) << 1
   adc   r18, r2
   movw  r17:r16, r1:r0
   fmulsu   r23, r20          ; ( (signed)ah * bl ) << 1
   sbc   r19, r2              ; Sign extend
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   fmulsu   r21, r22          ; ( (signed)bh * al ) << 1
   sbc   r19, r2              ; Sign extend
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   ret
```

fmac16x16_32

Description

Signed fractional multiply-accumulate of two 16-bit numbers with a 32-bit result.

Usage

R19:R18:R17:R16 += (R23:R22 • R21:R20) << 1

Statistics

Cycles: 25 + ret

Words: 21 + ret

Register usage: R0 to R2 and R16 to R23 (11 registers)

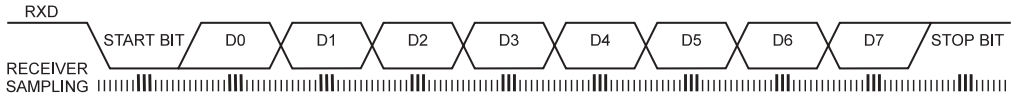
```
fmac16x16_32:                 ; Register usage optimized
   clr   r2

   fmuls r23, r21             ; ( (signed)ah * (signed)bh ) << 1
   add   r18, r0
   adc   r19, r1

   fmul  r22, r20             ; ( al * bl ) << 1
   adc   r18, r2
   adc   r19, r2
   add   r16, r0
```

If however, a valid start bit is detected, sampling of the data bits following the start bit is performed. These bits are also sampled at samples 8, 9 and 10. The logical value found in at least two of the three samples is taken as the bit value. All bits are shifted into the transmitter shift register as they are sampled. Sampling of an incoming character is shown in Figure 66. Note that the description above is not valid when the UART transmission speed is doubled. See “Double Speed Transmission” on page 128 for a detailed description.

Figure 66. Sampling Received Data[1]



Note: 1. This figure is not valid when the UART speed is doubled. See “Double Speed Transmission” on page 128 for a detailed description.

When the stop bit enters the receiver, the majority of the three samples must be one to accept the stop bit. If two or more samples are logic 0s, the Framing Error (FEn) flag in the UART Control and Status Register (UCSRnA) is set. Before reading the UDRn register, the user should always check the FEn bit to detect Framing Errors.

Whether or not a valid stop bit is detected at the end of a character reception cycle, the data is transferred to UDRn and the RXCn flag in UCSRnA is set. UDRn is in fact two physically separate registers, one for transmitted data and one for received data. When UDRn is read, the Receive Data register is accessed, and when UDRn is written, the Transmit Data register is accessed. If the 9-bit data word is selected (the CHR9n bit in the UART Control and Status Register, UCSRnB is set), the RXB8n bit in UCSRnB is loaded with bit 9 in the Transmit shift register when data is transferred to UDRn.

If, after having received a character, the UDRn register has not been read since the last receive, the OverRun (ORn) flag in UCSRnB is set. This means that the last data byte shifted into to the shift register could not be transferred to UDRn and has been lost. The ORn bit is buffered, and is updated when the valid data byte in UDRn is read. Thus, the user should always check the ORn bit after reading the UDRn register in order to detect any overruns if the baud-rate is High or CPU load is High.

When the RXEN bit in the UCSRnB register is cleared (zero), the receiver is disabled. This means that the PE1 (n=0) or PE3 (n=1) pin can be used as a general I/O pin. When $RXEN_n$ is set, the UART Receiver will be connected to PE1 (UART0) or PE3 (UART1), which is forced to be an input pin regardless of the setting of the DDE1 in DDRE (UART0) or DDB2 bit in DDRB (UART1). When PE1 (UART0) or PE3 (UART1) is forced to input by the UART, the PORTE1 (UART0) or PORTE3 (UART1) bit can still be used to control the pull-up resistor on the pin.

When the CHR9n bit in the UCSRnB register is set, transmitted and received characters are 9 bits long plus start and stop bits. The 9th data bit to be transmitted is the TXB8n bit in UCSRnB register. This bit must be set to the wanted value before a transmission is initiated by writing to the UDRn register. The 9th data bit received is the RXB8n bit in the UCSRnB register.

Table 37. UBR Settings at Various Crystal Frequencies in Double UART Speed Mode

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
1	**0000**	**00110011**	**033**	**51**	**2404**	**2400**	**0.2**
	0000	**00011001**	**019**	**25**	**4808**	**4800**	**0.2**
	0000	**00001100**	**00C**	**12**	**9615**	**9600**	**0.2**
	0000	00001000	008	8	13889	14400	3.7
	0000	00000110	006	6	17857	19200	7.5
	0000	00000011	003	3	31250	28880	7.6
	0000	00000010	002	2	41667	38400	7.8
	0000	00000001	001	1	62500	57600	7.8
	0000	00000001	001	1	62500	76800	22.9
	0000	00000000	000	0	125000	115200	7.8

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
1.843	**0000**	**01011111**	**05F**	**95**	**2400**	**2400**	**0.0**
	0000	**00101111**	**02F**	**47**	**4800**	**4800**	**0.0**
	0000	**00010111**	**017**	**23**	**9600**	**9600**	**0.0**
	0000	**00001111**	**00F**	**15**	**14400**	**14400**	**0.0**
	0000	**00001011**	**00B**	**11**	**19200**	**19200**	**0.0**
	0000	**00000111**	**007**	**7**	**28800**	**28880**	**0.3**
	0000	**00000101**	**005**	**5**	**38400**	**38400**	**0.0**
	0000	**00000011**	**003**	**3**	**57600**	**57600**	**0.0**
	0000	**00000010**	**002**	**2**	**76800**	**76800**	**0.0**
	0000	**00000001**	**001**	**1**	**115200**	**115200**	**0.0**

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
9.216	**0001**	**11011111**	**1DF**	**479**	**2400**	**2400**	**0.0**
	0000	**11101111**	**0EF**	**239**	**4800**	**4800**	**0.0**
	0000	**01110111**	**077**	**119**	**9600**	**9600**	**0.0**
	0000	**01001111**	**04F**	**79**	**14400**	**14400**	**0.0**
	0000	**00111011**	**03B**	**59**	**19200**	**19200**	**0.0**
	0000	**00100111**	**027**	**39**	**28800**	**28880**	**0.3**
	0000	**00011101**	**01D**	**29**	**38400**	**38400**	**0.0**
	0000	**00010011**	**013**	**19**	**57600**	**57600**	**0.0**
	0000	**00001110**	**00E**	**14**	**76800**	**76800**	**0.0**
	0000	**00001001**	**009**	**9**	**115200**	**115200**	**0.0**
	0000	**00000100**	**004**	**4**	**230400**	**230400**	**0.0**
	0000	00000010	002	2	384000	460800	20.0
	0000	00000000	000	0	1152000	912600	20.8

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
18.43	**0011**	**10111111**	**3BF**	**959**	**2400**	**2400**	**0.0**
	0001	**11011111**	**1DF**	**479**	**4800**	**4800**	**0.0**
	0000	**11101111**	**0EF**	**239**	**9600**	**9600**	**0.0**
	0000	**10011111**	**09F**	**159**	**14400**	**14400**	**0.0**
	0000	**01110111**	**077**	**119**	**19200**	**19200**	**0.0**
	0000	**01001111**	**04F**	**79**	**28800**	**28880**	**0.3**
	0000	**00111011**	**03B**	**59**	**38400**	**38400**	**0.0**
	0000	**00100111**	**027**	**39**	**57600**	**57600**	**0.0**
	0000	**00011101**	**01D**	**29**	**76800**	**76800**	**0.0**
	0000	**00010011**	**013**	**19**	**115200**	**115200**	**0.0**
	0000	**00001001**	**009**	**9**	**230400**	**230400**	**0.0**
	0000	**00000100**	**004**	**4**	**460800**	**460800**	**0.0**
	0000	00000010	002	2	**768000**	912600	18.8

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
25.576	**0101**	**00110011**	**533**	**1331**	**2400**	**2400**	**0.0**
	0010	**10011001**	**299**	**665**	**4800**	**4800**	**0.0**
	0001	**01001110**	**14E**	**334**	**9543**	**9600**	**0.6**
	0000	**11011101**	**0DD**	**221**	**14401**	**14400**	**0.0**
	0000	**10100110**	**0A6**	**166**	**19144**	**19200**	**0.3**
	0000	**01101110**	**06E**	**110**	**28802**	**28880**	**0.3**
	0000	**01010010**	**052**	**82**	**38518**	**38400**	**0.3**
	0000	00110111	037	55	57089	57600	0.9
	0000	00101001	029	41	76119	76800	0.9
	0000	00011011	01B	27	114179	115200	0.9
	0000	00001101	00D	13	228357	230400	0.9
	0000	00000110	006	6	456714	460800	0.9
	0000	00000011	003	3	799250	912600	14.2

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
40	**1000**	**00100010**	**822**	**2082**	**2400**	**2400**	**0.0**
	0100	**00010001**	**411**	**1041**	**4798**	**4800**	**0.0**
	0010	**00001000**	**208**	**520**	**9597**	**9600**	**0.0**
	0001	**01011010**	**15A**	**346**	**14409**	**14400**	**0.1**
	0001	**00000011**	**103**	**259**	**19231**	**19200**	**0.2**
	0000	**10101100**	**0AC**	**172**	**28902**	**28880**	**0.1**
	0000	**10000001**	**081**	**129**	**38462**	**38400**	**0.2**
	0000	**01010110**	**056**	**86**	**57471**	**57600**	**0.2**
	0000	**01000000**	**040**	**64**	**76923**	**76800**	**0.2**
	0000	00101010	02A	42	116279	115200	0.9
	0000	00010101	015	21	227273	230400	1.4
	0000	00001010	00A	10	454545	460800	1.4
	0000	00000100	004	4	1000000	912600	8.7

Table 41. Status Codes for Master Transmitter Mode

Status Code (TWSR)	Status of the 2-wire Serial Bus and 2-wire Serial Hardware	Application Software Response					Next Action Taken by 2-wire Serial Hardware
		To/From TWDR	To TWCR				
			STA	STO	TWINT	TWEA	
$08	A START condition has been transmitted	Load SLA+W	X	0	1	X	SLA+W will be transmitted; ACK or NOT ACK will be received
$10	A repeated START condition has been transmitted	Load SLA+W or	X	0	1	X	SLA+W will be transmitted; ACK or NOT ACK will be received
		Load SLA+R	X	0	1	X	SLA+R will be transmitted; Logic will switch to Master Receiver mode
$18	SLA+W has been transmitted; ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
$20	SLA+W has been transmitted; NOT ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
$28	Data byte has been transmitted; ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
$30	Data byte has been transmitted; NOT ACK has been received	Load data byte or	0	0	1	X	Data byte will be transmitted and ACK or NOT ACK will be received
		No TWDR action or	1	0	1	X	Repeated START will be transmitted
		No TWDR action or	0	1	1	X	STOP condition will be transmitted and TWSTO flag will be reset
		No TWDR action	1	1	1	X	STOP condition followed by a START condition will be transmitted and TWSTO flag will be reset
$38	Arbitration lost in SLA+W or data bytes	No TWDR action or	0	0	1	X	2-wire serial bus will be released and not addressed Slave mode entered
		No TWDR action	1	0	1	X	A START condition will be transmitted when the bus becomes free

I/O Ports

All AVR ports have true read-modify-write functionality when used as general I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

PortD

PortD is an 8-bit bi-directional I/O port with internal pull-up resistors.

Three I/O memory address locations are allocated for the PortD, one each for the Data Register – PORTD, $12($32), Data Direction Register – DDRD, $11($31) and the Port D Input Pins – PIND, $10($30). The Port D Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

The PortD output buffers can sink 20 mA. As inputs, PortD pins that are externally pulled Low will source current if the pull-up resistors are activated.

PortD Data Register – PORTD

Bit	7	6	5	4	3	2	1	0	
$12	**PORTD7**	**PORTD6**	**PORTD5**	**PORTD4**	**PORTD3**	**PORTD2**	**PORTD1**	**PORTD0**	**PORTD**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

PortD Data Direction Register – DDRD

Bit	7	6	5	4	3	2	1	0	
$11	**DDD7**	**DDD6**	**DDD5**	**DDD4**	**DDD3**	**DDD2**	**DDD1**	**DDD0**	**DDRD**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortD Input Pins Address – PIND

Bit	7	6	5	4	3	2	1	0	
$10	**PIND7**	**PIND6**	**PIND5**	**PIND4**	**PIND3**	**PIND2**	**PIND1**	**PIND0**	**PIND**
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	Pull1	Pull1	Pull1	Pull1	Pull1	Pull1	Pull1	Pull1	

The PortD Input Pins address – PIND – is not a register, and this address enables access to the physical value on each PortD pin. When reading PORTD, the PortD Data Latch is read, and when reading PIND, the logical values present on the pins are read.

PortD as General Digital I/O

PDn, General I/O pin: The DDDn bit in the DDRD register selects the direction of this pin. If DDDn is set (one), PDn is configured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. If PDn is set (one) when configured as an input pin the MOS pull-up resistor is activated. To switch the pull-up resistor off the PDn has to be cleared (zero) or the pin has to be configured as an output pin. The port pins are input with pull-up when a reset condition becomes active, even if the clock is not running, see Table 46.

AC & DC Timing Characteristics

Absolute Maximum Ratings*(1)

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage(2) on Any Pin with Respect to Ground	-0.5V to +5.0V
Supply Voltage (V_{CC})	-0.5V to +5.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Notes: 1. For AL parts only
2. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

DC and AC Operating Range – 3.3V Operation

		AT94K Commercial	AT94K Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-25	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	E -> E	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	L -> L	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	E -> L	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	E -> IO	1.4	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	L -> IO	1.4	ns	1 Unit Load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-25	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.9	ns	No Extra Delay
Input	t_{PD} (Maximum)	pad -> x/y	5.8	ns	1 Extra Delay
Input	t_{PD} (Maximum)	pad -> x/y	11.5	ns	2 Extra Delays
Input	t_{PD} (Maximum)	pad -> x/y	17.4	ns	3 Extra Delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	9.1	ns	50 pf Load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	7.6	ns	50 pf Load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	6.2	ns	50 pf Load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	9.5	ns	50 pf Load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	2.1	ns	50 pf Load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	7.4	ns	50 pf Load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	2.7	ns	50 pf Load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	5.9	ns	50 pf Load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	2.4	ns	50 pf Load

Table 56. AT94K Pin List (Continued)

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
I/O55	I/O83	I/O167			62	88
I/O56	I/O84	I/O168			63	89
GND	GND	GND			64	90
		I/O169				
		I/O170				
	I/O85	I/O171				
	I/O86	I/O172				
		I/O173				
		I/O174				
		GND				
		I/O175				
		I/O176				
	I/O87	I/O177				91
	I/O88	I/O178				92
I/O57	I/O89	I/O179				93
I/O58	I/O90	I/O180				94
		GND				
		VCC(1)				
		I/O181				
		I/O182				
I/O59 (TD2)	I/O91 (TD2)	I/O183 (TD2)	48	45	65	95
I/O60 (TD1)	I/O92 (TD1)	I/O184 (TD1)	49	46	66	96
		I/O185				
		I/O186				
		GND				
		I/O187				
		I/O188				
I/O61	I/O93	I/O189			67	97
I/O62	I/O94	I/O190			68	98
I/O63 (TD0)	I/O95 (TD0)	I/O191 (TD0)	50	47	69	99
I/O64, GCK4	I/O96, GCK4	I/O192, GCK4	51	48	70	100
GND	GND	GND	52	49	71	101
$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	53	50	72	103
East Side						

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.