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Embedded - FPGAs (Field Programmable Gate Array) with Microcontrollers: Enhancing Flexibility and Performance

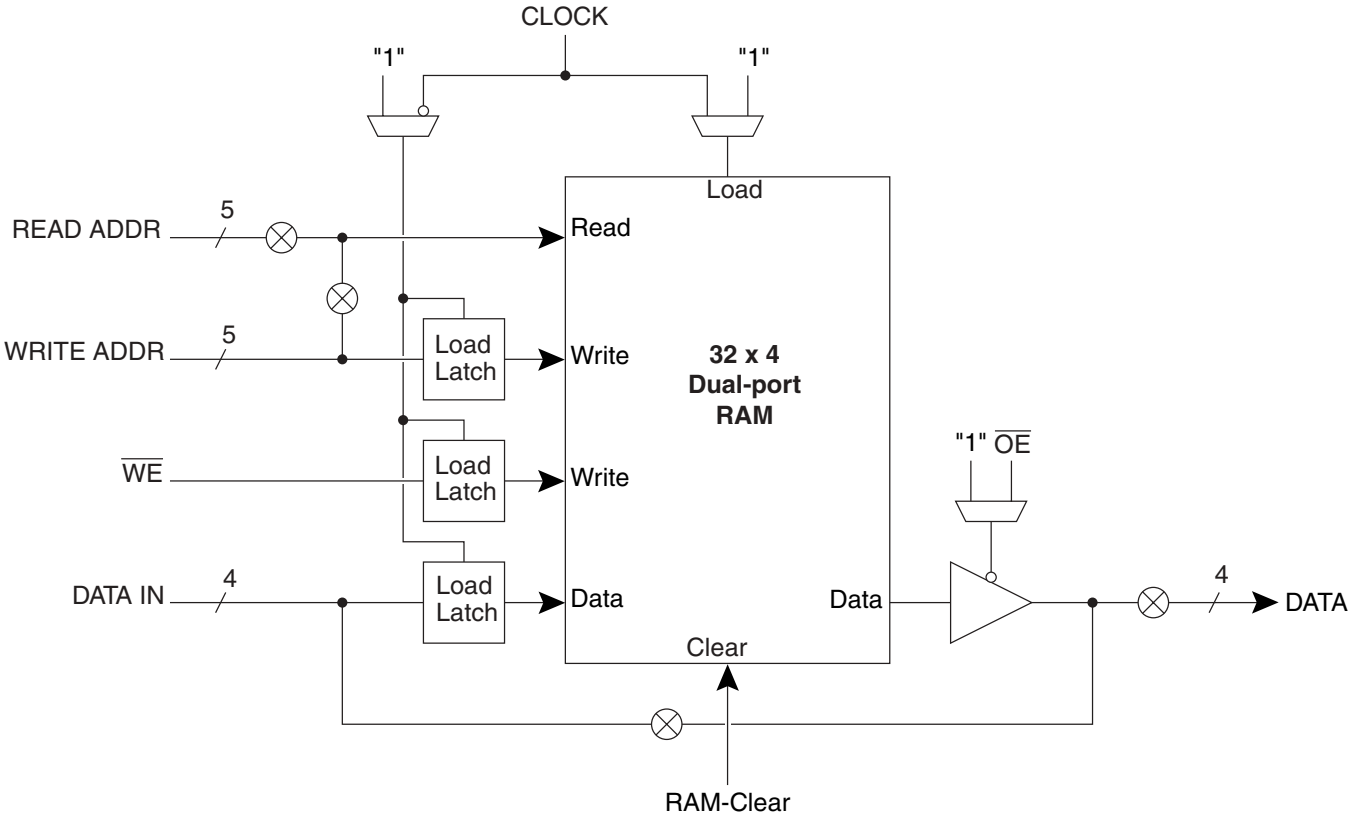
Embedded - FPGAs (Field Programmable Gate Arrays) with Microcontrollers represent a cutting-edge category of electronic components that combine the flexibility of FPGA technology with the processing power of integrated microcontrollers. This hybrid approach offers a versatile solution for designing and implementing complex digital systems that require both programmable logic and embedded processing capabilities.

What Are Embedded - FPGAs with Microcontrollers?

At their core, **FPGAs** are semiconductor devices that can

Details	
Product Status	Obsolete
Core Type	8-Bit AVR
Speed	25 MHz
Interface	I²C, UART
Program SRAM Bytes	4K-16K
FPGA SRAM	2kb
EEPROM Size	-
Data SRAM Bytes	4K ~ 16K
FPGA Core Cells	256
FPGA Gates	5K
FPGA Registers	436
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at94k05al-25bqc

Figure 9. FreeRAM Logic[1]



Note: 1. For dual port, the switches on READ ADDR and DATA OUT would be on. The other two would be off. The reverse is true for single port.

Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clock
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half-carry Flag in SREG	H ← 1	H	1
CLH		Clear Half-carry Flag in SREG	H ← 0	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(See specific description for Sleep)	None	1
WDR		Watchdog Reset	(See specific description for WDR)	None	1
BREAK		Break	For on-chip debug only	None	N/A

Pin Descriptions

V_{CC} Supply voltage

GND Ground

PortD (PD7..PD0) Port D is an 8-bit bi-directional I/O port with internal programmable pull-up resistors. The Port D output buffers can be programmed to sink/source either 6 or 20 mA (SCR54 – see "System Control Register – FPGA/AVR" on page 30). As inputs, Port D pins that are externally pulled Low will source current if the programmable pull-up resistors are activated.

The Port D pins are input with pull-up when a reset condition becomes active, even if the clock is not running. On lower pin count packages Port D may not be available. Check the Pin List for details.

PortE (PE7..PE0) Port E is an 8-bit bi-directional I/O port with internal programmable pull-up resistors. The Port E output buffers can be programmed to sink/source either 6 or 20 mA (SCR55 – see "System Control Register – FPGA/AVR" on page 30). As inputs, Port E pins that are externally pulled Low will source current if the pull-up resistors are activated.

Port E also serves the functions of various special features. See Table 47 on page 149.

The Port E pins are input with pull-up when a reset condition becomes active, even if the clock is not running

RX0 Input (receive) to UART(0) – See SCR52

TX0 Output (transmit) from UART(0) – See SCR52

RX1 Input (receive) to UART(1) – See SCR53

TX1 Output (transmit) from UART(1) – See SCR53

XTAL1 Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Memory-mapped I/O

The I/O space definition of the embedded AVR core is shown in the following table:

AT94K Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	51
$3E ($5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	57
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	51
$3C ($5C)	Reserved									
$3B ($5B)	EIMF	INTF3	INTF2	INTF1	INTF0	INT3	INT2	INT1	INT0	62
$3A ($5A)	SFTCR					FMXOR	WDTS	DBG	SRST	51
$39 ($59)	TIMSK	TOIE1	OCIE1A	OCIE1B	TOIE2	TICIE1	OCIE2	TOIE0	OCIE0	62
$38 ($58)	TIFR	TOV1	OCF1A	OCF1B	TOV2	ICF1	OCF2	TOV0	OCF0	63
$37 ($57)	Reserved									
$36 ($56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN		TWIE	110
$35 ($55)	MCUR	JTRF	JTD	SE	SM1	SM0	PORF	WDRF	EXTRF	51
$34 ($54)	Reserved									
$33 ($53)	TCCR0	FOC0	PWM0	COM01	COM00	CTC0	CS02	CS01	CS00	69
$32 ($52)	TCNT0	Timer/Counter0 (8-bit)								70
$31 ($51)	OCR0	Timer/Counter0 Output Compare Register								71
$30 ($50)	SFIOR							PSR2	PSR10	66
$2F ($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	PWM11	PWM10	76
$2E ($4E)	TCCR1B	ICNC1	ICES1	ICPE		CTC1	CS12	CS11	CS10	77
$2D ($4D)	TCNT1H	Timer/Counter1 - Counter Register High Byte								78
$2C ($4C)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								78
$2B ($4B)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								79
$2A ($4A)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								79
$29 ($49)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								79
$28 ($48)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								79
$27 ($47)	TCCR2	FOC2	PWM2	COM21	COM20	CTC2	CS22	CS21	CS20	69
$26 ($46)	ASSR					AS2	TCN20B	OCR2UB	TCR2UB	73
$25 ($45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								80
$24 ($44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								80
$23 ($43)	TCNT2	Timer/Counter2 (8-bit)								70
$22 ($42)	OCR2	Timer/Counter 2 Output Compare Register								71
$21 ($41)	WDTCR				WDTOE	WDE	WDP2	WDP1	WDP0	83
$20 ($40)	UBRRHI	UART1 Baud Rate High Nibble [11..8]				UART0 Baud Rate Low Nibble [11..8]				105
$1F ($3F)	TWDR	2-wire Serial Data Register								111
$1E ($3E)	TWAR	2-wire Serial Address Register								112
$1D ($3D)	TWSR	2-wire Serial Status Register								112
$1C ($3C)	TWBR	2-wire Serial Bit Rate Register								109
$1B ($3B)	FPGAD	FPGA Cache Data Register (D7 - D0)								52
$1A ($3A)	FPGAZ	FPGA Cache Z Address Register (T3 - T0) (Z3 - Z0)								53
$19 ($39)	FPGAY	FPGA Cache Y Address Register (Y7 - Y0)								53
$18 ($38)	FPGAX	FPGA Cache X Address Register (X7 - X0)								53
$17 ($37)	FISUD	FPGA I/O Select, Interrupt Mask/Flag Register D (Reserved on AT94K05)								54, 56

Table 16. Reset Characteristics (V_{CC} = 3.3V)

Symbol	Parameter	Minimum	Typical	Maximum	Units
$V_{POT(1)}$	Power-on Reset Threshold (Rising)	1.0	1.4	1.8	V
	Power-on Reset Threshold (Falling)	0.4	0.6	0.8	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		$V_{CC}/2$		V
T_{TOUT}	Reset Delay Time-out Period		5		CPU cycles
		0.4 3.2 12.8	0.5 4.0 16.0	0.6 4.8 19.2	ms

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Power-on Reset

A Power-on Reset (POR) circuit ensures that the device is reset from power-on. As shown in Figure 35, an internal timer clocked from the Watchdog Timer oscillator prevents the MCU from starting until after a certain period after V_{CC} has reached the Power-on Threshold voltage – V_{POT}, regardless of the V_{CC} rise time (see Figure 36 and Figure 37).

Figure 36. MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}

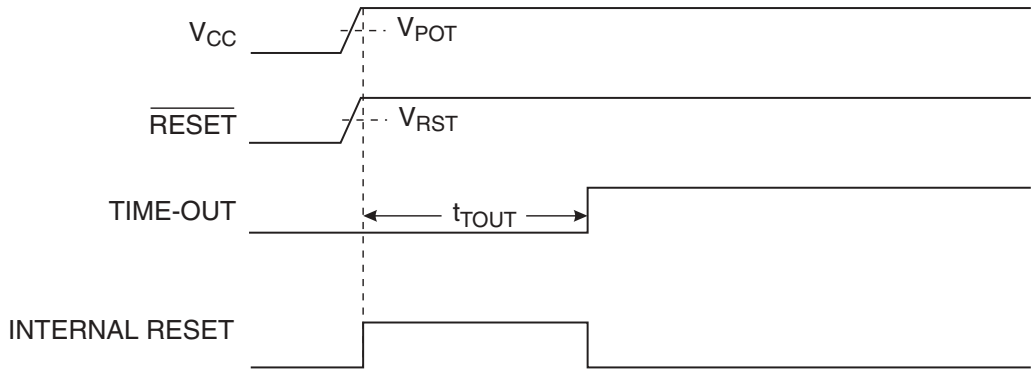
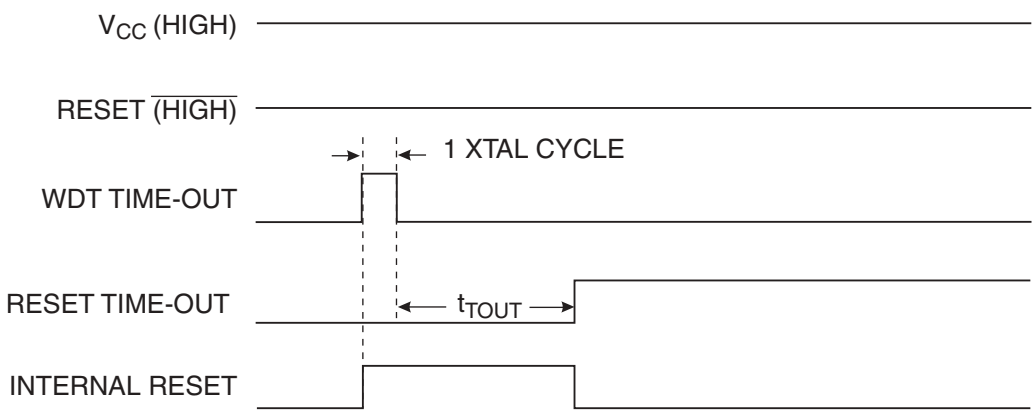


Figure 37. Watchdog Reset during Operation



On-chip Debug Specific JTAG Instructions

The On-Chip debug support is considered being private JTAG instructions, and distributed within ATMEL and to selected third-party vendors only. Table 17 lists the instruction opcode.

Table 17. JTAG Instruction and Code

JTAG Instruction	4-bit Code	Selected Scan Chain	# Bits
EXTEST	$0 (0000)	AVR I/O Boundary	69
IDCODE	$1 (0001)	Device ID	32
SAMPLE_PRELOAD	$2 (0010)	AVR I/O Boundary	69
RESERVED	$3 (0011)	N/A	–
PRIVATE	$4 (0100)	FPSLIC On-chip Debug System	–
PRIVATE	$5 (0101)	FPSLIC On-chip Debug System	–
PRIVATE	$6 (0110)	FPSLIC On-chip Debug System	–
RESERVED	$7 (0111)	N/A	–
PRIVATE	$8 (1000)	FPSLIC On-chip Debug System	–
PRIVATE	$9 (1001)	FPSLIC On-chip Debug System	–
PRIVATE	$A (1010)	FPSLIC On-chip Debug System	–
PRIVATE	$B (1011)	FPSLIC On-chip Debug System	–
AVR_RESET	$C (1100)	AVR Reset	1
RESERVED	$D (1101)	N/A	–
RESERVED	$E (1110)	N/A	–
BYPASS	$F (1111)	Bypass	1

IEEE 1149.1 (JTAG) Boundary-scan

Features

- **JTAG (IEEE std. 1149.1 compliant) Interface**
- **Boundary-scan Capabilities According to the JTAG Standard**
- **Full Scan of All Port Functions**
- **Supports the Optional IDCODE Instruction**
- **Additional Public AVR_RESET Instruction to Reset the AVR**

System Overview

The Boundary-Scan chain has the capability of driving and observing the logic levels on the AVR's digital I/O pins. At system level, all ICs having JTAG capabilities are connected serially by the TDI/TDO signals to form a long shift register. An external controller sets up the devices to drive values at their output pins, and observe the input values received from other devices. The controller compares the received data with the expected result. In this way, Boundary-Scan provides a mechanism for testing interconnections and integrity of components on Printed Circuits Boards by using the 4 TAP signals only.

The four IEEE 1149.1 defined mandatory JTAG instructions IDCODE, BYPASS, SAMPLE/PRELOAD, and EXTEST, as well as the AVR specific public JTAG instruction AVR_RESET can be used for testing the Printed Circuit Board. Initial scanning of the data register path will show the ID-code of the device, since IDCODE is the default JTAG instruction. It may be desirable to have the AVR device in reset during test mode. If not reset, inputs to the device may be determined by the scan operations, and the internal software may be in an

Table 20. AVR I/O Boundary Scan – JTAG Instructions $0/$2

I/O Ports	Description	Bit
PORTD	Data Out/In - PD7	44
	Enable Output - PD7	43
	Pull-up - PD7	42
	Data Out/In - PD6	41
	Enable Output - PD6	40
	Pull-up - PD6	39
	Data Out/In - PD5	38
	Enable Output - PD5	37
	Pull-up - PD5	36
	Data Out/In - PD4	35
	Enable Output - PD4	34
	Pull-up - PD4	33
	Data Out/In - PD3	32
	Enable Output - PD3	31
	Pull-up - PD3	30
	Data Out/In - PD2	29
	Enable Output - PD2	28
	Pull-up - PD2	27
	Data Out/In - PD1	26
	Enable Output - PD1	25
	Pull-up - PD1	24
	Data Out/In - PD0	23
	Enable Output - PD0	22
	Pull-up - PD0	21
EXT. INTERRUPTS	Input with Pull-up - INTP3	20[1]
	Input with Pull-up - INTP2	19[1]
	Input with Pull-up - INTP1	18[1]
	Input with Pull-up - INTP0	17[1]
UART1	Data Out/In - TX1	16
	Enable Output - TX1	15
	Pull-up - TX1	14
	Input with Pull-up - RX1	13[1]
UART0	Data Out/In - TX0	12
	Enable Output - TX0	11
	Pull-up - TX0	10
	Input with Pull-up - RX0	9[1]

Implementations

mul16x16_16

Description

Multiply of two 16-bit numbers with a 16-bit result.

Usage

R17:R16 = R23:R22 • R21:R20

Statistics

Cycles: 9 + ret

Words: 6 + ret

Register usage: R0, R1 and R16 to R23 (8 registers)(1)

Note: 1. Full orthogonality, i.e., any register pair can be used as long as the result and the two operands do not share register pairs. The routine is non-destructive to the operands.

```
mul16x16_16:
   mul   r22, r20        ; al * bl
   movw  r17:r16, r1:r0
   mul   r23, r20        ; ah * bl
   add   r17, r0
   mul   r21, r22        ; bh * al
   add   r17, r0
   ret
```

mul16x16_32

Description

Unsigned multiply of two 16-bit numbers with a 32-bit result.

Usage

R19:R18:R17:R16 = R23:R22 • R21:R20

Statistics

Cycles: 17 + ret

Words: 13 + ret

Register usage: R0 to R2 and R16 to R23 (11 registers)(1)

Note: 1. Full orthogonality, i.e., any register pair can be used as long as the result and the two operands do not share register pairs. The routine is non-destructive to the operands.

```
mul16x16_32:
   clr   r2
   mul   r23, r21        ; ah * bh
   movw  r19:r18, r1:r0
   mul   r22, r20        ; al * bl
   movw  r17:r16, r1:r0
   mul   r23, r20        ; ah * bl
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   mul   r21, r22        ; bh * al
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   ret
```

Multi-processor Communication Mode

The Multi-processor Communication Mode enables several Slave MCUs to receive data from a Master MCU. This is done by first decoding an address byte to find out which MCU has been addressed. If a particular Slave MCU has been addressed, it will receive the following data bytes as normal, while the other Slave MCUs will ignore the data bytes until another address byte is received.

For an MCU to act as a Master MCU, it should enter 9-bit transmission mode (CHR9n in UCSRnB set). The 9-bit must be one to indicate that an address byte is being transmitted, and zero to indicate that a data byte is being transmitted.

For the Slave MCUs, the mechanism appears slightly different for 8-bit and 9-bit Reception mode. In 8-bit Reception mode (CHR9n in UCSRnB cleared), the stop bit is one for an address byte and zero for a data byte. In 9-bit Reception mode (CHR9n in UCSRnB set), the 9-bit is one for an address byte and zero for a data byte, whereas the stop bit is always High.

The following procedure should be used to exchange data in Multi-processor Communication mode:

1. All Slave MCUs are in Multi-processor Communication Mode (MPCMn in UCSRnA is set).
2. The Master MCU sends an address byte, and all Slaves receive and read this byte. In the Slave MCUs, the RXCn flag in UCSRnA will be set as normal.
3. Each Slave MCU reads the UDRn register and determines if it has been selected. If so, it clears the MPCMn bit in UCSRnA, otherwise it waits for the next address byte.
4. For each received data byte, the receiving MCU will set the receive complete flag (RXCn in UCSRnA. In 8-bit mode, the receiving MCU will also generate a framing error (FEn in UCSRnA set), since the stop bit is zero. The other Slave MCUs, which still have the MPCMn bit set, will ignore the data byte. In this case, the UDRn register and the RXCn, FEn, or flags will not be affected.
5. After the last byte has been transferred, the process repeats from step 2.

UART Control

UART0 I/O Data Register – UDR0

Bit	7	6	5	4	3	2	1	0	
$0C ($2C)	MSB							LSB	UDR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

UART1 I/O Data Register – UDR1

Bit	7	6	5	4	3	2	1	0	
$03 ($23)	MSB							LSB	UDR1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The UDRn register is actually two physically separate registers sharing the same I/O address. When writing to the register, the UART Transmit Data register is written. When reading from UDRn, the UART Receive Data register is read.

Table 36. UBR Settings at Various Crystal Frequencies

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
1	**0000**	**00011001**	**019**	**25**	**2404**	**2400**	**0.2**
	0000	**00001100**	**00C**	**12**	**4808**	**4800**	**0.2**
	0000	00000110	006	6	8929	9600	7.5
	0000	00000011	003	3	15625	14400	7.8
	0000	00000010	002	2	20833	19200	7.8
	0000	00000001	001	1	31250	28880	7.6
	0000	00000001	001	1	31250	38400	22.9
	0000	00000000	000	0	62500	57600	7.8
	0000	00000000	000	0	62500	76800	22.9
	0000	00000000	000	0	62500	115200	84.3

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
1.8432	**0000**	**00101111**	**02F**	**47**	**2400**	**2400**	**0.0**
	0000	**00010111**	**017**	**23**	**4800**	**4800**	**0.0**
	0000	**00001011**	**00B**	**11**	**9600**	**9600**	**0.0**
	0000	**00000111**	**007**	**7**	**14400**	**14400**	**0.0**
	0000	**00000101**	**005**	**5**	**19200**	**19200**	**0.0**
	0000	**00000011**	**003**	**3**	**28800**	**28880**	**0.3**
	0000	**00000010**	**002**	**2**	**38400**	**38400**	**0.0**
	0000	**00000001**	**001**	**1**	**57600**	**57600**	**0.0**
	0000	00000001	001	1	57600	76800	33.3
	0000	**00000000**	**000**	**0**	**115200**	**115200**	**0.0**

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
9.216	**0000**	**11101111**	**0EF**	**239**	**2400**	**2400**	**0.0**
	0000	**01110111**	**077**	**119**	**4800**	**4800**	**0.0**
	0000	**00111011**	**03B**	**59**	**9600**	**9600**	**0.0**
	0000	**00100111**	**027**	**39**	**14400**	**14400**	**0.0**
	0000	**00011101**	**01D**	**29**	**19200**	**19200**	**0.0**
	0000	**00010011**	**013**	**19**	**28800**	**28880**	**0.3**
	0000	**00001110**	**00E**	**14**	**38400**	**38400**	**0.0**
	0000	**00001001**	**009**	**9**	**57600**	**57600**	**0.0**
	0000	00000111	007	7	72000	76800	6.7
	0000	**00000100**	**004**	**4**	**115200**	**115200**	**0.0**
	0000	00000001	001	1	288000	230400	20.0
	0000	00000000	000	0	576000	460800	20.0
	0000	00000000	000	0	576000	912600	58.4

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
18.432	**0001**	**11011111**	**1DF**	**479**	**2400**	**2400**	**0.0**
	0000	**11101111**	**0EF**	**239**	**4800**	**4800**	**0.0**
	0000	**01110111**	**077**	**119**	**9600**	**9600**	**0.0**
	0000	**01001111**	**04F**	**79**	**14400**	**14400**	**0.0**
	0000	**00111011**	**03B**	**59**	**19200**	**19200**	**0.0**
	0000	**00100111**	**027**	**39**	**28800**	**28880**	**0.3**
	0000	**00011101**	**01D**	**29**	**38400**	**38400**	**0.0**
	0000	**00010011**	**013**	**19**	**57600**	**57600**	**0.0**
	0000	**00001110**	**00E**	**14**	**76800**	**76800**	**0.0**
	0000	**00001001**	**009**	**9**	**115200**	**115200**	**0.0**
	0000	**00000100**	**004**	**4**	**230400**	**230400**	**0.0**
	0000	00000001	001	1	576000	460800	20.0
	0000	00000000	000	0	1152000	912600	20.8

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
25.576	**0010**	**10011001**	**299**	**665**	**2400**	**2400**	**0.0**
	0001	**01001100**	**14C**	**332**	**4800**	**4800**	**0.0**
	0000	**10100110**	**0A6**	**166**	**9572**	**9600**	**0.3**
	0000	**01101110**	**06E**	**110**	**14401**	**14400**	**0.0**
	0000	**01010010**	**052**	**82**	**19259**	**19200**	**0.3**
	0000	**00110110**	**036**	**54**	**29064**	**28880**	**0.6**
	0000	**00101001**	**029**	**41**	**38060**	**38400**	**0.9**
	0000	**00011011**	**01B**	**27**	**57089**	**57600**	**0.9**
	0000	**00010100**	**014**	**20**	**76119**	**76800**	**0.9**
	0000	**00001101**	**00D**	**13**	**114179**	**115200**	**0.9**
	0000	**00000110**	**006**	**6**	**228357**	**230400**	**0.9**
	0000	00000011	003	3	399625	460800	15.3
	0000	00000001	001	1	799250	912600	14.2

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
40	**0100**	**00010001**	**411**	**1041**	**2399**	**2400**	**0.0**
	0010	**00001000**	**208**	**520**	**4798**	**4800**	**0.0**
	0001	**00000011**	**103**	**259**	**9615**	**9600**	**0.2**
	0000	**10101100**	**0AC**	**172**	**14451**	**14400**	**0.4**
	0000	**10000001**	**081**	**129**	**19231**	**19200**	**0.2**
	0000	**01010110**	**056**	**86**	**28736**	**28880**	**0.5**
	0000	**01000000**	**040**	**64**	**38462**	**38400**	**0.2**
	0000	**00101010**	**02A**	**42**	**58140**	**57600**	**0.9**
	0000	00100000	020	32	75758	76800	1.4
	0000	00010101	015	21	113636	115200	1.4
	0000	00001010	00A	10	227273	230400	1.4
	0000	00000100	004	4	500000	460800	7.8
	0000	00000010	002	2	833333	912600	9.5

UART0 and UART1 High Byte Baud-rate Register UBRRHI

Bit	7	6	5	4	3	2	1	0	
$20 ($40)	**MSB1**			**LSB1**	**MSB0**			**LSB0**	**UBRRHI**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The UART baud register is a 12-bit register. The 4 most significant bits are located in a separate register, UBRRHI. Note that both UART0 and UART1 share this register. Bit 7 to bit 4 of UBRRHI contain the 4 most significant bits of the UART1 baud register. Bit 3 to bit 0 contain the 4 most significant bits of the UART0 baud register.

Figure 72. Formats and States in the Master Receiver Mode

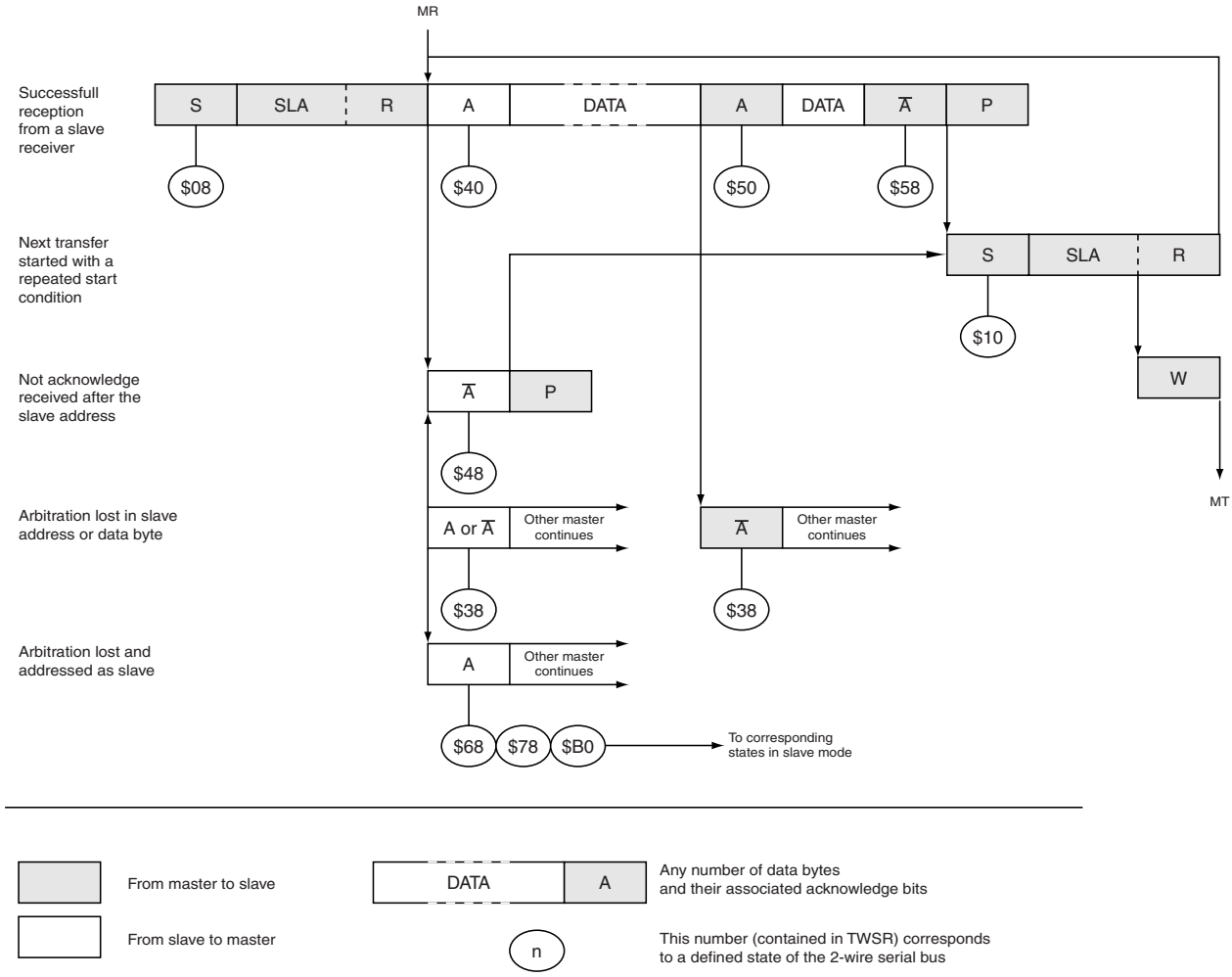


Table 44. Status Codes for Slave Transmitter Mode

Status Code (TWSR)	Status of the 2-wire Serial Bus and 2-wire Serial Hardware	Application Software Response					Next Action Taken by 2-wire Serial Hardware
			To TWCR				
		To/From TWDR	STA	STO	TWINT	TWEA	
$A8	Own SLA+R has been received; ACK has been returned	Load data byte or	X	0	1	0	Last data byte will be transmitted and NOT ACK should be received
		Load data byte	X	0	1	1	Data byte will be transmitted and ACK should be received
$B0	Arbitration lost in SLA+R/W as Master; own SLA+R has been received; ACK has been returned	Load data byte or	X	0	1	0	Last data byte will be transmitted and NOT ACK should be received
		Load data byte	X	0	1	1	Data byte will be transmitted and ACK should be received
$B8	Data byte in TWDR has been transmitted; ACK has been received	Load data byte or	X	0	1	0	Last data byte will be transmitted and NOT ACK should be received
		Load data byte	X	0	1	1	Data byte will be transmitted and ACK should be received
$C0	Data byte in TWDR has been transmitted; NOT ACK has been received	No TWDR action or	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		No TWDR action or	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”
		No TWDR action or	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		No TWDR action	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”; a START condition will be transmitted when the bus becomes free
$C8	Last data byte in TWDR has been transmitted (TWAE = “0”); ACK has been received	No TWDR action or	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		No TWDR action or	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”
		No TWDR action or	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		No TWDR action	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”; a START condition will be transmitted when the bus becomes free

I/O Ports

All AVR ports have true read-modify-write functionality when used as general I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

PortD

PortD is an 8-bit bi-directional I/O port with internal pull-up resistors.

Three I/O memory address locations are allocated for the PortD, one each for the Data Register – PORTD, $12($32), Data Direction Register – DDRD, $11($31) and the Port D Input Pins – PIND, $10($30). The Port D Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

The PortD output buffers can sink 20 mA. As inputs, PortD pins that are externally pulled Low will source current if the pull-up resistors are activated.

PortD Data Register – PORTD

Bit	7	6	5	4	3	2	1	0	
$12	**PORTD7**	**PORTD6**	**PORTD5**	**PORTD4**	**PORTD3**	**PORTD2**	**PORTD1**	**PORTD0**	**PORTD**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

PortD Data Direction Register – DDRD

Bit	7	6	5	4	3	2	1	0	
$11	**DDD7**	**DDD6**	**DDD5**	**DDD4**	**DDD3**	**DDD2**	**DDD1**	**DDD0**	**DDRD**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortD Input Pins Address – PIND

Bit	7	6	5	4	3	2	1	0	
$10	**PIND7**	**PIND6**	**PIND5**	**PIND4**	**PIND3**	**PIND2**	**PIND1**	**PIND0**	**PIND**
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	Pull1	Pull1	Pull1	Pull1	Pull1	Pull1	Pull1	Pull1	

The PortD Input Pins address – PIND – is not a register, and this address enables access to the physical value on each PortD pin. When reading PORTD, the PortD Data Latch is read, and when reading PIND, the logical values present on the pins are read.

PortD as General Digital I/O

PDn, General I/O pin: The DDDn bit in the DDRD register selects the direction of this pin. If DDDn is set (one), PDn is configured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. If PDn is set (one) when configured as an input pin the MOS pull-up resistor is activated. To switch the pull-up resistor off the PDn has to be cleared (zero) or the pin has to be configured as an output pin. The port pins are input with pull-up when a reset condition becomes active, even if the clock is not running, see Table 46.

AC & DC Timing Characteristics

Absolute Maximum Ratings*(1)

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage(2) on Any Pin with Respect to Ground	-0.5V to +5.0V
Supply Voltage (V_{CC})	-0.5V to +5.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Notes: 1. For AL parts only
2. Minimum voltage of -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns.

DC and AC Operating Range – 3.3V Operation

		AT94K Commercial	AT94K Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

Table 52. FPSLIC Interface Timing Information[1]

Symbol	Parameter	3.3V Commercial ± 10%			3.3V Industrial ± 10%			Units
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
t_{IXG4}	Clock Delay From XTAL2 Pad to GCK_5 Access to FPGA Core	3.6	4.8	7.6	3.4	4.8	7.9	ns
t_{IXG5}	Clock Delay From XTAL2 Pad to GCK_6 Access to FPGA Core	3.9	5.2	8.1	3.6	5.2	8.8	ns
t_{IXC}	Clock Delay From XTAL2 Pad to AVR Core Clock	2.8	3.7	6.3	2.5	3.7	6.9	ns
t_{IXI}	Clock Delay From XTAL2 Pad to AVR I/O Clock	3.5	4.7	7.5	3.2	4.7	7.8	ns
t_{CFIR}	AVR Core Clock to FPGA I/O Read Enable	5.3	6.6	7.9	4.4	6.6	9.2	ns
t_{CFIW}	AVR Core Clock to FPGA I/O Write Enable	5.2	6.6	7.9	4.4	6.6	9.2	ns
t_{CFIS}	AVR Core Clock to FPGA I/O Select Active	6.3	7.8	9.4	5.3	7.8	11.0	ns
t_{FIRQ}	FPGA Interrupt Net Propagation Delay to AVR Core	0.2	0.2	0.3	0.1	0.2	0.3	ns
t_{IFS}	FPGA SRAM Clock to On-chip SRAM	6.1	7.7	7.7	4.9	7.7	7.7	ns
t_{FRWS}	FPGA SRAM Write Stobe to On-chip SRAM	4.4	5.5	5.5	3.7	5.5	5.5	ns
t_{FAS}	FPGA SRAM Address Valid to On-chip SRAM Address Valid	5.4	6.7	6.7	4.3	6.7	6.7	ns
t_{FDWS}	FPGA Write Data Valid to On-chip SRAM Data Valid	1.3	1.7	2.0	1.3	1.7	2.0	ns
t_{FDRS}	On-chip SRAM Data Valid to FPGA Read Data Valid	0.2	0.2	0.2	0.2	0.2	0.2	ns

Note: 1. Insertion delays are specified from XTAL2. These delays are more meaningful because the XTAL1-to-XTAL2 delay is sensitive to system loading on XTAL2. If it is necessary to drive external devices with the system clock, devices should use XTAL2 output pin. Remember that XTAL2 is inverted in comparison to XTAL1.

External Clock Drive Waveforms

Figure 85. External Clock Drive Waveforms

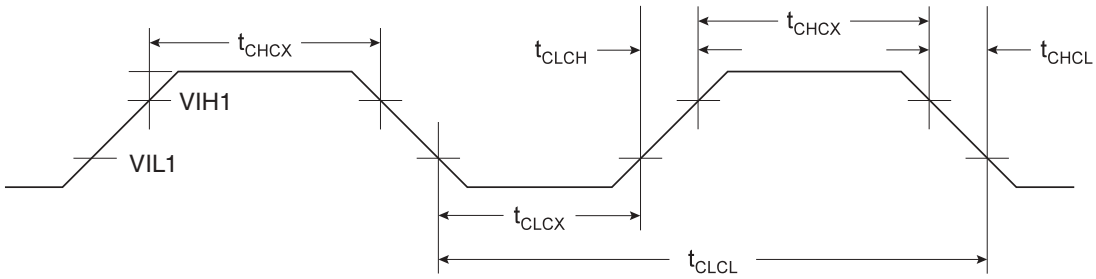


Table 53. External Clock Drive, V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Minimum	Maximum	Units
$1/t_{CLCL}$	Oscillator Frequency	0	25	MHz
t_{CLCL}	Clock Period	40	–	ns
t_{CHCX}	High Time	15	–	ns
t_{CLCX}	Low Time	15	–	ns
t_{CLCH}	Rise Time	–	1.6	µs
t_{CHCL}	Fall Time	–	1.6	µs

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-25	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	E -> E	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	L -> L	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	E -> L	2.2	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	E -> IO	1.4	ns	1 Unit Load
Repeater	t_{PD} (Maximum)	L -> IO	1.4	ns	1 Unit Load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-25	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.9	ns	No Extra Delay
Input	t_{PD} (Maximum)	pad -> x/y	5.8	ns	1 Extra Delay
Input	t_{PD} (Maximum)	pad -> x/y	11.5	ns	2 Extra Delays
Input	t_{PD} (Maximum)	pad -> x/y	17.4	ns	3 Extra Delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	9.1	ns	50 pf Load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	7.6	ns	50 pf Load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	6.2	ns	50 pf Load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	9.5	ns	50 pf Load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	2.1	ns	50 pf Load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	7.4	ns	50 pf Load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	2.7	ns	50 pf Load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	5.9	ns	50 pf Load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	2.4	ns	50 pf Load

Packaging and Pin List Information

FPSLIC devices should be laid out to support a split power supply for both AL and AX families. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note, available on the Atmel web site.

Table 54. Part and Package Combinations Available

Part #	Package	AT94K05	AT94K10	AT94K40
PLCC 84	AJ	46	46	
TQ 100	AQ	58	58	
LQ144	BQ	82	84	84
PQ 208	DQ	96	116	120

Table 55. AT94K JTAG ICE Pin List

Pin	AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O
TDI	IO34	IO50	IO98
TDO	IO38	IO54	IO102
TMS	IO43	IO63	IO123
TCK	IO44	IO64	IO124

Table 56. AT94K Pin List

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
West Side						
GND	GND	GND	12	1	1	2
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	2	2	4
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	3	3	5
I/O3	I/O3	I/O3			4	6
I/O4	I/O4	I/O4			5	7
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	4	6	8
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	5	7	9
		GND				
		I/O7				
		I/O8				
		I/O9				

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.

Table 56. AT94K Pin List (Continued)

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
		I/O64				
		I/O65				
		I/O66				
		GND				
	I/O31	I/O67				
	I/O32	I/O68				
	VDD(2)	VDD(2)				
I/O21 (A26)	I/O33 (A26)	I/O69 (A26)	25	16	23	33
I/O22 (A27)	I/O34 (A27)	I/O70 (A27)	26	17	24	34
I/O23	I/O35	I/O71			25	35
I/O24, FCK2	I/O36, FCK2	I/O72, FCK2			26	36
GND	GND	GND			27	37
		I/O73				
		I/O74				
	I/O37	I/O75				
	I/O38	I/O76				
		I/O77				
		I/O78				
		GND				
		I/O79				
		I/O80				
	I/O39	I/O81				38
	I/O40	I/O82				39
I/O25	I/O41	I/O83				40
I/O26	I/O42	I/O84				41
		GND				
		VCC(1)				
		I/O85				
		I/O86				
		I/O87				
		I/O88				
I/O27 (A28)	I/O43 (A28)	I/O89 (A28)	27	18	28	42
I/O28	I/O44	I/O90		19	29	43
		GND				

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.

Table 56. AT94K Pin List (Continued)

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
		GND				
		VCC(1)				
		I/O373				
		I/O374				
		I/O375				
		I/O376				
		I/O377				
		I/O378				
		GND				
	I/O187	I/O379				
	I/O188	I/O380				
I/O125	I/O189	I/O381			140	201
I/O126	I/O190	I/O382			141	202
I/O127 (A14)	I/O191 (A14)	I/O383 (A14)	9	98	142	203
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O384, GCK8 (A15)	10	99	143	204
VCC(1)	VCC(1)	VCC(1)	11	100	144	205

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.