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Embedded - FPGAs (Field Programmable Gate Arrays) with Microcontrollers represent a cutting-edge category of electronic components that combine the flexibility of FPGA technology with the processing power of integrated microcontrollers. This hybrid approach offers a versatile solution for designing and implementing complex digital systems that require both programmable logic and embedded processing capabilities.

What Are Embedded - FPGAs with Microcontrollers?

At their core, **FPGAs** are semiconductor devices that can

Details	
Product Status	Obsolete
Core Type	8-Bit AVR
Speed	25 MHz
Interface	I²C, UART
Program SRAM Bytes	20K-32K
FPGA SRAM	4kb
EEPROM Size	-
Data SRAM Bytes	4K ~ 16K
FPGA Core Cells	576
FPGA Gates	10K
FPGA Registers	846
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at94k10al-25aqc

FPGA/AVR Interface and System Control

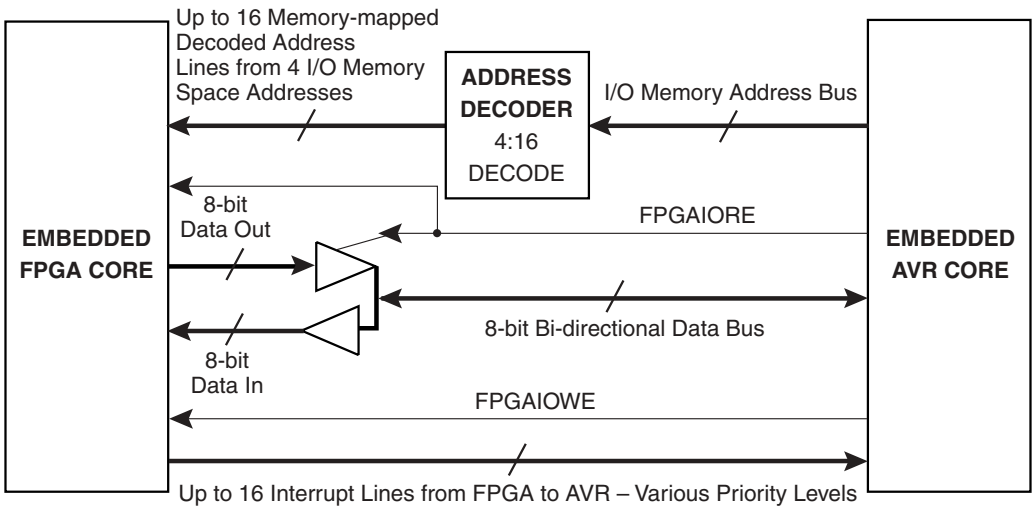
The FPGA and AVR share a flexible interface which allows for many methods of system integration.

- Both FPGA and AVR share access to the 15 ns dual-port SRAM.
- The AVR data bus interfaces directly into the FPGA busing resources, effectively treating the FPGA as a large I/O device. Users have complete flexibility on the types of additional peripherals which are placed and routed inside the FPGA user logic.
- Up to 16 decoded address lines are provided into the FPGA.
- Up to 16 interrupts are available from the FPGA to the AVR.
- The AVR can reprogram the FPGA during operation to create a dynamic reconfigurable system (Cache Logic).

FPGA/AVR Interface– Memory-mapped Peripherals

The FPGA core can be directly accessed by the AVR core, see Figure 18. Four memory locations in the AVR memory map are decoded into 16 select lines (8 for AT94K05) and are presented to the FPGA along with the AVR 8-bit data bus. The FPGA can be used to create additional custom peripherals for the AVR microcontroller through this interface. In addition there are 16 interrupt lines (8 for AT94K05) from the FPGA back into the AVR interrupt controller. Programmable peripherals or regular logic can use these interrupt lines. Full support for programmable peripherals is available within the System Designer tool suite.

Figure 18. FPGA/AVR Interface: Interrupts and Addressing



The FPGA I/O selection is controlled by the AVR. This is described in detail beginning on page 53. The FPGA I/O interrupts are described beginning on page 57.

Table 11. FPSLIC System Control Register

Bit	Description
SCR6	0 = OTS Disabled 1 = OTS Enabled Setting SCR6 makes the OTS (output tri-state) pin an input which controls the global tri-state control for all user I/O. This junction allows the user at any time to tristate all user I/O and isolate the chip.
SCR7 - SCR12	Reserved
SCR13	0 = CCLK Normal Operation 1 = CCLK Continues After Configuration. Setting bit SCR13 allows the CCLK pin to continue to run after configuration download is completed. This bit is valid for Master mode, mode 0 only. The CCLK is not available internally on the device. If it is required in the design, it must be connected to another device I/O.
SCR14 - SCR15	Reserved
SCR16 - SCR23	0 = GCK 0:7 Always Enabled 1 = GCK 0:7 Disabled During Internal and External Configuration Download. Setting SCR16:SCR23 allows the user to disable the input buffers driving the global clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective GCK signal, and stop in a High “1” state. Setting one of these bits disables the appropriate GCK input buffer only and has no effect on the connection from the input buffer to the FPGA array.
SCR24 - SCR25	0 = FCK 0:1 Always Enabled 1 = FCK 0:1 Disabled During Internal and External Configuration Download. Setting SCR24:SCR25 allows the user to disable the input buffers driving the fast clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective FCK signal, and stop in a High “1” state. Setting one of these bits disables the appropriate FCK input buffer only and has no effect on the connection from the input buffer to the FPGA array.
SCR26	0 = Disable On-chip Debugger 1 = Enable On-chip Debugger. JTAG Enable, SCR27, must also be set (one) and the configuration memory lockout, SCR4, must be clear (zero) for the user to have access to internal scan chains.
SCR27	0 = Disable TAP at user FPGA I/O Ports 1 = Enable TAP at user FPGA I/O Ports. Device ID scan chain and AVR I/O boundary scan chain are available. The user must set (one) the On-chip Debug Enable, SCR26, and must keep the configuration memory lockout, SCR4, clear (zero) for the user to have access to internal scan chains.
SCR28 - SCR29	Reserved
SCR30	0 = Global Set/Reset Normal 1 = Global Set/Reset Active (Low) During Internal and External Configuration Download. SCR30 allows the Global set/reset to hold the core DFFs in reset during any configuration download. The Global set/reset net is released at the end of configuration download on the rising edge of CON, if set.
SCR31	0 = Disable I/O Tri-state 1 = I/O Tri-state During (Internal and External) Configuration Download. SCR31 forces all user defined I/O pins to go tri-state during configuration download. Tri-state is released at the end of configuration download on the rising edge of CON, if set.

Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clock
CLS		Clear Signed Test Flag	S 0	S	1
SEV		Set Two's Complement Overflow	V 1	V	1
CLV		Clear Two's Complement Overflow	V 0	V	1
SET		Set T in SREG	T 1	T	1
CLT		Clear T in SREG	T 0	T	1
SEH		Set Half-carry Flag in SREG	H 1	H	1
CLH		Clear Half-carry Flag in SREG	H 0	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(See specific description for Sleep)	None	1
WDR		Watchdog Reset	(See specific description for WDR)	None	1
BREAK		Break	For on-chip debug only	None	N/A

Pin Descriptions

V_{CC} Supply voltage

GND Ground

PortD (PD7..PD0) Port D is an 8-bit bi-directional I/O port with internal programmable pull-up resistors. The Port D output buffers can be programmed to sink/source either 6 or 20 mA (SCR54 – see "System Control Register – FPGA/AVR" on page 30). As inputs, Port D pins that are externally pulled Low will source current if the programmable pull-up resistors are activated.

The Port D pins are input with pull-up when a reset condition becomes active, even if the clock is not running. On lower pin count packages Port D may not be available. Check the Pin List for details.

PortE (PE7..PE0) Port E is an 8-bit bi-directional I/O port with internal programmable pull-up resistors. The Port E output buffers can be programmed to sink/source either 6 or 20 mA (SCR55 – see "System Control Register – FPGA/AVR" on page 30). As inputs, Port E pins that are externally pulled Low will source current if the pull-up resistors are activated.

Port E also serves the functions of various special features. See Table 47 on page 149.

The Port E pins are input with pull-up when a reset condition becomes active, even if the clock is not running

RX0 Input (receive) to UART(0) – See SCR52

TX0 Output (transmit) from UART(0) – See SCR52

RX1 Input (receive) to UART(1) – See SCR53

TX1 Output (transmit) from UART(1) – See SCR53

XTAL1 Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2 Output from the inverting oscillator amplifier

TOSC1 Input to the inverting timer/counter oscillator amplifier

TOSC2 Output from the inverting timer/counter oscillator amplifier

SCL 2-wire serial input/output clock

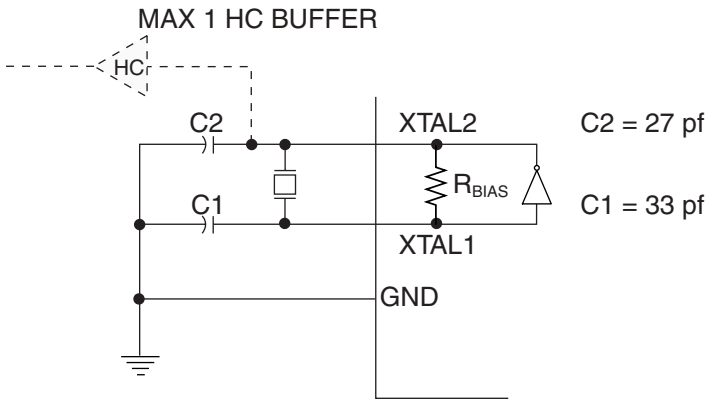
SDA 2-wire serial input/output data

Clock Options

Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier, which can be configured for use as an on-chip oscillator, as shown in Figure 24. Either a quartz crystal or a ceramic resonator may be used.

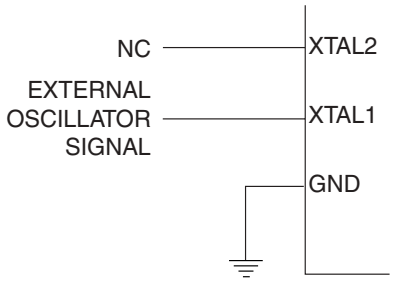
Figure 24. Oscillator Connections



External Clock

To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 25.

Figure 25. External Clock Drive Configuration



AT94K Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
$16 ($36)	FISUC	FPGA I/O Select, Interrupt Mask/Flag Register C (Reserved on AT94K05)								54, 56
$15 ($35)	FISUB	FPGA I/O Select, Interrupt Mask/Flag Register B								54, 56
$14 ($34)	FISUA	FPGA I/O Select, Interrupt Mask/Flag Register A								54, 56
$13 ($33)	FISCR	FIADR						XFIS1	XFIS0	53
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	124
$11 ($31)	DDRD	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0	124
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	124
$0F ($2F)	Reserved									
$0E ($2E)	Reserved									
$0D ($2D)	Reserved									
$0C ($2C)	UDR0	UART0 I/O Data Register								101
$0B ($2B)	UCSR0A	RXC0	TXC0	UDRE0	FE0	OR0		U2X0	MPCM0	101
$0A ($2A)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	CHR90	RXB80	TXB80	103
$09 ($29)	UBRR0	UART0 Baud-rate Register								105
$08 ($28)	OCDR (Reserved)	IDRD								Reserved[1]
$07 ($27)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	126
$06 ($26)	DDRE	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	DDRE1	DDRE0	126
$05 ($25)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	126
$04 ($24)	Reserved									
$03 ($23)	UDR1	UART1 I/O Data Register								101
$02 ($22)	UCSR1A	RXC1	TXC1	UDRE1	FE1	OR1		U2X1	MPCM1	101
$01 ($21)	UCSR1B	RXCIE1	TXCIE1	UDRIE1	RXEN1	TXEN1	CHR91	RXB81	TXB81	103
$00 ($20)	UBRR1	UART1 Baud-rate Register								105

Note: 1. The On-chip Debug Register (OCDR) is detailed on the “FPSLIC On-chip Debug System” distributed within Atmel and select third-party vendors only under Non-Disclosure Agreement (NDA). Contact fpslic@atmel.com for a copy of this document.

The embedded AVR core I/Os and peripherals, and all the virtual FPGA peripherals are placed in the I/O space. The different I/O locations are directly accessed by the IN and OUT instructions transferring data between the 32 x 8 general-purpose working registers and the I/O space. I/O registers within the address range $00 – $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. When using the I/O specific instructions IN, OUT, the I/O register address $00 – $3F are used, see Figure 32. When addressing I/O registers as SRAM, $20 must be added to this address. All I/O register addresses throughout this document are shown with the SRAM address in parentheses.

Watchdog Timer Control Register – WDTCR

Bit	7	6	5	4	3	2	1	0	
$21 ($41)	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- Bits 7..5 - Res: Reserved Bits

These bits are reserved bits in the FPSLIC and will always read as zero.

- Bit 4 - WDTOE: Watchdog Turn-off Enable

This bit must be set (one) when the WDE bit is cleared. Otherwise, the watchdog will not be disabled. Once set, the hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit below for a watchdog disable procedure.

- Bit 3 - WDE: Watchdog Enable

When the WDE is set (one) the Watchdog Timer is enabled, but if the WDE is cleared (zero), the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit is set (one). To disable an enabled Watchdog Timer, the following procedure must be followed:

1. In the same operation, write a logic 1 to WDTOE and WDE. A logic 1 must be written to WDE even though it is set to one before the disable operation starts.
2. Within the next four clock cycles, write a logic 0 to WDE. This disables the watchdog.

- Bits 2..0 - WDP2, WDP1, WDP0: Watchdog Timer Prescaler 2, 1 and 0

The WDP2, WDP1 and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding Time-out periods are shown in Table 33.

Table 33. Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles (1)	Typical Time-out at V_{CC} = 3.0V
0	0	0	16K	15 ms
0	0	1	32K	30 ms
0	1	0	64K	60 ms
0	1	1	128K	0.12s
1	0	0	256K	0.24s
1	0	1	512K	0.49s
1	1	0	1,024K	0.97s
1	1	1	2,048K	1.9s

Note: 1. The frequency of the watchdog oscillator is voltage dependent as shown in the Electrical Characteristics section. The WDR (watchdog reset) instruction should always be executed before the Watchdog Timer is enabled. This ensures that the reset period will be in accordance with the Watchdog Timer prescale settings. If the Watchdog Timer is enabled without reset, the Watchdog Timer may not start counting from zero.

fmuls16x16_32

Description

Signed fractional multiply of two 16-bit numbers with a 32-bit result.

Usage

R19:R18:R17:R16 = (R23:R22 • R21:R20) << 1

Statistics

Cycles: 20 + ret

Words: 16 + ret

Register usage: R0 to R2 and R16 to R23 (11 registers)(1)

Note: 1. The routine is non-destructive to the operands.

```
fmuls16x16_32:
   clr   r2
   fmuls r23, r21             ; ( (signed)ah * (signed)bh ) << 1
   movw  r19:r18, r1:r0
   fmul  r22, r20             ; ( al * bl ) << 1
   adc   r18, r2
   movw  r17:r16, r1:r0
   fmulsu   r23, r20          ; ( (signed)ah * bl ) << 1
   sbc   r19, r2              ; Sign extend
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   fmulsu   r21, r22          ; ( (signed)bh * al ) << 1
   sbc   r19, r2              ; Sign extend
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   ret
```

fmac16x16_32

Description

Signed fractional multiply-accumulate of two 16-bit numbers with a 32-bit result.

Usage

R19:R18:R17:R16 += (R23:R22 • R21:R20) << 1

Statistics

Cycles: 25 + ret

Words: 21 + ret

Register usage: R0 to R2 and R16 to R23 (11 registers)

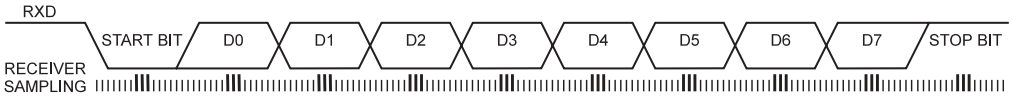
```
fmac16x16_32:                 ; Register usage optimized
   clr   r2

   fmuls r23, r21             ; ( (signed)ah * (signed)bh ) << 1
   add   r18, r0
   adc   r19, r1

   fmul  r22, r20             ; ( al * bl ) << 1
   adc   r18, r2
   adc   r19, r2
   add   r16, r0
```

If however, a valid start bit is detected, sampling of the data bits following the start bit is performed. These bits are also sampled at samples 8, 9 and 10. The logical value found in at least two of the three samples is taken as the bit value. All bits are shifted into the transmitter shift register as they are sampled. Sampling of an incoming character is shown in Figure 66. Note that the description above is not valid when the UART transmission speed is doubled. See “Double Speed Transmission” on page 128 for a detailed description.

Figure 66. Sampling Received Data(1)



Note: 1. This figure is not valid when the UART speed is doubled. See “Double Speed Transmission” on page 128 for a detailed description.

When the stop bit enters the receiver, the majority of the three samples must be one to accept the stop bit. If two or more samples are logic 0s, the Framing Error (FEn) flag in the UART Control and Status Register (UCSRnA) is set. Before reading the UDRn register, the user should always check the FEn bit to detect Framing Errors.

Whether or not a valid stop bit is detected at the end of a character reception cycle, the data is transferred to UDRn and the RXCn flag in UCSRnA is set. UDRn is in fact two physically separate registers, one for transmitted data and one for received data. When UDRn is read, the Receive Data register is accessed, and when UDRn is written, the Transmit Data register is accessed. If the 9-bit data word is selected (the CHR9n bit in the UART Control and Status Register, UCSRnB is set), the RXB8n bit in UCSRnB is loaded with bit 9 in the Transmit shift register when data is transferred to UDRn.

If, after having received a character, the UDRn register has not been read since the last receive, the OverRun (ORn) flag in UCSRnB is set. This means that the last data byte shifted into to the shift register could not be transferred to UDRn and has been lost. The ORn bit is buffered, and is updated when the valid data byte in UDRn is read. Thus, the user should always check the ORn bit after reading the UDRn register in order to detect any overruns if the baud-rate is High or CPU load is High.

When the RXEN bit in the UCSRnB register is cleared (zero), the receiver is disabled. This means that the PE1 (n=0) or PE3 (n=1) pin can be used as a general I/O pin. When $RXEN_n$ is set, the UART Receiver will be connected to PE1 (UART0) or PE3 (UART1), which is forced to be an input pin regardless of the setting of the DDE1 in DDRE (UART0) or DDB2 bit in DDRB (UART1). When PE1 (UART0) or PE3 (UART1) is forced to input by the UART, the PORTE1 (UART0) or PORTE3 (UART1) bit can still be used to control the pull-up resistor on the pin.

When the CHR9n bit in the UCSRnB register is set, transmitted and received characters are 9 bits long plus start and stop bits. The 9th data bit to be transmitted is the TXB8n bit in UCSRnB register. This bit must be set to the wanted value before a transmission is initiated by writing to the UDRn register. The 9th data bit received is the RXB8n bit in the UCSRnB register.

Table 44. Status Codes for Slave Transmitter Mode

Status Code (TWSR)	Status of the 2-wire Serial Bus and 2-wire Serial Hardware	Application Software Response					Next Action Taken by 2-wire Serial Hardware
		To/From TWDR	To TWCR				
			STA	STO	TWINT	TWEA	
$A8	Own SLA+R has been received; ACK has been returned	Load data byte or	X	0	1	0	Last data byte will be transmitted and NOT ACK should be received
		Load data byte	X	0	1	1	Data byte will be transmitted and ACK should be received
$B0	Arbitration lost in SLA+R/W as Master; own SLA+R has been received; ACK has been returned	Load data byte or	X	0	1	0	Last data byte will be transmitted and NOT ACK should be received
		Load data byte	X	0	1	1	Data byte will be transmitted and ACK should be received
$B8	Data byte in TWDR has been transmitted; ACK has been received	Load data byte or	X	0	1	0	Last data byte will be transmitted and NOT ACK should be received
		Load data byte	X	0	1	1	Data byte will be transmitted and ACK should be received
$C0	Data byte in TWDR has been transmitted; NOT ACK has been received	No TWDR action or	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		No TWDR action or	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”
		No TWDR action or	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		No TWDR action	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”; a START condition will be transmitted when the bus becomes free
$C8	Last data byte in TWDR has been transmitted (TWAE = “0”); ACK has been received	No TWDR action or	0	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA
		No TWDR action or	0	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”
		No TWDR action or	1	0	1	0	Switched to the not addressed Slave mode; no recognition of own SLA or GCA; a START condition will be transmitted when the bus becomes free
		No TWDR action	1	0	1	1	Switched to the not addressed Slave mode; own SLA will be recognized; GCA will be recognized if GC = “1”; a START condition will be transmitted when the bus becomes free

Alternate I/O Functions of PortE

PortE may also be used for various Timer/Counter functions, such as External Input Clocks (TC0 and TC1), Input Capture (TC1), Pulse Width Modulation (TC0, TC1 and TC2), and toggling upon an Output Compare (TC0, TC1 and TC2). For a detailed pinout description, consult Table 47 on page 149. For more information on the function of each pin, See “Timer/Counters” on page 85.

PortE Schematics

Note that all port pins are synchronized. The synchronization latches are, however, not shown in the figures.

Figure 76. PortE Schematic Diagram (Pin PE0)

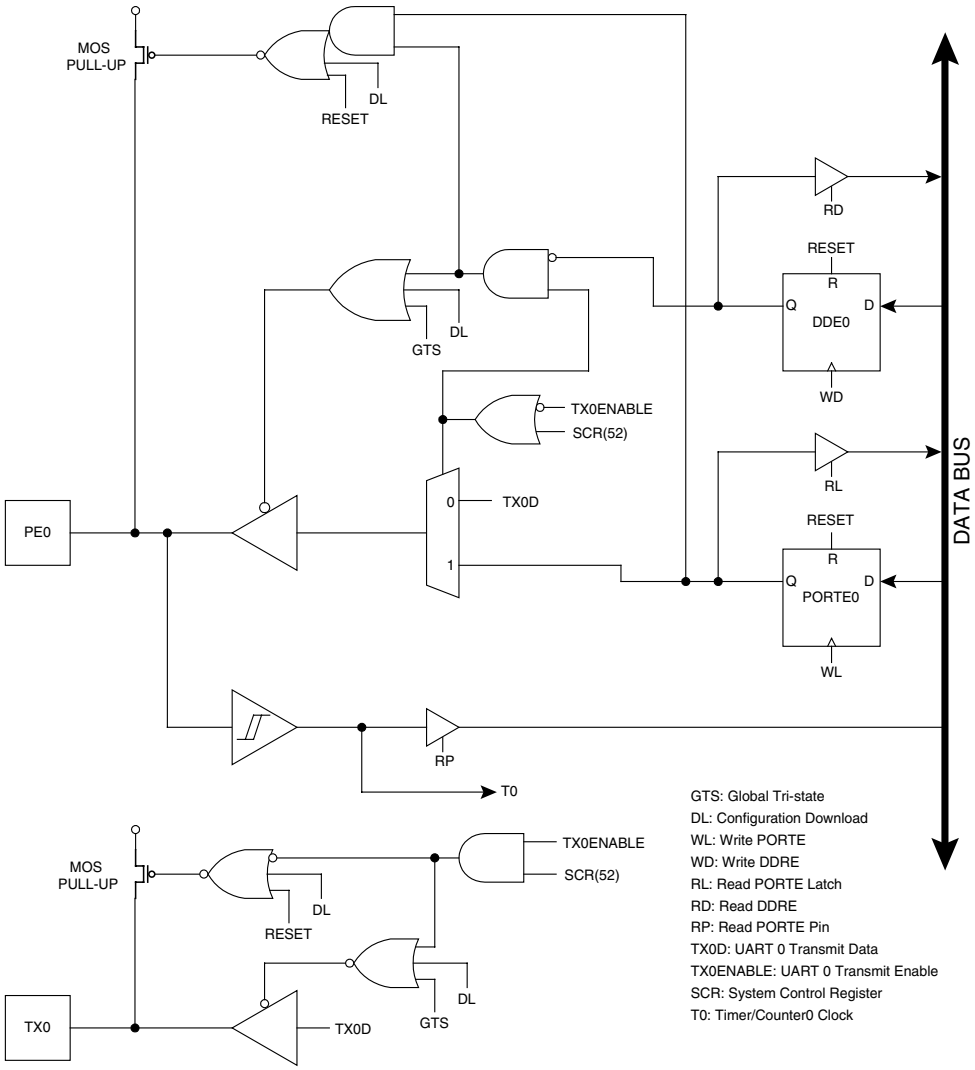


Table 52. FPSLIC Interface Timing Information[1]

Symbol	Parameter	3.3V Commercial ± 10%			3.3V Industrial ± 10%			Units
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
t_{IXG4}	Clock Delay From XTAL2 Pad to GCK_5 Access to FPGA Core	3.6	4.8	7.6	3.4	4.8	7.9	ns
t_{IXG5}	Clock Delay From XTAL2 Pad to GCK_6 Access to FPGA Core	3.9	5.2	8.1	3.6	5.2	8.8	ns
t_{IXC}	Clock Delay From XTAL2 Pad to AVR Core Clock	2.8	3.7	6.3	2.5	3.7	6.9	ns
t_{IXI}	Clock Delay From XTAL2 Pad to AVR I/O Clock	3.5	4.7	7.5	3.2	4.7	7.8	ns
t_{CFIR}	AVR Core Clock to FPGA I/O Read Enable	5.3	6.6	7.9	4.4	6.6	9.2	ns
t_{CFIW}	AVR Core Clock to FPGA I/O Write Enable	5.2	6.6	7.9	4.4	6.6	9.2	ns
t_{CFIS}	AVR Core Clock to FPGA I/O Select Active	6.3	7.8	9.4	5.3	7.8	11.0	ns
t_{FIRQ}	FPGA Interrupt Net Propagation Delay to AVR Core	0.2	0.2	0.3	0.1	0.2	0.3	ns
t_{IFS}	FPGA SRAM Clock to On-chip SRAM	6.1	7.7	7.7	4.9	7.7	7.7	ns
t_{FRWS}	FPGA SRAM Write Stobe to On-chip SRAM	4.4	5.5	5.5	3.7	5.5	5.5	ns
t_{FAS}	FPGA SRAM Address Valid to On-chip SRAM Address Valid	5.4	6.7	6.7	4.3	6.7	6.7	ns
t_{FDWS}	FPGA Write Data Valid to On-chip SRAM Data Valid	1.3	1.7	2.0	1.3	1.7	2.0	ns
t_{FDRS}	On-chip SRAM Data Valid to FPGA Read Data Valid	0.2	0.2	0.2	0.2	0.2	0.2	ns

Note: 1. Insertion delays are specified from XTAL2. These delays are more meaningful because the XTAL1-to-XTAL2 delay is sensitive to system loading on XTAL2. If it is necessary to drive external devices with the system clock, devices should use XTAL2 output pin. Remember that XTAL2 is inverted in comparison to XTAL1.

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-25	Units	Notes
Core					
2 Input Gate	t_{PD} (Maximum)	x/y -> x/y	2.9	ns	1 Unit Load
3 Input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.8	ns	1 Unit Load
3 Input Gate	t_{PD} (Maximum)	x/y/w -> x/y	3.4	ns	1 Unit Load
4 Input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	y -> y	2.3	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	x -> y	2.9	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	y -> x	3.0	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	x -> x	2.3	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	w -> y	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	w -> x	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	z -> y	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	z -> x	2.4	ns	1 Unit Load
DFF	t_{PD} (Maximum)	q -> x/y	2.8	ns	1 Unit Load
DFF	t_{setup} (Minimum)	x/y -> clk	–	–	–
DFF	t_{hold} (Minimum)	x/y -> clk	–	–	–
DFF	t_{PD} (Maximum)	R -> x/y	3.2	ns	1 Unit Load
DFF	t_{PD} (Maximum)	S -> x/y	3.0	ns	1 Unit Load
DFF	t_{PD} (Maximum)	q -> w	2.7	ns	–
incremental -> L	t_{PD} (Maximum)	x/y -> L	2.4	ns	–
Local Output Enable	t_{PZX} (Maximum)	oe -> L	2.8	ns	1 Unit Load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	2.4	ns	

Packaging and Pin List Information

FPSLIC devices should be laid out to support a split power supply for both AL and AX families. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note, available on the Atmel web site.

Table 54. Part and Package Combinations Available

Part #	Package	AT94K05	AT94K10	AT94K40
PLCC 84	AJ	46	46	
TQ 100	AQ	58	58	
LQ144	BQ	82	84	84
PQ 208	DQ	96	116	120

Table 55. AT94K JTAG ICE Pin List

Pin	AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O
TDI	IO34	IO50	IO98
TDO	IO38	IO54	IO102
TMS	IO43	IO63	IO123
TCK	IO44	IO64	IO124

Table 56. AT94K Pin List

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
West Side						
GND	GND	GND	12	1	1	2
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	2	2	4
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	3	3	5
I/O3	I/O3	I/O3			4	6
I/O4	I/O4	I/O4			5	7
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	4	6	8
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	5	7	9
		GND				
		I/O7				
		I/O8				
		I/O9				

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.

Table 56. AT94K Pin List (Continued)

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
I/O100	I/O148	I/O292			114	164
		I/O293				
		I/O294				
		GND				
		I/O295				
		I/O296				
I/O101 ($\overline{CS1}$, A2)	I/O149 ($\overline{CS1}$, A2)	I/O297 ($\overline{CS1}$, A2)	79	80	115	165
I/O102 (A3)	I/O150 (A3)	I/O298 (A3)	80	81	116	166
		I/O299				
		I/O300				
		VCC[1]				
		GND				
I/O104	I/O151	I/O301	Shorted to Testclock	Shorted to Testclock	Shorted to Testclock	Shorted to Testclock
	I/O152	I/O302				
I/O103	I/O153	I/O303			117	167
	I/O154	I/O304				168
		I/O305				
		I/O306				
		GND				
		I/O307				
		I/O308				
	I/O155	I/O309				169
	I/O156	I/O310				170
		I/O311				
		I/O312				
GND	GND	GND			118	171
I/O105	I/O157	I/O313			119	172
I/O106	I/O158	I/O314			120	173
	I/O159	I/O315				
	I/O160	I/O316				
	VCC[1]	VCC[1]				
		I/O317				
		I/O318				

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.