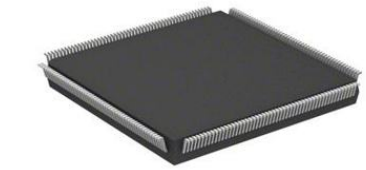

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Details	
Product Status	Obsolete
Core Type	8-Bit AVR
Speed	25 MHz
Interface	I²C, UART
Program SRAM Bytes	20K-32K
FPGA SRAM	4kb
EEPROM Size	-
Data SRAM Bytes	4K ~ 16K
FPGA Core Cells	576
FPGA Gates	10K
FPGA Registers	846
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at94k10al-25dqi

Figure 4. Busing Plane (One of Five)

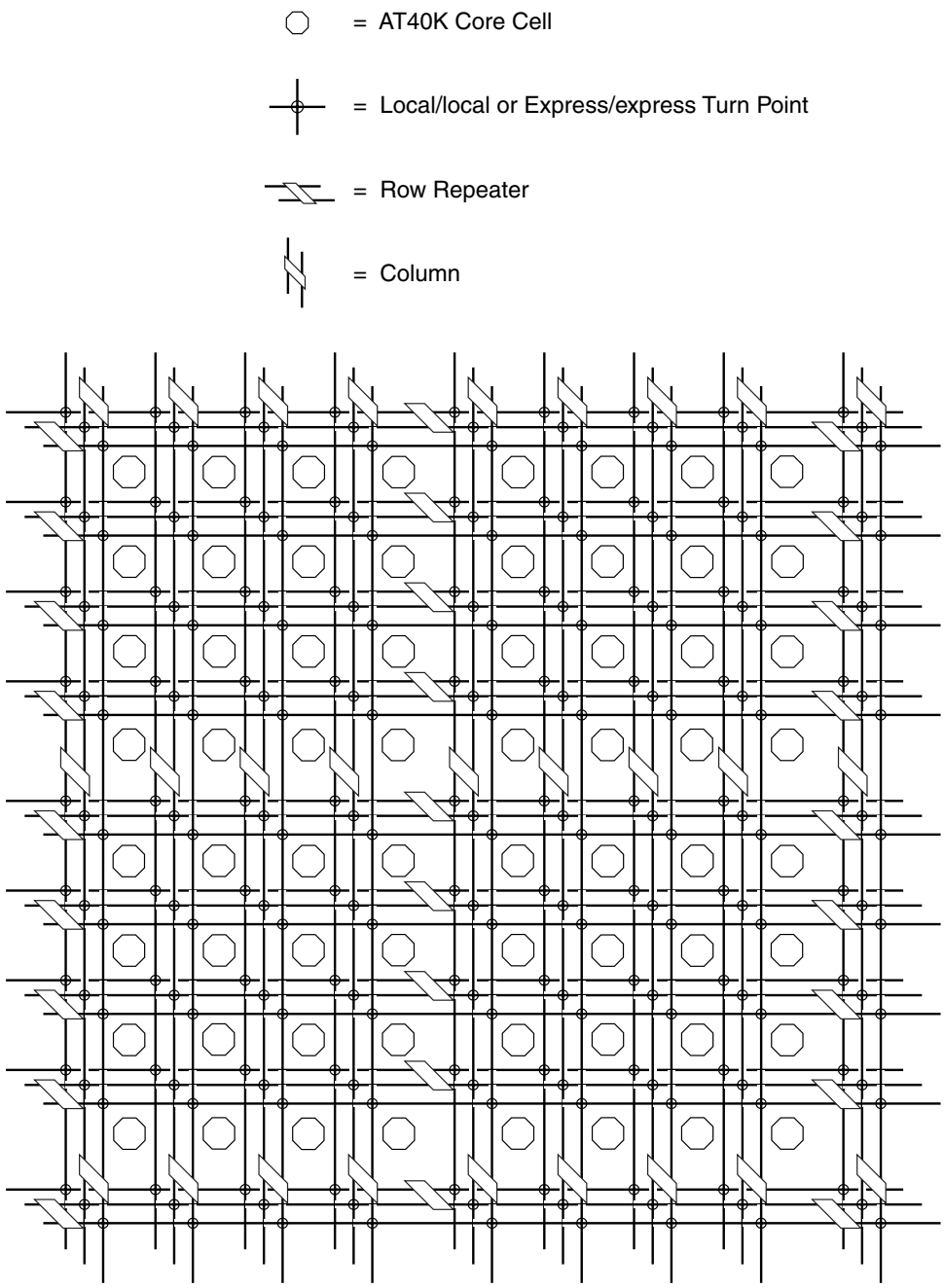


Table 11. FPSLIC System Control Register

Bit	Description
SCR6	0 = OTS Disabled 1 = OTS Enabled Setting SCR6 makes the OTS (output tri-state) pin an input which controls the global tri-state control for all user I/O. This junction allows the user at any time to tristate all user I/O and isolate the chip.
SCR7 - SCR12	Reserved
SCR13	0 = CCLK Normal Operation 1 = CCLK Continues After Configuration. Setting bit SCR13 allows the CCLK pin to continue to run after configuration download is completed. This bit is valid for Master mode, mode 0 only. The CCLK is not available internally on the device. If it is required in the design, it must be connected to another device I/O.
SCR14 - SCR15	Reserved
SCR16 - SCR23	0 = GCK 0:7 Always Enabled 1 = GCK 0:7 Disabled During Internal and External Configuration Download. Setting SCR16:SCR23 allows the user to disable the input buffers driving the global clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective GCK signal, and stop in a High “1” state. Setting one of these bits disables the appropriate GCK input buffer only and has no effect on the connection from the input buffer to the FPGA array.
SCR24 - SCR25	0 = FCK 0:1 Always Enabled 1 = FCK 0:1 Disabled During Internal and External Configuration Download. Setting SCR24:SCR25 allows the user to disable the input buffers driving the fast clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective FCK signal, and stop in a High “1” state. Setting one of these bits disables the appropriate FCK input buffer only and has no effect on the connection from the input buffer to the FPGA array.
SCR26	0 = Disable On-chip Debugger 1 = Enable On-chip Debugger. JTAG Enable, SCR27, must also be set (one) and the configuration memory lockout, SCR4, must be clear (zero) for the user to have access to internal scan chains.
SCR27	0 = Disable TAP at user FPGA I/O Ports 1 = Enable TAP at user FPGA I/O Ports. Device ID scan chain and AVR I/O boundary scan chain are available. The user must set (one) the On-chip Debug Enable, SCR26, and must keep the configuration memory lockout, SCR4, clear (zero) for the user to have access to internal scan chains.
SCR28 - SCR29	Reserved
SCR30	0 = Global Set/Reset Normal 1 = Global Set/Reset Active (Low) During Internal and External Configuration Download. SCR30 allows the Global set/reset to hold the core DFFs in reset during any configuration download. The Global set/reset net is released at the end of configuration download on the rising edge of CON, if set.
SCR31	0 = Disable I/O Tri-state 1 = I/O Tri-state During (Internal and External) Configuration Download. SCR31 forces all user defined I/O pins to go tri-state during configuration download. Tri-state is released at the end of configuration download on the rising edge of CON, if set.

Conditional Branch Summary

Test	Boolean	Mnemonic	Complementary	Boolean	Mnemonic	Comment
Rd > Rr	Z•(N ⊕ V) = 0	BRLT	Rd ≤ Rr	Z+(N ⊕ V) = 1	BRGE	Signed
Rd ≥ Rr	(N ⊕ V) = 0	BRGE	Rd < Rr	(N ⊕ V) = 1	BRLT	Signed
Rd = Rr	Z = 1	BREQ	Rd ≠ Rr	Z = 0	BRNE	Signed
Rd ≤ Rr	Z+(N ⊕ V) = 1	BRGE	Rd > Rr	Z•(N ⊕ V) = 0	BRLT	Signed
Rd < Rr	(N ⊕ V) = 1	BRLT	Rd ≥ Rr	(N ⊕ V) = 0	BRGE	Signed
Rd > Rr	C + Z = 0	BRLO	Rd ≤ Rr	C + Z = 1	BRSH	Unsigned
Rd ≥ Rr	C = 0	BRSH/BRCC	Rd < Rr	C = 1	BRLO/BRCS	Unsigned
Rd = Rr	Z = 1	BREQ	Rd ≠ Rr	Z = 0	BRNE	Unsigned
Rd ≤ Rr	C + Z = 1	BRSH	Rd > Rr	C + Z = 0	BRLO	Unsigned
Rd < Rr	C = 1	BRLO/BRCS	Rd ≥ Rr	C = 0	BRSH/BRCC	Unsigned
Carry	C = 1	BRCS	No Carry	C = 0	BRCC	Simple
Negative	N = 1	BRMI	Positive	N = 0	BRPL	Simple
Overflow	V = 1	BRVS	No Overflow	V = 0	BRVC	Simple
Zero	Z = 1	BREQ	Not Zero	Z = 0	BRNE	Simple

Complete Instruction Set Summary

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clock
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd+1:Rd ← Rd+1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd+1:Rd ← Rd+1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One's Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two's Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd, K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1

External Interrupt Mask/Flag Register – EIMF

Bit	7	6	5	4	3	2	1	0	
$3B ($5B)	INTF3	INTF2	INTF1	INTF0	INT3	INT2	INT1	INT0	EIMF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 3..0 - INT3, 2, 1, 0: External Interrupt Request 3, 2, 1, 0 Enable**

When an INT3 - INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the corresponding external pin interrupt is enabled. The external interrupts are always negative edge triggered interrupts, see “Sleep Modes” on page 66.

- **Bits 7..4 - INTF3, 2, 1, 0: External Interrupt 3, 2, 1, 0 Flags**

When a falling edge is detected on the INT3, 2, 1, 0 pins, an interrupt request is triggered. The corresponding interrupt flag, INTF3, 2, 1, 0 becomes set (one). If the I-bit in SREG and the corresponding interrupt enable bit, INT3, 2, 1, 0 in EIMF, are set (one), the MCU will jump to the interrupt vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag is cleared by writing a logic 1 to it.

Timer/Counter Interrupt Mask Register – TIMSK

Bit	7	6	5	4	3	2	1	0	
$39 ($39)	TOIE1	OCIE1A	OCIE1B	TOIE2	TICIE1	OCIE2	TOIE0	OCIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 - TOIE1: Timer/Counter1 Overflow Interrupt Enable**

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow interrupt is enabled. The corresponding interrupt is executed if an overflow in Timer/Counter1 occurs, i.e., when the TOV1 bit is set in the Timer/Counter Interrupt Flag Register – TIFR.

- **Bit 6 - OCIE1A: Timer/Counter1 Output CompareA Match Interrupt Enable**

When the OCIE1A bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 CompareA Match interrupt is enabled. The corresponding interrupt is executed if a CompareA match in Timer/Counter1 occurs, i.e., when the OCF1A bit is set in the Timer/Counter Interrupt Flag Register – TIFR.

- **Bit 5 - OCIE1B: Timer/Counter1 Output CompareB Match Interrupt Enable**

When the OCIE1B bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 CompareB Match interrupt is enabled. The corresponding interrupt is executed if a CompareB match in Timer/Counter1 occurs, i.e., when the OCF1B bit is set in the Timer/Counter Interrupt Flag Register – TIFR.

- **Bit 4 - TOIE2: Timer/Counter2 Overflow Interrupt Enable**

When the TOIE2 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter2 overflow interrupt is enabled. The corresponding interrupt is executed if an overflow in Timer/Counter2 occurs, i.e., when the TOV2 bit is set in the Timer/Counter interrupt flag register – TIFR.

- **Bit 3 - TICIE1: Timer/Counter1 Input Capture Interrupt Enable**

When the TICIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 input capture event interrupt is enabled. The corresponding interrupt is executed if a capture-triggering event occurs on pin 29, (IC1), i.e., when the ICF1 bit is set in the Timer/Counter interrupt flag register – TIFR.

Table 20. AVR I/O Boundary Scan – JTAG Instructions $0/$2

I/O Ports	Description	Bit	
XTAL	Clock In - XTAL1	8[1]	
	Enable Clock - XTAL 1	7	
TOSC	Clock In - TOSC 1	6[1]	
	Enable Clock - TOSC 1	5	
2-wire Serial	Data Out/In - SDA	4[1]	
	Enable Output - SDA	3	
	Clock Out/In - SCL	2[1]	
	Enable Output - SCL	1	
[2]	AVR Reset	0[1]	-> TDO

Notes: 1. Observe-only scan cell.
2. AVR Reset is High (one) if AVRResetn activated (Low) and enabled or the device is in general reset (Resetn or power-on) or configuration download.

Table 21. Bit EXTEST and SAMPLE_PRELOAD

Bit Type	EXTEST	SAMPLE_PRELOAD
Data Out/In - PXn	**Defines value driven if enabled**. Capture-DR grabs signal on pad.	Capture-DR grabs signal from pad if output disabled, or from the AVR if the output drive is enabled.
Enable Output - PXn	**1 = output drive enabled**. Capture-DR grabs output enable scan latch.	Capture-DR grabs output enable from the AVR.
Pull-up - PXn	**1 = pull-up disabled**. Capture-DR grabs pull-up control from the AVR.	Capture-DR grabs pull-up control from the AVR.
Input with Pull-up - INTPn	**Observe only**. Capture-DR grabs signal from pad.	Capture-DR grabs signal from pad.
Data Out - TXn	**Defines value driven if enabled**. Capture-DR grabs signal on pad.	Capture-DR always grabs “0” since Tx input is NC and tied to ground internally.
Enable Output - TXn	**1 = output drive enabled**. Capture-DR grabs output enable scan latch.	Capture-DR grabs output enable from the AVR.
Pull-up - TXn	**1 = pull-up disabled**. Capture-DR grabs pull-up control from the AVR.	Capture-DR grabs pull-up control from the AVR.
Input with Pull-up - RXn	**Observe only**. Capture-DR grabs signal from pad.	Capture-DR grabs signal from pad.
Clock In - XTAL1	**Observe only**. Capture-DR grabs signal from pad.	Capture-DR grabs signal from pad if clock is enabled, “1” if disabled.
Enable Clock - XTAL 1	**1 = clock disabled**. Capture-DR grabs clock enable from the AVR.	Capture-DR grabs enable from the AVR.

Table 24. Clock 2 Prescale Select

CS22	CS21	CS20	Description
0	0	0	Stop, the Timer/Counter2 is stopped
0	0	1	PCK2
0	1	0	PCK2/8
0	1	1	PCK2/32
1	0	0	PCK2/64
1	0	1	PCK2/128
1	1	0	PCK2/256
1	1	1	PCK2/1024

The Stop condition provides a Timer Enable/Disable function. The prescaled modes are scaled directly from the CK oscillator clock for Timer/Counter0 and PCK2 for Timer/Counter2. If the external pin modes are used for Timer/Counter0, transitions on PE0/(T0) will clock the counter even if the pin is configured as an output. This feature can give the user SW control of the counting.

Timer Counter0 – TCNT0

Bit	7	6	5	4	3	2	1	0	
$32 ($52)	MSB							LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Timer/Counter2 – TCNT2

Bit	7	6	5	4	3	2	1	0	
$23 ($43)	MSB							LSB	TCNT2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

These 8-bit registers contain the value of the Timer/Counters.

Both Timer/Counters are realized as up or up/down (in PWM mode) counters with read and write access. If the Timer/Counter is written to and a clock source is selected, it continues counting in the timer clock cycle following the write operation.

Timer/Counter0 Output Compare Register – OCR0

Bit	7	6	5	4	3	2	1	0	
$31 ($51)	MSB							LSB	OCR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Timer/Counter2 Output Compare Register – OCR2

Bit	7	6	5	4	3	2	1	0	
$22 ($42)	MSB							LSB	OCR2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The mechanisms for reading TCNT2, OCR2 and TCCR2 are different. When reading TCNT2, the actual timer value is read. When reading OCR2 or TCCR2, the value in the temporary storage register is read.

Asynchronous Operation of Timer/Counter2

When Timer/Counter2 operates asynchronously, some considerations must be taken:

- When switching between asynchronous and synchronous clocking of Timer/Counter2, the timer registers TCNT2, OCR2 and TCCR2 might get corrupted. A safe procedure for switching the clock source is:
  1. Disable the Timer/Counter2 interrupts by clearing OCIE2 and TOIE2.
  2. Select clock source by setting AS2 as appropriate.
  3. Write new values to TCNT2, OCR2 and TCCR2.
  4. To switch to asynchronous operation: Wait for TCN2UB, OCR2UB, and TCR2UB.
  5. Enable interrupts, if needed.
- The oscillator is optimized for use with a 32.768 kHz watch crystal. An external clock signal applied to this pin goes through the same amplifier having a bandwidth of 256 kHz. The external clock signal should therefore be in the interval
  0 Hz – 1 MHz. The frequency of the clock signal applied to the TOSC1 pin must be lower than one fourth of the CPU main clock frequency.
- When writing to one of the registers TCNT2, OCR2, or TCCR2, the value is transferred to a temporary register, and latched after two positive edges on TOSC1. The user should not write a new value before the contents of the temporary register have been transferred to its destination. Each of the three mentioned registers have their individual temporary register, which means that, e.g., writing to TCNT2 does not disturb an OCR2 write in progress. To detect that a transfer to the destination register has taken place, an Asynchronous Status Register – ASSR has been implemented.
- When entering Power-save mode after having written to TCNT2, OCR2, or TCCR2, the user must wait until the written register has been updated if Timer/Counter2 is used to wake-up the device. Otherwise, the MCU will go to sleep before the changes have had any effect. This is extremely important if the Output Compare2 interrupt is used to wake-up the device; Output compare is disabled during write to OCR2 or TCNT2. If the write cycle is not finished (i.e., the MCU enters Sleep mode before the OCR2UB bit returns to zero), the device will never get a compare match and the MCU will not wake-up.
- If Timer/Counter2 is used to wake-up the device from Power-save mode, precautions must be taken if the user wants to re-enter Power-save mode: The interrupt logic needs one TOSC1 cycle to be reset. If the time between wake-up and reentering Power-save mode is less than one TOSC1 cycle, the interrupt will not occur and the device will fail to wake up. If the user is in doubt whether the time before re-entering power-save is sufficient, the following algorithm can be used to ensure that one TOSC1 cycle has elapsed:
  1. Write a value to TCCR2, TCNT2, or OCR2.
  2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
  3. Enter Power-save mode.
- When asynchronous operation is selected, the 32.768 kHz oscillator for Timer/Counter2 is always running, except in Power-down mode. After a power-up reset or wake-up from power-down, the user should be aware of the fact that this oscillator might take as long as one second to stabilize. Therefore, the contents of all Timer2 registers must be considered lost after a wake-up from power-down, due to the unstable clock signal. The user is advised to wait for at least one second before using Timer/Counter2 after power-up or wake-up from power-down.
- Description of wake-up from Power-save mode when the timer is clocked asynchronously. When the interrupt condition is met, the wake-up process is started on the following cycle

Table 32. PWM Outputs OCR1X = $0000 or TOP[1]

COM1X1[2]	COM1X0[2]	OCR1X[2]	Output OC1X[2]
1	0	$0000	L
1	0	TOP	H
1	1	$0000	H
1	1	TOP	L

Notes: 1. In overflow PWM mode, this table is only valid for OCR1X = TOP.
2. X = A or B

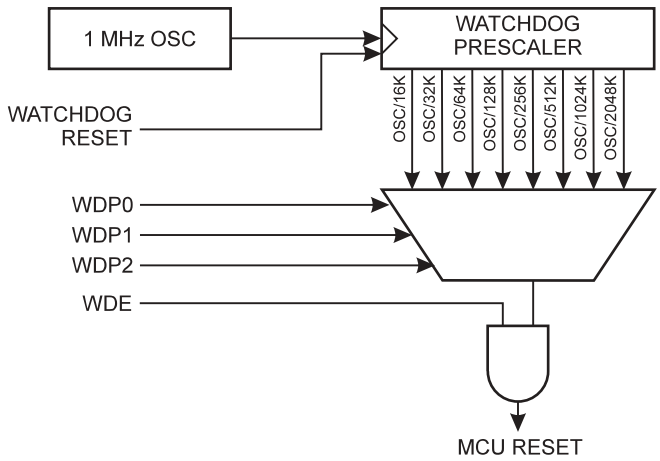
In up/down PWM mode, the Timer Overflow Flag1, TOV1, is set when the counter advances from $0000. In overflow PWM mode, the Timer Overflow flag is set as in normal Timer/Counter mode. Timer Overflow Interrupt1 operates exactly as in normal Timer/Counter mode, i.e., it is executed when TOV1 is set provided that Timer Overflow Interrupt1 and global interrupts are enabled. This also applies to the Timer Output Compare1 flags and interrupts.

Watchdog Timer

The Watchdog Timer is clocked from a separate on-chip oscillator which runs at 1 MHz. This is the typical value at V_{CC} = 3.3V. See characterization data for typical values at other V_{CC} levels. By controlling the Watchdog Timer prescaler, the watchdog reset interval can be adjusted, see Table 33 on page 105 for a detailed description. The WDR (watchdog reset) instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another watchdog reset, the FPSLIC resets and executes from the reset vector.

To prevent unintentional disabling of the watchdog, a special turn-off sequence must be followed when the watchdog is disabled, see Figure 58.

Figure 58. Watchdog Timer



fmuls16x16_32

Description

Signed fractional multiply of two 16-bit numbers with a 32-bit result.

Usage

R19:R18:R17:R16 = (R23:R22 • R21:R20) << 1

Statistics

Cycles: 20 + ret

Words: 16 + ret

Register usage: R0 to R2 and R16 to R23 (11 registers)[1]

Note: 1. The routine is non-destructive to the operands.

```
fmuls16x16_32:
   clr   r2
   fmuls r23, r21             ; ( (signed)ah * (signed)bh ) << 1
   movw  r19:r18, r1:r0
   fmul  r22, r20             ; ( al * bl ) << 1
   adc   r18, r2
   movw  r17:r16, r1:r0
   fmulsu   r23, r20          ; ( (signed)ah * bl ) << 1
   sbc   r19, r2              ; Sign extend
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   fmulsu   r21, r22          ; ( (signed)bh * al ) << 1
   sbc   r19, r2              ; Sign extend
   add   r17, r0
   adc   r18, r1
   adc   r19, r2
   ret
```

fmac16x16_32

Description

Signed fractional multiply-accumulate of two 16-bit numbers with a 32-bit result.

Usage

R19:R18:R17:R16 += (R23:R22 • R21:R20) << 1

Statistics

Cycles: 25 + ret

Words: 21 + ret

Register usage: R0 to R2 and R16 to R23 (11 registers)

```
fmac16x16_32:                 ; Register usage optimized
   clr   r2

   fmuls r23, r21             ; ( (signed)ah * (signed)bh ) << 1
   add   r18, r0
   adc   r19, r1

   fmul  r22, r20             ; ( al * bl ) << 1
   adc   r18, r2
   adc   r19, r2
   add   r16, r0
```

Table 36. UBR Settings at Various Crystal Frequencies

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
1	**0000**	**00011001**	**019**	**25**	**2404**	**2400**	**0.2**
	0000	**00001100**	**00C**	**12**	**4808**	**4800**	**0.2**
	0000	00000110	006	6	8929	9600	7.5
	0000	00000011	003	3	15625	14400	7.8
	0000	00000010	002	2	20833	19200	7.8
	0000	00000001	001	1	31250	28880	7.6
	0000	00000001	001	1	31250	38400	22.9
	0000	00000000	000	0	62500	57600	7.8
	0000	00000000	000	0	62500	76800	22.9
	0000	00000000	000	0	62500	115200	84.3

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
1.8432	**0000**	**00101111**	**02F**	**47**	**2400**	**2400**	**0.0**
	0000	**00010111**	**017**	**23**	**4800**	**4800**	**0.0**
	0000	**00001011**	**00B**	**11**	**9600**	**9600**	**0.0**
	0000	**00000111**	**007**	**7**	**14400**	**14400**	**0.0**
	0000	**00000101**	**005**	**5**	**19200**	**19200**	**0.0**
	0000	**00000011**	**003**	**3**	**28800**	**28880**	**0.3**
	0000	**00000010**	**002**	**2**	**38400**	**38400**	**0.0**
	0000	**00000001**	**001**	**1**	**57600**	**57600**	**0.0**
	0000	00000001	001	1	57600	76800	33.3
	0000	**00000000**	**000**	**0**	**115200**	**115200**	**0.0**

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
9.216	**0000**	**11101111**	**0EF**	**239**	**2400**	**2400**	**0.0**
	0000	**01110111**	**077**	**119**	**4800**	**4800**	**0.0**
	0000	**00111011**	**03B**	**59**	**9600**	**9600**	**0.0**
	0000	**00100111**	**027**	**39**	**14400**	**14400**	**0.0**
	0000	**00011101**	**01D**	**29**	**19200**	**19200**	**0.0**
	0000	**00010011**	**013**	**19**	**28800**	**28880**	**0.3**
	0000	**00001110**	**00E**	**14**	**38400**	**38400**	**0.0**
	0000	**00001001**	**009**	**9**	**57600**	**57600**	**0.0**
	0000	00000111	007	7	72000	76800	6.7
	0000	**00000100**	**004**	**4**	**115200**	**115200**	**0.0**
	0000	00000001	001	1	288000	230400	20.0
	0000	00000000	000	0	576000	460800	20.0
	0000	00000000	000	0	576000	912600	58.4

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
18.432	**0001**	**11011111**	**1DF**	**479**	**2400**	**2400**	**0.0**
	0000	**11101111**	**0EF**	**239**	**4800**	**4800**	**0.0**
	0000	**01110111**	**077**	**119**	**9600**	**9600**	**0.0**
	0000	**01001111**	**04F**	**79**	**14400**	**14400**	**0.0**
	0000	**00111011**	**03B**	**59**	**19200**	**19200**	**0.0**
	0000	**00100111**	**027**	**39**	**28800**	**28880**	**0.3**
	0000	**00011101**	**01D**	**29**	**38400**	**38400**	**0.0**
	0000	**00010011**	**013**	**19**	**57600**	**57600**	**0.0**
	0000	**00001110**	**00E**	**14**	**76800**	**76800**	**0.0**
	0000	**00001001**	**009**	**9**	**115200**	**115200**	**0.0**
	0000	**00000100**	**004**	**4**	**230400**	**230400**	**0.0**
	0000	00000001	001	1	576000	460800	20.0
	0000	00000000	000	0	1152000	912600	20.8

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
25.576	**0010**	**10011001**	**299**	**665**	**2400**	**2400**	**0.0**
	0001	**01001100**	**14C**	**332**	**4800**	**4800**	**0.0**
	0000	**10100110**	**0A6**	**166**	**9572**	**9600**	**0.3**
	0000	**01101110**	**06E**	**110**	**14401**	**14400**	**0.0**
	0000	**01010010**	**052**	**82**	**19259**	**19200**	**0.3**
	0000	**00110110**	**036**	**54**	**29064**	**28880**	**0.6**
	0000	**00101001**	**029**	**41**	**38060**	**38400**	**0.9**
	0000	**00011011**	**01B**	**27**	**57089**	**57600**	**0.9**
	0000	**00010100**	**014**	**20**	**76119**	**76800**	**0.9**
	0000	**00001101**	**00D**	**13**	**114179**	**115200**	**0.9**
	0000	**00000110**	**006**	**6**	**228357**	**230400**	**0.9**
	0000	00000011	003	3	399625	460800	15.3
	0000	00000001	001	1	799250	912600	14.2

Clock MHz	UBRRHI 7:4 or 3:0	UBRRn	UBR HEX	UBR	Actual Freq	Desired Freq.	% Error
40	**0100**	**00010001**	**411**	**1041**	**2399**	**2400**	**0.0**
	0010	**00001000**	**208**	**520**	**4798**	**4800**	**0.0**
	0001	**00000011**	**103**	**259**	**9615**	**9600**	**0.2**
	0000	**10101100**	**0AC**	**172**	**14451**	**14400**	**0.4**
	0000	**10000001**	**081**	**129**	**19231**	**19200**	**0.2**
	0000	**01010110**	**056**	**86**	**28736**	**28880**	**0.5**
	0000	**01000000**	**040**	**64**	**38462**	**38400**	**0.2**
	0000	**00101010**	**02A**	**42**	**58140**	**57600**	**0.9**
	0000	00100000	020	32	75758	76800	1.4
	0000	00010101	015	21	113636	115200	1.4
	0000	00001010	00A	10	227273	230400	1.4
	0000	00000100	004	4	500000	460800	7.8
	0000	00000010	002	2	833333	912600	9.5

UART0 and UART1 High Byte Baud-rate Register UBRRHI

Bit	7	6	5	4	3	2	1	0	
$20 ($40)	**MSB1**			**LSB1**	**MSB0**			**LSB0**	**UBRRHI**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The UART baud register is a 12-bit register. The 4 most significant bits are located in a separate register, UBRRHI. Note that both UART0 and UART1 share this register. Bit 7 to bit 4 of UBRRHI contain the 4 most significant bits of the UART1 baud register. Bit 3 to bit 0 contain the 4 most significant bits of the UART0 baud register.

- **Bits 7..0 - 2-wire Serial Bit-rate Register**

TWBR selects the division factor for the bit-rate generator. The bit-rate generator is a frequency divider which generates the SCL clock frequency in the Master modes according to the following equation:

$$\text{Bit-rate} = \frac{f_{CK}}{16 + 2(\text{TWBR})}$$

- Bit-rate = SCL frequency
- f_{CK} = CPU Clock frequency
- TWBR = Contents of the 2-wire Serial Bit Rate Register

Both the receiver and the transmitter can stretch the Low period of the SCL line when waiting for user response, thereby reducing the average bit rate.

The 2-wire Serial Control Register – TWCR

Bit	7	6	5	4	3	2	1	0	
$36 ($56)	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE	TWCR
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 - TWINT: 2-wire Serial Interrupt Flag**

This bit is set by the hardware when the 2-wire Serial Interface has finished its current job and expects application software response. If the I-bit in the SREG and TWIE in the TWCR register are set (one), the MCU will jump to the interrupt vector at address $0046. While the TWINT flag is set, the bus SCL clock line Low period is stretched. The TWINT flag must be cleared by software by writing a logic 1 to it. Note that this flag is not automatically cleared by the hardware when executing the interrupt routine. Also note that clearing this flag starts the operation of the 2-wire Serial Interface, so all accesses to the 2-wire Serial Address Register – TWAR, 2-wire Serial Status Register – TWSR, and 2-wire Serial Data Register – TWDR must be complete before clearing this flag.

- **Bit 6 - TWEA: 2-wire Serial Enable Acknowledge Flag**

TWEA flag controls the generation of the acknowledge pulse. If the TWEA bit is set, the ACK pulse is generated on the 2-wire Serial Bus if the following conditions are met:

- The device's own Slave address has been detected
- A general call has been received, while the TWGCE bit in the TWAR is set
- A data byte has been received in Master Receiver or Slave Receiver mode

By setting the TWEA bit Low the device can be virtually disconnected from the 2-wire Serial Bus temporarily. Address recognition can then be resumed by setting the TWEA bit again.

- **Bit 5 - TWSTA: 2-wire Serial Bus START Condition Flag**

The TWSTA flag is set by the CPU when it desires to become a Master on the 2-wire Serial Bus. The 2-wire serial hardware checks if the bus is available, and generates a Start condition on the bus if the bus is free. However, if the bus is not free, the 2-wire Serial Interface waits until a STOP condition is detected, and then generates a new Start condition to claim the bus Master status.

The 2-wire Serial Data Register – TWDR

Bit	7	6	5	4	3	2	1	0	
$1F ($3F)	MSB							LSB	TWDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

- **Bits 7..0 - TWD: 2-wire Serial Data Register**

These eight bits constitute the next data byte to be transmitted, or the latest data byte received on the 2-wire Serial Bus.

In transmit mode, TWDR contains the next byte to be transmitted. In receive mode, the TWDR contains the last byte received. It is writable while the 2-wire Serial Interface is not in the process of shifting a byte. This occurs when the 2-wire Serial Interrupt flag (TWINT) is set by the hardware. Note that the data register cannot be initialized by the user before the first interrupt occurs. The data in TWDR remains stable as long as TWINT is set. While data is shifted out, data on the bus is simultaneously shifted in. TWDR always contains the last byte present on the bus, except after a wake up from Power-down Mode, or Power-save Mode by the 2-wire Serial Interrupt. For example, in the case of the lost bus arbitration, no data is lost in the transition from Master-to-Slave. Receiving the ACK flag is controlled by the 2-wire Serial Logic automatically, the CPU cannot access the ACK bit directly.

The 2-wire Serial (Slave) Address Register – TWAR

Bit	7	6	5	4	3	2	1	0	
$1E ($3E)	MSB						LSB	TWGCE	TWAR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	0	

- **Bits 7..1 - TWA: 2-wire Serial Slave Address Register**

These seven bits constitute the Slave address of the 2-wire Serial Bus interface unit.

- **Bit 0 - TWGCE: 2-wire Serial General Call Recognition Enable Bit**

This bit enables, if set, the recognition of the General Call given over the 2-wire Serial Bus.

The TWAR should be loaded with the 7-bit Slave address (in the seven most significant bits of TWAR) to which the 2-wire Serial Interface will respond when programmed as a Slave transmitter or receiver, and not needed in the Master modes. The LSB of TWAR is used to enable recognition of the general call address ($00). There is an associated address comparator that looks for the Slave address (or general call address if enabled) in the received serial address. If a match is found, an interrupt request is generated.

2-wire Serial Modes

The 2-wire Serial Interface can operate in four different modes:

- Master Transmitter
- Master Receiver
- Slave Receiver
- Slave Transmitter

Data transfer in each mode of operation is shown in Figure 71 to Figure 74. These figures contain the following abbreviations:

S: START condition

R: Read bit (High level at SDA)

W: Write bit (Low level at SDA)

A: Acknowledge bit (Low level at SDA)

$\overline{A}$: Not acknowledge bit (High level at SDA)

Data: 8-bit data byte

P: STOP condition

In Figure 71 to Figure 74, circles are used to indicate that the 2-wire Serial Interrupt flag is set. The numbers in the circles show the status code held in TWSR. At these points, an interrupt routine must be executed to continue or complete the 2-wire Serial Transfer. The 2-wire Serial Transfer is suspended until the 2-wire Serial Interrupt flag is cleared by software.

The 2-wire Serial Interrupt flag is not automatically cleared by the hardware when executing the interrupt routine. Also note that the 2-wire Serial Interface starts execution as soon as this bit is cleared, so that all access to TWAR, TWDR and TWSR must have been completed before clearing this flag.

When the 2-wire Serial Interrupt flag is set, the status code in TWSR is used to determine the appropriate software action. For each status code, the required software action and details of the following serial transfer are given in Table 41 to Table 45.

Master Transmitter Mode

In the Master Transmitter mode, a number of data bytes are transmitter to a Slave Receiver, see Figure 71. Before the Master Transmitter mode can be entered, the TWCR must be initialized as shown in Table 38.

Table 38. TWCR: Master Transmitter Mode Initialization

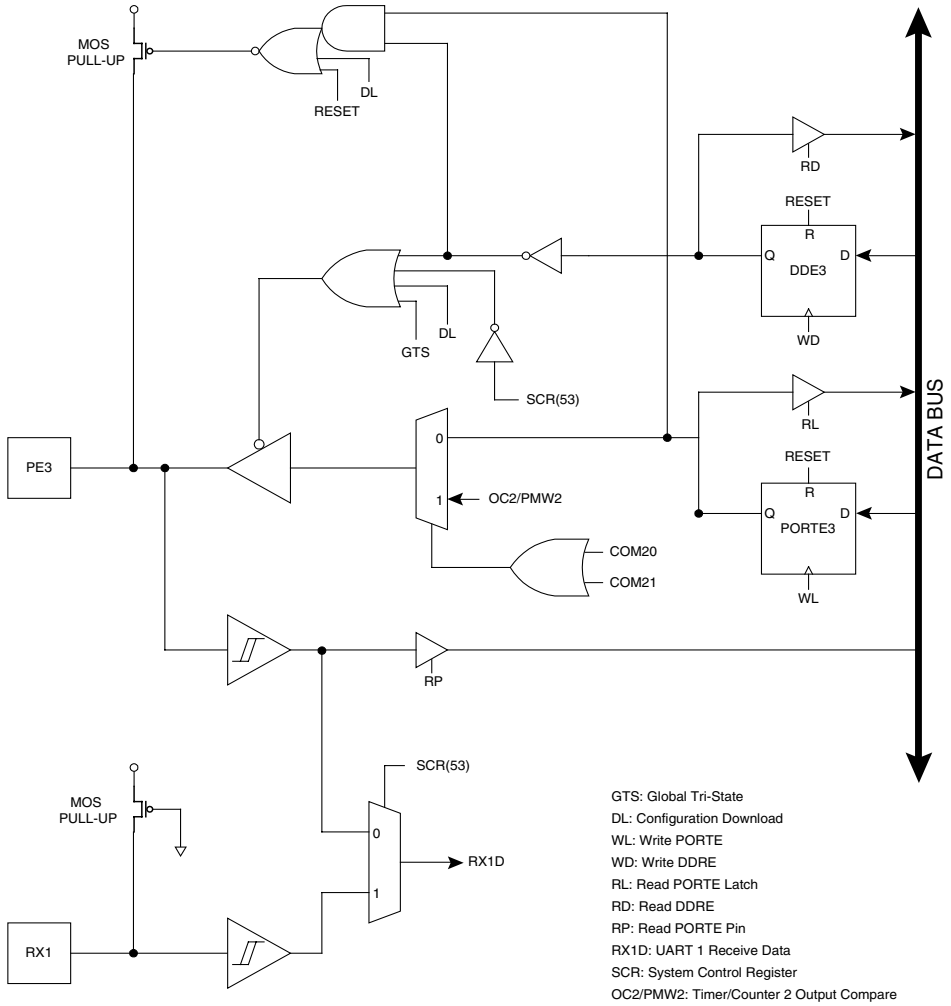
TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
value	0	X	0	0	0	1	0	X

TWEN must be set to enable the 2-wire Serial Interface, TWSTA and TWSTO must be cleared.

The Master Transmitter mode may now be entered by setting the TWSTA bit. The 2-wire Serial Logic will now test the 2-wire Serial Bus and generate a START condition as soon as the bus becomes free. When a START condition is transmitted, the 2-wire Serial Interrupt flag (TWINT) is set by the hardware, and the status code in TWSR will be $08. TWDR must then be loaded with the Slave address and the data direction bit (SLA+W). The TWINT flag must then be cleared by software before the 2-wire Serial Transfer can continue. The TWINT flag is cleared by writing a logic 1 to the flag.

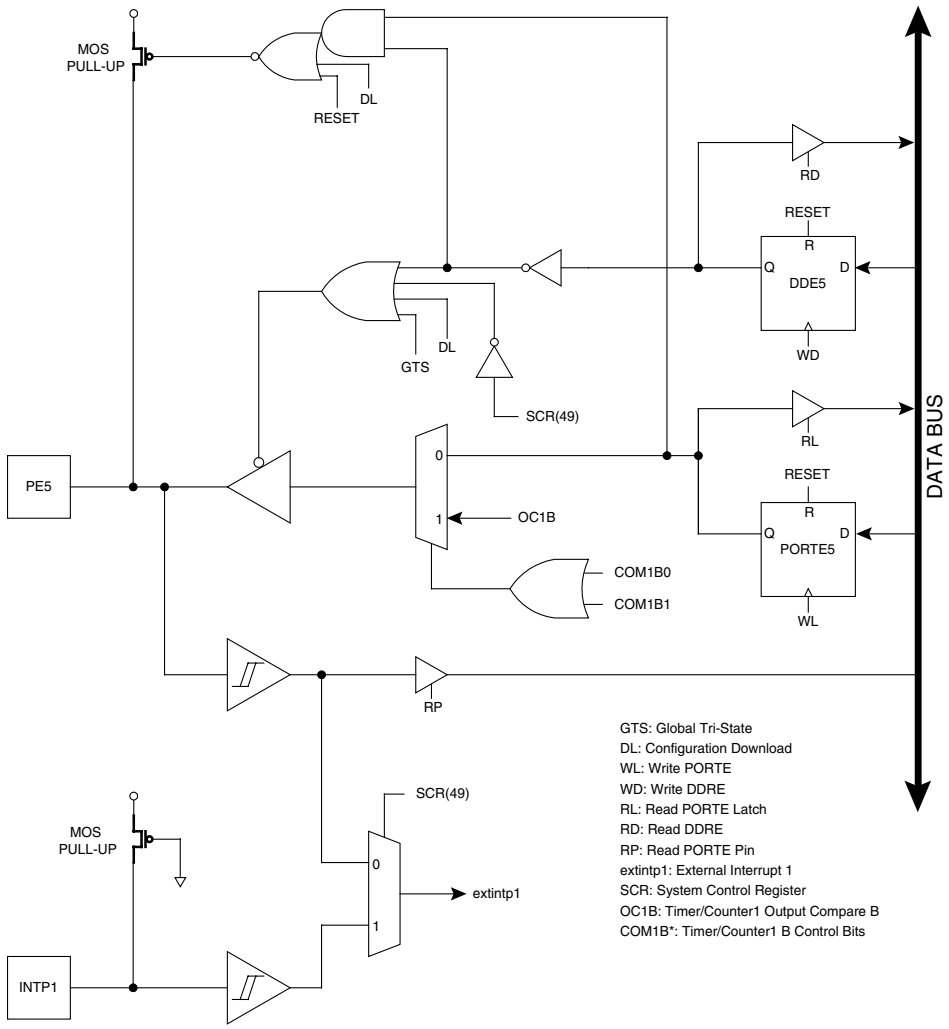
When the Slave address and the direction bit have been transmitted and an acknowledgment bit has been received, TWINT is set again and a number of status codes in TWSR are possible. Status codes $18, $20, or $38 apply to Master mode, and status codes $68, $78, or $B0 apply to Slave mode. The appropriate action to be taken for each of these status codes is

PortE Schematic Diagram (Pin PE3)



GTS: Global Tri-State
DL: Configuration Download
WL: Write PORTE
WD: Write DDRE
RL: Read PORTE Latch
RD: Read DDRE
RP: Read PORTE Pin
RX1D: UART 1 Receive Data
SCR: System Control Register
OC2/PMW2: Timer/Counter 2 Output Compare
COM2*: Timer/Counter2 Control Bits

Figure 80. PortE Schematic Diagram (Pin PE5)



AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-25	Units	Notes
Core					
2 Input Gate	t_{PD} (Maximum)	x/y -> x/y	2.9	ns	1 Unit Load
3 Input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.8	ns	1 Unit Load
3 Input Gate	t_{PD} (Maximum)	x/y/w -> x/y	3.4	ns	1 Unit Load
4 Input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	y -> y	2.3	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	x -> y	2.9	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	y -> x	3.0	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	x -> x	2.3	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	w -> y	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	w -> x	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	z -> y	3.4	ns	1 Unit Load
Fast Carry	t_{PD} (Maximum)	z -> x	2.4	ns	1 Unit Load
DFF	t_{PD} (Maximum)	q -> x/y	2.8	ns	1 Unit Load
DFF	t_{setup} (Minimum)	x/y -> clk	–	–	–
DFF	t_{hold} (Minimum)	x/y -> clk	–	–	–
DFF	t_{PD} (Maximum)	R -> x/y	3.2	ns	1 Unit Load
DFF	t_{PD} (Maximum)	S -> x/y	3.0	ns	1 Unit Load
DFF	t_{PD} (Maximum)	q -> w	2.7	ns	–
incremental -> L	t_{PD} (Maximum)	x/y -> L	2.4	ns	–
Local Output Enable	t_{PZX} (Maximum)	oe -> L	2.8	ns	1 Unit Load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	2.4	ns	

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-25	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	–
Write	t_{WEL} (Minimum)	we	5.0	ns	Pulse Width Low
Write	t_{WEH} (Minimum)	we	5.0	ns	Pulse Width High
Write	t_{setup} (Minimum)	wr addr setup-> we	5.3	ns	
Write	t_{hold} (Minimum)	wr addr hold -> we	0.0	ns	–
Write	t_{setup} (Minimum)	din setup -> we	5.0	ns	
Write	t_{hold} (Minimum)	din hold -> we	0.0	ns	–
Write	t_{hold} (Minimum)	oe hold -> we	0.0	ns	
Write/Read	t_{PD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Read	t_{PD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{PZX} (Maximum)	oe -> dout	2.9	ns	–
Read	t_{PXZ} (Maximum)	oe -> dout	3.5	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
Write	t_{CLKL} (Minimum)	clk	5.0	ns	–
Write	t_{CLKH} (Minimum)	clk	5.0	ns	Pulse Width High
Write	t_{setup} (Minimum)	we setup-> clk	3.2	ns	
Write	t_{hold} (Minimum)	we hold -> clk	0.0	ns	–
Write	t_{setup} (Minimum)	wr addr setup-> clk	5.0	ns	
Write	t_{hold} (Minimum)	wr addr hold -> clk	0.0	ns	–
Write	t_{setup} (Minimum)	wr data setup-> clk	3.9	ns	
Write	t_{hold} (Minimum)	wr data hold -> clk	0.0	ns	–
Write/Read	t_{PD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Write/Read	t_{PD} (Maximum)	clk -> dout	5.8	ns	rd addr = wr addr
Read	t_{PD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{PZX} (Maximum)	oe -> dout	2.9	ns	–
Read	t_{PXZ} (Maximum)	oe -> dout	3.5	ns	

CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant. Buffer delay is to a pad voltage of 1.5V with one output switching. Parameter based on characterization and simulation; not tested in production. An FPGA power calculation is available in Atmel's System Designer software (see also page 160).

Table 56. AT94K Pin List (Continued)

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
		I/O113				
		I/O114				
		GND				
		I/O115				
		I/O116				
	I/O59	I/O117				
	I/O60	I/O118				
		I/O119				
		I/O120				
GND	GND	GND			45	67
I/O41	I/O61	I/O121			46	68
I/O42	I/O62	I/O122			47	69
I/O43/TMS	I/O63/TMS	I/O123/TMS	38	31	48	70
I/O44/TCK	I/O64/TCK	I/O124/TCK	39	32	49	71
	$VCC^{(1)}$	$VCC^{(1)}$				
	I/O65	I/O125				72
	I/O66	I/O126				73
		GND				
		I/O127				
		I/O128				
		I/O129				
		I/O130				
		I/O131				
		I/O132				
		GND				
		$VCC^{(1)}$				
		I/O133				
		I/O134				
	I/O67	I/O135				
	I/O68	I/O136				
I/O45	I/O69	I/O137		33	50	74
I/O46	I/O70	I/O138		34	51	75
		GND				
		I/O139				

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.

Table 56. AT94K Pin List (Continued)

AT94K05 96 FPGA I/O	AT94K10 192 FPGA I/O	AT94K40 384 FPGA I/O	Packages			
			PC84	TQ100	PQ144	PQ208
	I/O173	I/O345				188
	I/O174	I/O346				189
I/O117 (A10)	I/O175 (A10)	I/O347 (A10)	5	94	133	190
I/O118 (A11)	I/O176 (A11)	I/O348 (A11)	6	95	134	191
		VCC(1)				
		GND				
		I/O349				
		I/O350				
		I/O351				
		I/O352				
		I/O353				
		I/O354				
		GND				
		I/O355				
		I/O356				
	VDD(2)	VDD(2)				
	I/O177	I/O357				
	I/O178	I/O358				
I/O119	I/O179	I/O359			135	192
I/O120	I/O180	I/O360			136	193
GND	GND	GND			137	194
		I/O361				
		I/O362				
	I/O181	I/O363				195
	I/O182	I/O364				196
		I/O365				
		I/O366				
		GND				
		I/O367				
		I/O368				
I/O121	I/O183	I/O369				197
I/O122	I/O184	I/O370				198
I/O123 (A12)	I/O185 (A12)	I/O371 (A12)	7	96	138	199
I/O124 (A13)	I/O186 (A13)	I/O372 (A13)	8	97	139	200

Notes:
1. VCC is I/O high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
2. VDD is core high voltage. Please refer to the “Designing in Split Power Supply Support for AT94KAL and AT94SAL Devices” application note.
3. Unbonded pins are No Connects.

Ordering Information

Usable Gates	Speed Grade	Ordering Code	Package	Operation Range
5,000	-25 MHz	AT94K05AL-25AJC AT94K05AL-25AQC AT94K05AL-25BQC AT94K05AL-25DQC	84J 100A 144L1 208Q1	Commercial (0°C - 70°C)
		AT94K05AL-25AJI AT94K05AL-25AQI AT94K05AL-25BQI AT94K05AL-25DQI	84J 100A 144L1 208Q1	Industrial (-40°C - 85°C)
10,000	-25 MHz	AT94K10AL-25AJC AT94K10AL-25AQC AT94K10AL-25BQC AT94K10AL-25DQC	84J 100A 144L1 208Q1	Commercial (0°C - 70°C)
		AT94K10AL-25AJI AT94K10AL-25AQI AT94K10AL-25BQI AT94K10AL-25DQI	84J 100A 144L1 208Q1	Industrial (-40°C - 85°C)
40,000	-25 MHz	AT94K40AL-25BQC AT94K40AL-25DQC	144L1 208Q1	Commercial (0°C - 70°C)
		AT94K40AL-25BQI AT94K40AL-25DQI	144L1 208Q1	Industrial (-40°C - 85°C)

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100A	100-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
144L1	144-lead, Low Profile Plastic Gull Wing Quad Flat Package (LQFP)
208Q1	208-lead, Plastic Gull Wing Quad Flat Package (PQFP)