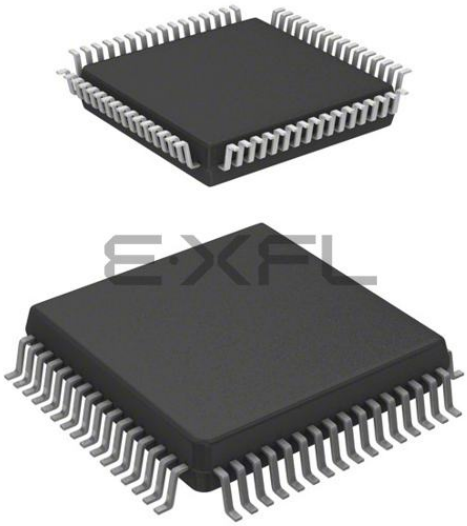

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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	53
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908gz60cfu

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0459	TIM2 Channel 3 Status and Control Register (T2SC3) See page 293.	Read:	CH3F	CH3IE	0	MS3A	ELS3B	ELS3A	TOV3	CH3MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$045A	TIM2 Channel 3 Register High (T2CH3H) See page 297.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$045B	TIM2 Channel 3 Register Low (T2CH3L) See page 297.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$045C	TIM2 Channel 4 Status and Control Register (T2SC4) See page 293.	Read:	CH4F	CH4IE	MS4B	MS4A	ELS4B	ELS4A	TOV4	CH4MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$045D	TIM2 Channel 4 Register High (T2CH4H) See page 297.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$045E	TIM2 Channel 4 Register Low (T2CH4L) See page 297.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$045F	TIM2 Channel 5 Status and Control Register (T2SC5) See page 293.	Read:	CH5F	CH5IE	0	MS5A	ELS5B	ELS5A	TOV 5	CH5MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0460	TIM2 Channel 5 Register High (T2CH5H) See page 297.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$0461	TIM2 Channel 5 Register Low (T2CH5L) See page 297.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$FE00	Break Status Register (BSR) See page 237.	Read:	R	R	R	R	R	R	SBSW	R
		Write:							NOTE 1	
		Reset:	0	0	0	0	0	0	0	0

1. Writing a 0 clears SBSW.

$FE01	SIM Reset Status Register (SRSR) See page 237.	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:								
		POR:	1	0	0	0	0	0	0	0
$FE02	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 7 of 9)

2.6.2.2 FLASH-1 Block Protect Register

The FLASH-1 block protect register (FL1BPR) is implemented as a byte within the FLASH-1 memory; therefore, it can only be written during a FLASH programming sequence. The value in this register determines the starting location of the protected range within the FLASH-1 memory.

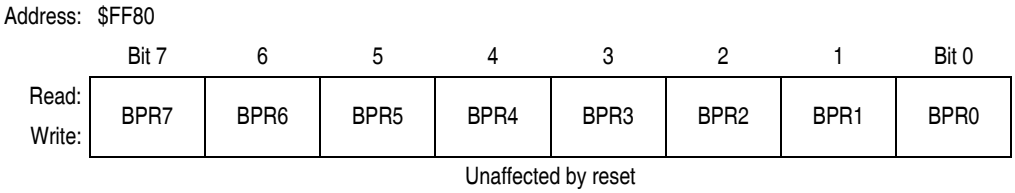

Figure 2-4. FLASH-1 Block Protect Register (FL1BPR)

FL1BPR[7:0] — Block Protect Register Bits 7 to 0

These eight bits represent bits [14:7] of a 16-bit memory address. Bit 15 is a 1 and bits [6:0] are 0s.

The resultant 16-bit address is used for specifying the start address of the FLASH-1 memory for block protection. FLASH-1 is protected from this start address to the end of FLASH-1 memory at $FFFF. With this mechanism, the protect start address can be $XX00 and $XX80 (128 byte page boundaries) within the FLASH-1 array.

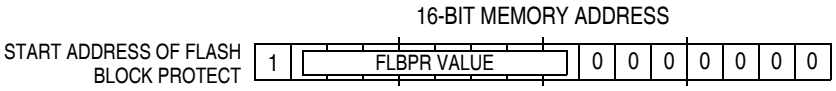

Figure 2-5. FLASH-1 Block Protect Start Address

Table 2-2. FLASH-1 Protected Ranges

FL1BPR[7:0]	Protected Range
$FF	No protection
$FE	$FF00–$FFFF
$FD ↓ $0B	$FE80–$FFFF ↓ $8580–$FFFF
$0A	$8500–$FFFF
$09	$8480–$FFFF
$08 ↓ $04	$8400–$FFFF ↓ $8200–$FFFF
$03	$8180–$FFFF
$02	$8100–$FFFF
$01	$8080–$FFFF
$00	$8000–$FFFF

Decreasing the value in FL1BPR by one increases the protected range by one page (128 bytes). However, programming the block protect register with $FE protects a range twice that size, 256 bytes, in the corresponding array. $FE means that locations $FF00–$FFFF are protected in FLASH-1.

The FLASH memory does not exist at some locations. The block protection range configuration is unaffected if FLASH memory does not exist in that range. Refer to Figure 2-1 and make sure that the desired locations are protected.

2.6.3 FLASH-1 Block Protection

Due to the ability of the on-board charge pump to erase and program the FLASH memory in the target application, provision is made for protecting blocks of memory from unintentional erase or program operations due to system malfunction. This protection is done by using the FLASH-1 block protection register (FL1BPR). FL1BPR determines the range of the FLASH-1 memory which is to be protected. The range of the protected area starts from a location defined by FL1BPR and ends at the bottom of the FLASH-1 memory ($FFFF). When the memory is protected, the HVEN bit can not be set in either ERASE or PROGRAM operations.

NOTE

In performing a program or erase operation, the FLASH-1 block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit.

When the FLASH-1 block protect register is programmed with all 0's, the entire memory is protected from being programmed and erased. When all the bits are erased (all 1's), the entire memory is accessible for program and erase.

When bits within FL1BPR are programmed (0), they lock a block of memory address ranges as shown in Figure 2-4. If FL1BPR is programmed with any value other than $FF, the protected block of FLASH memory can not be erased or programmed.

NOTE

The vector locations and the FLASH block protect registers are located in the same page. FL1BPR and FL2BPR are not protected with special hardware or software. Therefore, if this page is not protected by FL1BPR and the vector locations are erased by either a page or a mass erase operation, then both FL1BPR and FL2BPR will also get erased.

2.6.4 FLASH-1 Mass Erase Operation

Use this step-by-step procedure to erase the entire FLASH-1 memory:

1. Set both the ERASE bit and the MASS bit in the FLASH-1 control register (FL1CR).
2. Read the FLASH-1 block protect register (FL1BPR).

NOTE

Mass erase is disabled whenever any block is protected (FL1BPR does not equal $FF).

3. Write to any FLASH-1 address within the FLASH-1 array with any data.
4. Wait for a time, t_{NVS} (minimum 10 μs).
5. Set the HVEN bit.
6. Wait for a time, t_{MERASE} (minimum 4 ms).
7. Clear the ERASE and MASS bits.
8. Wait for a time, t_{NVHL} (minimum 100 μs).
9. Clear the HVEN bit.
10. Wait for a time, t_{RCV}, (typically 1 μs) after which the memory can be accessed in normal read mode.

NOTES

A. *Programming and erasing of FLASH locations can not be performed by code being executed from the same FLASH array.*

4.3.1 Crystal Oscillator Circuit

The crystal oscillator circuit consists of an inverting amplifier and an external crystal. The OSC1 pin is the input to the amplifier and the OSC2 pin is the output. The SIMOSCEN signal from the system integration module (SIM) or the OSCENINSTOP bit in the CONFIG register enable the crystal oscillator circuit.

The CGMXCLK signal is the output of the crystal oscillator circuit and runs at a rate equal to the crystal frequency. CGMXCLK is then buffered to produce CGMRCLK, the PLL reference clock.

CGMXCLK can be used by other modules which require precise timing for operation. The duty cycle of CGMXCLK is not guaranteed to be 50% and depends on external factors, including the crystal and related external components. An externally generated clock also can feed the OSC1 pin of the crystal oscillator circuit. Connect the external clock to the OSC1 pin and let the OSC2 pin float.

4.3.2 Phase-Locked Loop Circuit (PLL)

The PLL is a frequency generator that can operate in either acquisition mode or tracking mode, depending on the accuracy of the output frequency. The PLL can change between acquisition and tracking modes either automatically or manually.

4.3.3 PLL Circuits

The PLL consists of these circuits:

- Voltage-controlled oscillator (VCO)
- Modulo VCO frequency divider
- Phase detector
- Loop filter
- Lock detector

The operating range of the VCO is programmable for a wide range of frequencies and for maximum immunity to external noise, including supply and CGMXFC noise. The VCO frequency is bound to a range from roughly one-half to twice the center-of-range frequency, f_{VRS}. Modulating the voltage on the CGMXFC pin changes the frequency within this range. By design, f_{VRS} is equal to the nominal center-of-range frequency, f_{NOM}, (71.4 kHz) times a linear factor, L, and a power-of-two factor, E, or $(L \times 2^E)f_{NOM}$.

CGMRCLK is the PLL reference clock, a buffered version of CGMXCLK. CGMRCLK runs at a frequency, f_{RCLK}. The VCO's output clock, CGMVCLK, running at a frequency, f_{VCLK}, is fed back through a programmable modulo divider. The modulo divider reduces the VCO clock by a factor, N. The dividers output is the VCO feedback clock, CGMVDV, running at a frequency, $f_{VDV} = f_{VCLK}/(N)$. (For more information, see 4.3.6 Programming the PLL.)

The phase detector then compares the VCO feedback clock, CGMVDV, with the final reference clock, CGMRDV. A correction pulse is generated based on the phase difference between the two signals. The loop filter then slightly alters the DC voltage on the external capacitor connected to CGMXFC based on the width and direction of the correction pulse. The filter can make fast or slow corrections depending on its mode, described in 4.3.4 Acquisition and Tracking Modes. The value of the external capacitor and the reference frequency determines the speed of the corrections and the stability of the PLL.

The lock detector compares the frequencies of the VCO feedback clock, CGMVDV, and the reference clock, CGMRCLK. Therefore, the speed of the lock detector is directly proportional to the reference

NOTE

Do not inadvertently clear the PLLF bit. Any read or read-modify-write operation on the PLL control register clears the PLLF bit.

PLLON — PLL On Bit

This read/write bit activates the PLL and enables the VCO clock, CGMVCLK. PLLON cannot be cleared if the VCO clock is driving the base clock, CGMOUT (BCS = 1). (See 4.3.8 Base Clock Selector Circuit.) Reset sets this bit so that the loop can stabilize as the MCU is powering up.

1 = PLL on
0 = PLL off

BCS — Base Clock Select Bit

This read/write bit selects either the crystal oscillator output, CGMXCLK, or the VCO clock, CGMVCLK, as the source of the CGM output, CGMOUT. CGMOUT frequency is one-half the frequency of the selected clock. BCS cannot be set while the PLLON bit is clear. After toggling BCS, it may take up to three CGMXCLK and three CGMVCLK cycles to complete the transition from one source clock to the other. During the transition, CGMOUT is held in stasis. (See 4.3.8 Base Clock Selector Circuit.) Reset clears the BCS bit.

1 = CGMVCLK divided by two drives CGMOUT
0 = CGMXCLK divided by two drives CGMOUT

NOTE

PLLON and BCS have built-in protection that prevents the base clock selector circuit from selecting the VCO clock as the source of the base clock if the PLL is off. Therefore, PLLON cannot be cleared when BCS is set, and BCS cannot be set when PLLON is clear. If the PLL is off (PLLON = 0), selecting CGMVCLK requires two writes to the PLL control register. (See 4.3.8 Base Clock Selector Circuit.).

VPR1 and VPR0 — VCO Power-of-Two Range Select Bits

These read/write bits control the VCO's hardware power-of-two range multiplier E that, in conjunction with L controls the hardware center-of-range frequency, f_{VRS}. VPR1:VPR0 cannot be written when the PLLON bit is set. Reset clears these bits. (See 4.3.3 PLL Circuits, 4.3.6 Programming the PLL, and 4.5.5 PLL VCO Range Select Register.)

Table 4-4. VPR1 and VPR0 Programming

VPR1 and VPR0	E	VCO Power-of-Two Range Multiplier
00	0	1
01	1	2
10	2(1)	4

1. Do not program E to a value of 3.

NOTE

Verify that the value of the VPR1 and VPR0 bits in the PCTL register are appropriate for the given reference and VCO clock frequencies before enabling the PLL. See 4.3.6 Programming the PLL for detailed instructions on selecting the proper value for these control bits.

MSCAN08 bus activity can wake the MCU from CPU stop/MSCAN08 power-down mode. However, until the oscillator starts up and synchronization is achieved the MSCAN08 will not respond to incoming data.

12.8.4 CPU Wait Mode

The MSCAN08 module remains active during CPU wait mode. The MSCAN08 will stay synchronized to the CAN bus and generates transmit, receive, and error interrupts to the CPU, if enabled. Any such interrupt will bring the MCU out of wait mode.

12.8.5 Programmable Wakeup Function

The MSCAN08 can be programmed to apply a low-pass filter function to the CAN_{RX} input line while in internal sleep mode (see information on control bit WUPM in 12.13.2 MSCAN08 Module Control Register 1). This feature can be used to protect the MSCAN08 from wakeup due to short glitches on the CAN bus lines. Such glitches can result from electromagnetic inference within noisy environments.

12.9 Timer Link

The MSCAN08 will generate a timer signal whenever a valid frame has been received. Because the CAN specification defines a frame to be valid if no errors occurred before the EOF field has been transmitted successfully, the timer signal will be generated right after the EOF. A pulse of one bit time is generated. As the MSCAN08 receiver engine also receives the frames being sent by itself, a timer signal also will be generated after a successful transmission.

The previously described timer signal can be routed into the on-chip timer interface module (TIM). This signal is connected to channel 0 of timer interface module 1 (TIM1) under the control of the timer link enable (TLNKEN) bit in CMCR0.

After timer n has been programmed to capture rising edge events, it can be used under software control to generate 16-bit time stamps which can be stored with the received message.

12.10 Clock System

Figure 12-8 shows the structure of the MSCAN08 clock generation circuitry and its interaction with the clock generation module (CGM). With this flexible clocking scheme the MSCAN08 is able to handle CAN bus rates ranging from 10 kbps up to 1 Mbps.

The clock source bit (CLKSRC) in the MSCAN08 module control register (CMCR1) (see 12.13.1 MSCAN08 Module Control Register 0) defines whether the MSCAN08 is connected to the output of the crystal oscillator or to the PLL output.

The clock source has to be chosen such that the tight oscillator tolerance requirements (up to 0.4%) of the CAN protocol are met.

NOTE

If the system clock is generated from a PLL, it is recommended to select the crystal clock source rather than the system clock source due to jitter considerations, especially at faster CAN bus rates.

12.13.6 MSCAN08 Receiver Interrupt Enable Register

Address: $0505

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WUPIE	RWRNIE	TWRNIE	RERRIE	TERRIE	BOFFIE	OVRIE	RXFIE
Reset:	0	0	0	0	0	0	0	0

Figure 12-21. Receiver Interrupt Enable Register (CRIER)

WUPIE — Wakeup Interrupt Enable

1 = A wakeup event will result in a wakeup interrupt.
0 = No interrupt will be generated from this event.

RWRNIE — Receiver Warning Interrupt Enable

1 = A receiver warning status event will result in an error interrupt.
0 = No interrupt is generated from this event.

TWRNIE — Transmitter Warning Interrupt Enable

1 = A transmitter warning status event will result in an error interrupt.
0 = No interrupt is generated from this event.

RERRIE — Receiver Error Passive Interrupt Enable

1 = A receiver error passive status event will result in an error interrupt.
0 = No interrupt is generated from this event.

TERRIE — Transmitter Error Passive Interrupt Enable

1 = A transmitter error passive status event will result in an error interrupt.
0 = No interrupt is generated from this event.

BOFFIE — Bus-Off Interrupt Enable

1 = A bus-off event will result in an error interrupt.
0 = No interrupt is generated from this event.

OVRIE — Overrun Interrupt Enable

1 = An overrun event will result in an error interrupt.
0 = No interrupt is generated from this event.

RXFIE — Receiver Full Interrupt Enable

1 = A receive buffer full (successful message reception) event will result in a receive interrupt.
0 = No interrupt will be generated from this event.

NOTE

The CRIER register is held in the reset state when the SFTRES bit in CMCR0 is set.

14.3 Pin Name Conventions

The generic names of the ESCI input/output (I/O) pins are:

- RxD (receive data)
- TxD (transmit data)

ESCI I/O lines are implemented by sharing parallel I/O port pins. The full name of an ESCI input or output reflects the name of the shared port pin. Table 14-1 shows the full names and the generic names of the ESCI I/O pins. The generic pin names appear in the text of this section.

Table 14-1. Pin Name Conventions

Generic Pin Names	RxD	TxD
Full Pin Names	PTE1/RxD	PTE0/TxD

14.4 Functional Description

Figure 14-3 shows the structure of the ESCI module. The ESCI allows full-duplex, asynchronous, NRZ serial communication between the MCU and remote devices, including other MCUs. The transmitter and receiver of the ESCI operate independently, although they use the same baud rate generator. During normal operation, the CPU monitors the status of the ESCI, writes the data to be transmitted, and processes received data.

The baud rate clock source for the ESCI can be selected via the configuration bit, SCIBDSRC, of the CONFIG2 register ($001E)

For reference, a summary of the ESCI module input/output registers is provided in Figure 14-4.

14.4.1 Data Format

The SCI uses the standard non-return-to-zero mark/space data format illustrated in Figure 14-2.

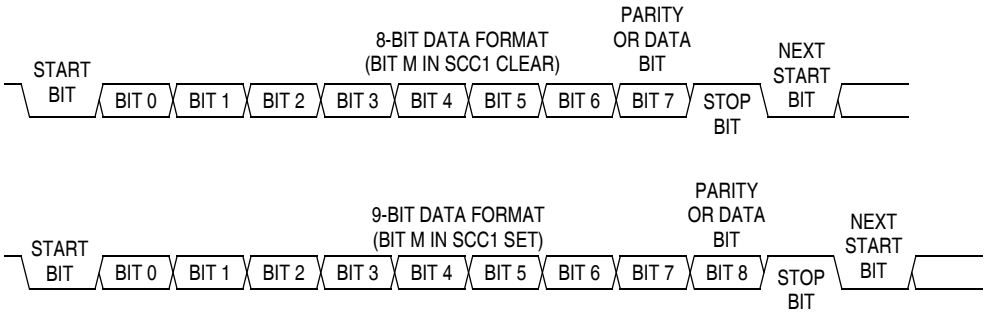

Figure 14-2. SCI Data Formats

14.4.3.5 Baud Rate Tolerance

A transmitting device may be operating at a baud rate below or above the receiver baud rate. Accumulated bit time misalignment can cause one of the three stop bit data samples to fall outside the actual stop bit. Then a noise error occurs. If more than one of the samples is outside the stop bit, a framing error occurs. In most applications, the baud rate tolerance is much more than the degree of misalignment that is likely to occur.

As the receiver samples an incoming character, it resynchronizes the RT clock on any valid falling edge within the character. Resynchronization within characters corrects misalignments between transmitter bit times and receiver bit times.

Slow Data Tolerance

Figure 14-8 shows how much a slow received character can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

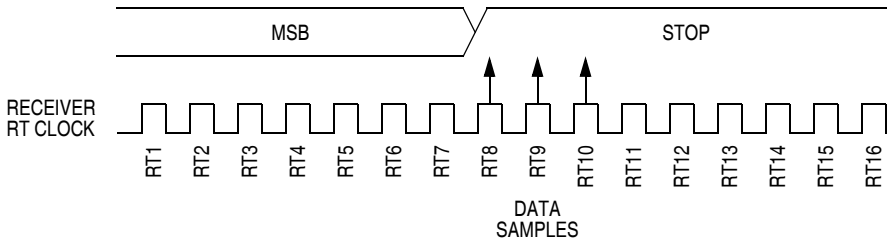

Figure 14-8. Slow Data

For an 8-bit character, data sampling of the stop bit takes the receiver
9 bit times × 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned character shown in Figure 14-8, the receiver counts 154 RT cycles at the point when the count of the transmitting device is
9 bit times × 16 RT cycles + 3 RT cycles = 147 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit character with no errors is:

$$\left|\frac{154 - 147}{154}\right| \times 100 = 4.54\%$$

For a 9-bit character, data sampling of the stop bit takes the receiver
10 bit times × 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in Figure 14-8, the receiver counts 170 RT cycles at the point when the count of the transmitting device is
10 bit times × 16 RT cycles + 3 RT cycles = 163 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is:

$$\left|\frac{170 - 163}{170}\right| \times 100 = 4.12\%$$

RPF — Reception in Progress Flag Bit

This read-only bit is set when the receiver detects a 0 during the RT1 time period of the start bit search. RPF does not generate an interrupt request. RPF is reset after the receiver detects false start bits (usually from noise or a baud rate mismatch), or when the receiver detects an idle character. Polling RPF before disabling the ESCI module or entering stop mode can show whether a reception is in progress.

1 = Reception in progress
0 = No reception in progress

14.8.6 ESCI Data Register

The ESCI data register (SCDR) is the buffer between the internal data bus and the receive and transmit shift registers. Reset has no effect on data in the ESCI data register.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	Unaffected by reset							

Figure 14-16. ESCI Data Register (SCDR)

R7/T7:R0/T0 — Receive/Transmit Data Bits

Reading address $0018 accesses the read-only received data bits, R7:R0. Writing to address $0018 writes the data to be transmitted, T7:T0. Reset has no effect on the ESCI data register.

NOTE

Do not use read-modify-write instructions on the ESCI data register.

14.8.7 ESCI Baud Rate Register

The ESCI baud rate register (SCBR) together with the ESCI prescaler register selects the baud rate for both the receiver and the transmitter.

NOTE

There are two prescalers available to adjust the baud rate. One in the ESCI baud rate register and one in the ESCI prescaler register.

Address: $0019

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LINT	LINR	SCP1	SCP0	R	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 14-17. ESCI Baud Rate Register (SCBR)

LINT — LIN Transmit Enable

This read/write bit selects the enhanced ESCI features for the local interconnect network (LIN) protocol as shown in Table 14-6. Reset clears LINT.

ARUN— Arbiter Counter Running Flag

This read-only bit indicates the arbiter counter is running. Reset clears ARUN.

1 = Arbiter counter running
0 = Arbiter counter stopped

AROVFL— Arbiter Counter Overflow Bit

This read-only bit indicates an arbiter counter overflow. Clear AROVFL by writing any value to SCIACTL. Writing 0s to AM1 and AM0 resets the counter keeps it in this idle state. Reset clears AROVFL.

1 = Arbiter counter overflow has occurred
0 = No arbiter counter overflow has occurred

ARD8— Arbiter Counter MSB

This read-only bit is the MSB of the 9-bit arbiter counter. Clear ARD8 by writing any value to SCIACTL. Reset clears ARD8.

14.9.2 ESCI Arbiter Data Register

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-20. ESCI Arbiter Data Register (SCIADAT)

ARD7–ARD0 — Arbiter Least Significant Counter Bits

These read-only bits are the eight LSBs of the 9-bit arbiter counter. Clear ARD7–ARD0 by writing any value to SCIACTL. Writing 0s to AM1 and AM0 permanently resets the counter and keeps it in this idle state. Reset clears ARD7–ARD0.

14.9.3 Bit Time Measurement

Two bit time measurement modes, described here, are available according to the state of ACLK.

1. ACLK = 0 — The counter is clocked with the bus clock divided by four. The counter is started when a falling edge on the RxD pin is detected. The counter will be stopped on the next falling edge. ARUN is set while the counter is running, AFIN is set on the second falling edge on RxD (for instance, the counter is stopped). This mode is used to recover the received baud rate. See Figure 14-21.
2. ACLK = 1 — The counter is clocked with one half of the ESCI input clock generated by the ESCI prescaler. The counter is started when a 0 is detected on RxD (see Figure 14-22). A 0 on RxD on enabling the bit time measurement with ACLK = 1 leads to immediate start of the counter (see Figure 14-23). The counter will be stopped on the next rising edge of RxD. This mode is used to measure the length of a received break.

14.9.4 Arbitration Mode

If AM[1:0] is set to 10, the arbiter module operates in arbitration mode. On every rising edge of SCI_TxD (output of the ESCI module, internal chip signal), the counter is started. When the counter reaches $38 (ACLK = 0) or $08 (ACLK = 1), RxD is statically sensed. If in this case, RxD is sensed low (for example,

16.9.2 Stop Mode

The SPI module is inactive after the execution of a STOP instruction. The STOP instruction does not affect register conditions. SPI operation resumes after an external interrupt. If stop mode is exited by reset, any transfer in progress is aborted, and the SPI is reset.

16.10 SPI During Break Interrupts

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. BCFE in the SIM break flag control register (SBFCR) enables software to clear status bits during the break state. See Chapter 15 System Integration Module (SIM).

To allow software to clear status bits during a break interrupt, write a 1 to BCFE. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to BCFE. With BCFE at 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a 2-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is 0. After the break, doing the second step clears the status bit.

Since the SPTE bit cannot be cleared during a break with BCFE cleared, a write to the transmit data register in break mode does not initiate a transmission nor is this data transferred into the shift register. Therefore, a write to the SPDR in break mode with BCFE cleared has no effect.

16.11 I/O Signals

The SPI module has four I/O pins:

- MISO — Master input/slave output
- MOSI — Master output/slave input
- SPSCK — Serial clock
- $\overline{SS}$ — Slave select

16.11.1 MISO (Master In/Slave Out)

MISO is one of the two SPI module pins that transmits serial data. In full duplex operation, the MISO pin of the master SPI module is connected to the MISO pin of the slave SPI module. The master SPI simultaneously receives data on its MISO pin and transmits data from its MOSI pin.

Slave output data on the MISO pin is enabled only when the SPI is configured as a slave. The SPI is configured as a slave when its SPMSTR bit is 0 and its $\overline{SS}$ pin is low. To support a multiple-slave system, a high on the $\overline{SS}$ pin puts the MISO pin in a high-impedance state.

When enabled, the SPI controls data direction of the MISO pin regardless of the state of the data direction register of the shared I/O port.

16.11.2 MOSI (Master Out/Slave In)

MOSI is one of the two SPI module pins that transmits serial data. In full-duplex operation, the MOSI pin of the master SPI module is connected to the MOSI pin of the slave SPI module. The master SPI simultaneously transmits data from its MOSI pin and receives data on its MISO pin.

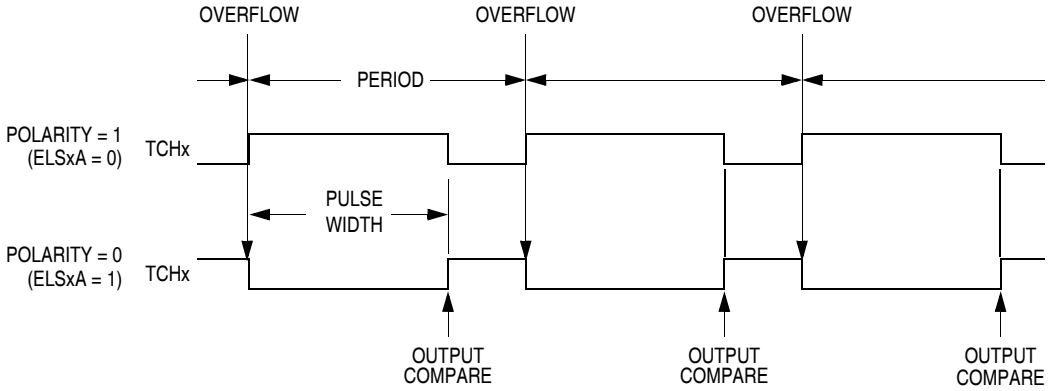

Figure 18-4. PWM Period and Pulse Width

18.3.4.1 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in 18.3.4 Pulse Width Modulation (PWM). The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the old value currently in the TIM1 channel registers.

An unsynchronized write to the TIM1 channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIM1 overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIM1 may pass the new value before it is written to the timer channel (T1CHxH:T1CHxL) registers.

Use the following methods to synchronize unbuffered changes in the PWM pulse width on channel x:

- When changing to a shorter pulse width, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current pulse. The interrupt routine has until the end of the PWM period to write the new value.
- When changing to a longer pulse width, enable TIM1 overflow interrupts and write the new value in the TIM1 overflow interrupt routine. The TIM1 overflow interrupt occurs at the end of the current PWM period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same PWM period.

NOTE

In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare also can cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.

Writing to the TIM2 channel 5 registers enables the TIM2 channel 5 registers to synchronously control the output after the TIM2 overflows. At each subsequent overflow, the TIM2 channel registers (4 or 5) that control the output are the ones written to last. T2SC4 controls and monitors the buffered output compare function, and TIM2 channel 5 status and control register (T2SC5) is unused. While the MS4B bit is set, the channel 5 pin, T2CH5, is available as a general-purpose I/O pin.

NOTE

In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.

19.3.4 Pulse Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM2 can generate a PWM signal. The value in the TIM2 counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM2 counter modulo registers. The time between overflows is the period of the PWM signal.

As Figure 19-4 shows, the output compare value in the TIM2 channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM2 to clear the channel pin on output compare if the polarity of the PWM pulse is 1 (ELSxA = 0). Program the TIM2 to set the pin if the polarity of the PWM pulse is 0 (ELSxA = 1).

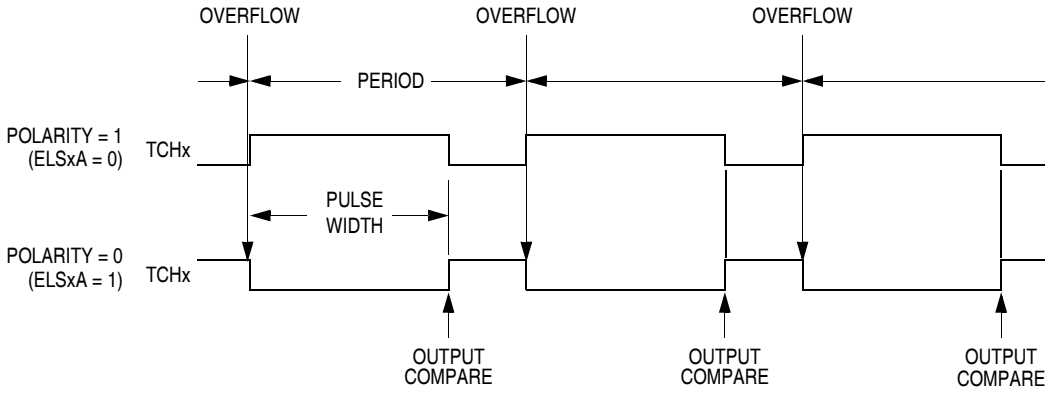

Figure 19-4. PWM Period and Pulse Width

The value in the TIM2 counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing $00FF (255) to the TIM2 counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is 000 (see 19.8.1 TIM2 Status and Control Register).

The value in the TIM2 channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing $0080 (128) to the TIM2 channel registers produces a duty cycle of 128/256 or 50%.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM2 channel 0 registers (T2CH0H:T2CH0L) initially control the buffered PWM output. TIM2 status control register 0 (T2SC0) controls and monitors the PWM signal from the linked channels. MS0B takes priority over MS0A.

Setting MS2B links channels 2 and 3 and configures them for buffered PWM operation. The TIM2 channel 2 registers (T2CH2H:T2CH2L) initially control the buffered PWM output. TIM2 status control register 2 (T2SC2) controls and monitors the PWM signal from the linked channels. MS2B takes priority over MS2A.

Setting MS4B links channels 4 and 5 and configures them for buffered PWM operation. The TIM2 channel 4 registers (T2CH4H:T2CH4L) initially control the buffered PWM output. TIM2 status control register 4 (T2SC4) controls and monitors the PWM signal from the linked channels. MS4B takes priority over MS4A.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM2 overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0% duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and setting the TOVx bit generates a 100% duty cycle output. (See 19.8.4 TIM2 Channel Status and Control Registers.)

19.4 Interrupts

The following TIM2 sources can generate interrupt requests:

- TIM2 overflow flag (TOF) — The TOF bit is set when the TIM2 counter reaches the modulo value programmed in the TIM2 counter modulo registers. The TIM2 overflow interrupt enable bit, TOIE, enables TIM2 overflow interrupt requests. TOF and TOIE are in the TIM2 status and control register.
- TIM2 channel flags (CH5F:CH0F) — The CHxF bit is set when an input capture or output compare occurs on channel x. Channel x TIM2 CPU interrupt requests are controlled by the channel x interrupt enable bit, CHxIE.

19.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power standby modes.

19.5.1 Wait Mode

The TIM2 remains active after the execution of a WAIT instruction. In wait mode, the TIM2 registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM2 can bring the MCU out of wait mode.

If TIM2 functions are not required during wait mode, reduce power consumption by stopping the TIM2 before executing the WAIT instruction.

19.5.2 Stop Mode

The TIM2 is inactive after the execution of a STOP instruction. The STOP instruction does not affect register conditions or the state of the TIM2 counter. TIM2 operation resumes when the MCU exits stop mode.

19.8.3 TIM2 Counter Modulo Registers

The read/write TIM2 modulo registers contain the modulo value for the TIM2 counter. When the TIM2 counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM2 counter resumes counting from $0000 at the next timer clock. Writing to the high byte (T2MODH) inhibits the TOF bit and overflow interrupts until the low byte (T2MODL) is written. Reset sets the TIM2 counter modulo registers.

Address: $002E T2MODH

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
Reset:	1	1	1	1	1	1	1	1

Address: $002F T2MODL

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	1	1	1	1	1	1	1	1

Figure 19-7. TIM2 Counter Modulo Registers (T2MODH and T2MODL)

NOTE

Reset the TIM2 counter before writing to the TIM2 counter modulo registers.

19.8.4 TIM2 Channel Status and Control Registers

Each of the TIM2 channel status and control registers:

- Flags input captures and output compares
- Enables input capture and output compare interrupts
- Selects input capture, output compare, or PWM operation
- Selects high, low, or toggling output on output compare
- Selects rising edge, falling edge, or any edge as the active input capture trigger
- Selects output toggling on TIM2 overflow
- Selects 0% and 100% PWM duty cycle
- Selects buffered or unbuffered output compare/PWM operation

Address: $0030 T2SC0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 19-8. TIM2 Channel Status and Control Registers (T2SC0:T2SC5)

21.9.3 CGM Acquisition/Lock Time Information

Characteristic	Symbol	Min	Typ	Max	Unit
Acquisition mode entry frequency tolerance(1)	Δ_{ACQ}	± 3.6	—	± 7.2	%
Tracking mode entry frequency tolerance(2)	Δ_{TRK}	0	—	± 3.6	%
LOCK entry frequency tolerance(3)	Δ_{LOCK}	0	—	± 0.9	%
LOCK exit frequency tolerance(4)	Δ_{UNL}	± 0.9	—	± 1.8	%
Reference cycles per acquisition mode period	n_{ACQ}	—	32	—	
Reference cycles per tracking mode period	n_{TRK}	—	128	—	
Automatic mode time to stable	t_{ACQ}	n_{ACQ}/f_{RCLK}	See note(5)	—	s
Automatic stable to lock time	t_{AL}	n_{TRK}/f_{RCLK}	See note(6)	—	s
Automatic lock time ($t_{ACQ} + t_{AL}$)(7)	t_{LOCK}	—	5	25	ms
PLL jitter, deviation of average bus frequency over 2 ms period	f_J	0	—	f_{RCLK} x 0.025% x N/4	Hz

1. Deviation between VCO frequency and desired frequency to enter PLL acquisition mode.
2. Deviation between VCO frequency and desired frequency to enter PLL tracking mode (stable).
3. Deviation between VCO frequency and desired frequency to enter locked mode.
4. Deviation between VCO frequency and desired frequency to exit locked mode.
5. Acquisition time is an integer multiple of reference cycles divided by reference clock.
6. Stable to lock time is an integer multiple of reference cycles divided by reference clock.
7. Maximum lock time depends on CGMXFC filter components, power supply filtering, and reference clock stability. PLL may not lock if improper components or poor filtering and layout are used.

21.15 Memory Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	—	V
FLASH program bus clock frequency	—	1	—	—	MHz
FLASH read bus clock frequency	f_{Read} (1)	0	—	8 M	Hz
FLASH page erase time <1 k cycles >1 k cycles	t_{Erase}	 0.9 3.6	 1 4	 1.1 5.5	ms
FLASH mass erase time	t_{MErase}	4	—	—	ms
FLASH PGM/ERASE to HVEN setup time	t_{NVS}	10	—	—	µs
FLASH high-voltage hold time	t_{NVH}	5	—	—	µs
FLASH high-voltage hold time (mass erase)	t_{NVHL}	100	—	—	µs
FLASH program hold time	t_{PGS}	5	—	—	µs
FLASH program time	t_{PROG}	30	—	40	µs
FLASH return to read time	t_{RCV} (2)	1	—	—	µs
FLASH cumulative program HV period	t_{HV} (3)	—	—	4	ms
FLASH endurance(4)	—	10 k	100 k	—	Cycles
FLASH data retention time(5)	—	15	100	—	Years

1. f_{Read} is defined as the frequency range for which the FLASH memory can be read.
2. t_{RCV} is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to 0.
3. t_{HV} is defined as the cumulative high voltage programming time to the same row before next erase. t_{HV} must satisfy this condition: $t_{NVS} + t_{NVH} + t_{PGS} + (t_{PROG} \times 32) \leq t_{HV}$ maximum.
4. Typical endurance was evaluated for this product family. For additional information on how Freescale defines *Typical Endurance*, please refer to Engineering Bulletin EB619.
5. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines *Typical Data Retention*, please refer to Engineering Bulletin EB618.

Chapter 22
Ordering Information and Mechanical Specifications

22.1 Introduction

This section contains ordering numbers for the MC68HC908GZ60 and gives the dimensions for:

- 32-pin low-profile quad flat pack (case 873A)
- 48-pin low-profile quad flat pack (case 932-03)
- 64-pin quad flat pack (case 840B)

The following figures show the latest package drawings at the time of this publication. To make sure that you have the latest package specifications, contact your local Freescale Sales Office.

22.2 MC Order Numbers

Table 22-1. MC Order Numbers

MC Order Number	Operating Temperature Range	Package
MC908GZ60CFJ	–40°C to +85°C	32-pin low-profile quad flat package (LQFP)
MC908GZ60VFJ	–40°C to +105°C	
MC908GZ60MFJ	–40°C to +125°C	
MC908GZ60CFA	–40°C to +85°C	48-pin low-profile quad flat package (LQFP)
MC908GZ60VFA	–40°C to +105°C	
MC908GZ60MFA	–40°C to +125°C	
MC908GZ60CFU	–40°C to +85°C	64-pin quad flat package (QFP)
MC908GZ60VFU	–40°C to +105°C	
MC908GZ60MFU	–40°C to +125°C	

Temperature designators:
C = –40°C to +85°C
V = –40°C to +105°C
M = –40°C to +125°C

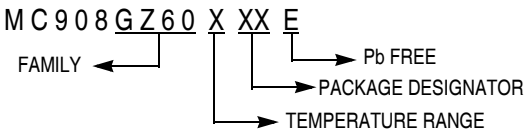

Figure 22-1. Device Numbering System

22.3 Package Dimensions

Refer to the following pages for detailed package dimensions.