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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gz32mfae

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Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$FF80	FLASH-1 Block Protect Register (FL1BPR) ⁽¹⁾ See page 47.	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Write:								
		Reset:	Unaffected by reset							
\$FF81	FLASH-2 Block Protect Register (FL2BPR) ⁽¹⁾ See page 54.	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Write:								
		Reset:	Unaffected by reset							
1. Non-volatile FLASH register										
\$FF88	FLASH-1 Control Register (FL1CR) See page 46.	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$FFFF	COP Control Register (COPCTL) See page 97.	Read:	Low byte of reset vector							
		Write:	Writing clears COP counter (any value)							
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 9 of 9)

Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
Lowest 	IF24	\$FFCC	TIM2 Channel 5 Vector (High)
		\$FFCD	TIM2 Channel 5 Vector (Low)
	IF23	\$FFCE	TIM2 Channel 4 Vector (High)
		\$FFCF	TIM2 Channel 4 Vector (Low)
	IF22	\$FFD0	TIM2 Channel 3 Vector (High)
		\$FFD1	TIM2 Channel 3 Vector (Low)
	IF21	\$FFD2	TIM2 Channel 2 Vector (High)
		\$FFD3	TIM2 Channel 2 Vector (Low)
	IF20	\$FFD4	MSCAN08 Transmit Vector (High)
		\$FFD5	MSCAN08 Transmit Vector (Low)
	IF19	\$FFD6	MSCAN08 Receive Vector (High)
		\$FFD7	MSCAN08 Receive Vector (Low)
	IF18	\$FFD8	MSCAN08 Error Vector (High)
		\$FFD9	MSCAN08 Error Vector (Low)
	IF17	\$FFDA	MSCAN08 Wakeup Vector (High)
		\$FFDB	MSCAN08 Wakeup Vector (Low)
IF16	\$FFDC	Timebase Vector (High)	
	\$FFDD	Timebase Vector (Low)	

2.6.2.2 FLASH-1 Block Protect Register

The FLASH-1 block protect register (FL1BPR) is implemented as a byte within the FLASH-1 memory; therefore, it can only be written during a FLASH programming sequence. The value in this register determines the starting location of the protected range within the FLASH-1 memory.



Figure 2-4. FLASH-1 Block Protect Register (FL1BPR)

FL1BPR[7:0] — Block Protect Register Bits 7 to 0

These eight bits represent bits [14:7] of a 16-bit memory address. Bit 15 is a 1 and bits [6:0] are 0s.

The resultant 16-bit address is used for specifying the start address of the FLASH-1 memory for block protection. FLASH-1 is protected from this start address to the end of FLASH-1 memory at \$FFFF. With this mechanism, the protect start address can be \$XX00 and \$XX80 (128 byte page boundaries) within the FLASH-1 array.

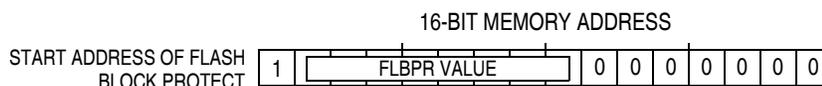


Figure 2-5. FLASH-1 Block Protect Start Address

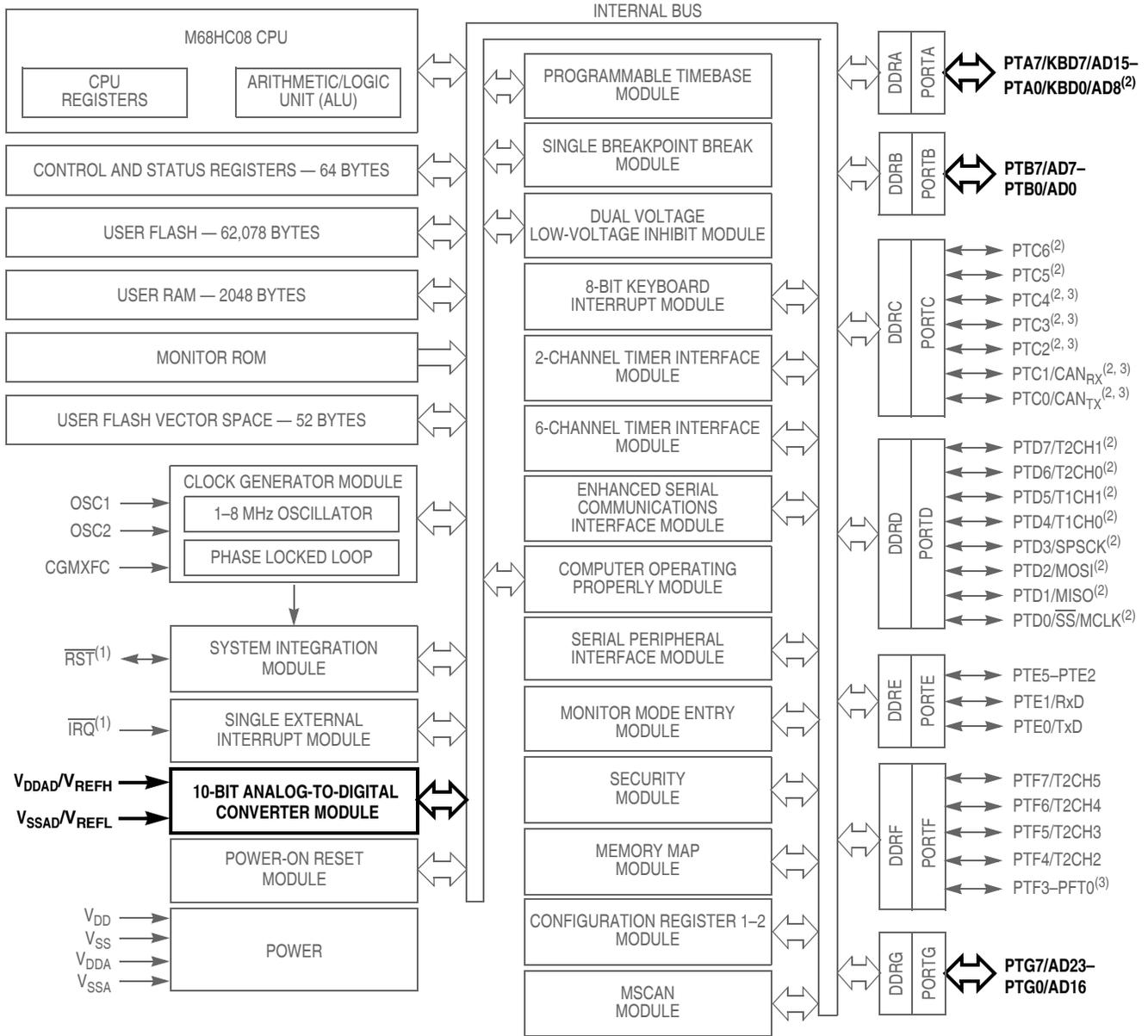
Table 2-2. FLASH-1 Protected Ranges

FL1BPR[7:0]	Protected Range
\$FF	No protection
\$FE	\$FF00–\$FFFF
\$FD	\$FE80–\$FFFF
↓	↓
\$0B	\$8580–\$FFFF
\$0A	\$8500–\$FFFF
\$09	\$8480–\$FFFF
\$08	\$8400–\$FFFF
↓	↓
\$04	\$8200–\$FFFF
\$03	\$8180–\$FFFF
\$02	\$8100–\$FFFF
\$01	\$8080–\$FFFF
\$00	\$8000–\$FFFF

Decreasing the value in FL1BPR by one increases the protected range by one page (128 bytes). However, programming the block protect register with \$FE protects a range twice that size, 256 bytes, in the corresponding array. \$FE means that locations \$FF00–\$FFFF are protected in FLASH-1.

The FLASH memory does not exist at some locations. The block protection range configuration is unaffected if FLASH memory does not exist in that range. Refer to Figure 2-1 and make sure that the desired locations are protected.

Analog-to-Digital Converter (ADC)



1. Pin contains integrated pullup device.

2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.

3. Higher current drive port pins

Figure 3-1. Block Diagram Highlighting ADC Block and Pins

3.7.3 ADC Voltage Reference High Pin (V_{REFH})

The ADC analog portion uses V_{REFH} as its upper voltage reference pin. By default, connect the V_{REFH} pin to the same voltage potential as V_{DD} . External filtering is often necessary to ensure a clean V_{REFH} for good results. Any noise present on this pin will be reflected and possibly magnified in A/D conversion values.

NOTE

For maximum noise immunity, route V_{REFH} carefully and place bypass capacitors as close as possible to the package. Routing V_{REFH} close and parallel to V_{REFL} may improve common mode noise rejection.

V_{DDAD} and V_{REFH} are bonded internally.

3.7.4 ADC Voltage Reference Low Pin (V_{REFL})

The ADC analog portion uses V_{REFL} as its lower voltage reference pin. By default, connect the V_{REFL} pin to the same voltage potential as V_{SS} . External filtering is often necessary to ensure a clean V_{REFL} for good results. Any noise present on this pin will be reflected and possibly magnified in A/D conversion values.

NOTE

For maximum noise immunity, route V_{REFL} carefully and, if not connected to V_{SS} , place bypass capacitors as close as possible to the package. Routing V_{REFH} close and parallel to V_{REFL} may improve common mode noise rejection.

V_{SSAD} and V_{REFL} are bonded internally.

3.7.5 ADC Voltage In (V_{ADIN})

V_{ADIN} is the input voltage signal from one of the 24 ADC channels to the ADC module.

3.8 I/O Registers

These I/O registers control and monitor ADC operation:

- ADC status and control register (ADSCR)
- ADC data register (ADRH and ADRL)
- ADC clock register (ADCLK)

4.3.1 Crystal Oscillator Circuit

The crystal oscillator circuit consists of an inverting amplifier and an external crystal. The OSC1 pin is the input to the amplifier and the OSC2 pin is the output. The SIMOSCEN signal from the system integration module (SIM) or the OSCENINSTOP bit in the CONFIG register enable the crystal oscillator circuit.

The CGMXCLK signal is the output of the crystal oscillator circuit and runs at a rate equal to the crystal frequency. CGMXCLK is then buffered to produce CGMRCLK, the PLL reference clock.

CGMXCLK can be used by other modules which require precise timing for operation. The duty cycle of CGMXCLK is not guaranteed to be 50% and depends on external factors, including the crystal and related external components. An externally generated clock also can feed the OSC1 pin of the crystal oscillator circuit. Connect the external clock to the OSC1 pin and let the OSC2 pin float.

4.3.2 Phase-Locked Loop Circuit (PLL)

The PLL is a frequency generator that can operate in either acquisition mode or tracking mode, depending on the accuracy of the output frequency. The PLL can change between acquisition and tracking modes either automatically or manually.

4.3.3 PLL Circuits

The PLL consists of these circuits:

- Voltage-controlled oscillator (VCO)
- Modulo VCO frequency divider
- Phase detector
- Loop filter
- Lock detector

The operating range of the VCO is programmable for a wide range of frequencies and for maximum immunity to external noise, including supply and CGMXFC noise. The VCO frequency is bound to a range from roughly one-half to twice the center-of-range frequency, f_{VRS} . Modulating the voltage on the CGMXFC pin changes the frequency within this range. By design, f_{VRS} is equal to the nominal center-of-range frequency, f_{NOM} , (71.4 kHz) times a linear factor, L , and a power-of-two factor, E , or $(L \times 2^E)f_{NOM}$.

CGMRCLK is the PLL reference clock, a buffered version of CGMXCLK. CGMRCLK runs at a frequency, f_{RCLK} . The VCO's output clock, CGMVCLK, running at a frequency, f_{VCLK} , is fed back through a programmable modulo divider. The modulo divider reduces the VCO clock by a factor, N . The divider's output is the VCO feedback clock, CGMVDV, running at a frequency, $f_{VDV} = f_{VCLK}/(N)$. (For more information, see 4.3.6 Programming the PLL.)

The phase detector then compares the VCO feedback clock, CGMVDV, with the final reference clock, CGMRDV. A correction pulse is generated based on the phase difference between the two signals. The loop filter then slightly alters the DC voltage on the external capacitor connected to CGMXFC based on the width and direction of the correction pulse. The filter can make fast or slow corrections depending on its mode, described in 4.3.4 Acquisition and Tracking Modes. The value of the external capacitor and the reference frequency determines the speed of the corrections and the stability of the PLL.

The lock detector compares the frequencies of the VCO feedback clock, CGMVDV, and the reference clock, CGMRCLK. Therefore, the speed of the lock detector is directly proportional to the reference

MSCAN08 Controller (MSCAN08)

Addr.	Register		Bit 7	6	5	4	3	2	1	Bit 0
\$0514	CIDMR0	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0515	CIDMR1	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0516	CIDMR2	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
\$0517	CIDMR3	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								

= Unimplemented
 R = Reserved

Figure 12-15. MSCAN08 Control Register Structure (Continued)

12.13.1 MSCAN08 Module Control Register 0

Address: \$0500

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	SYNCH	TLNKEN	SLPAK	SLPRQ	SFTRES
Write:								
Reset:	0	0	0	0	0	0	0	1

= Unimplemented

Figure 12-16. Module Control Register 0 (CMCR0)

SYNCH — Synchronized Status

This bit indicates whether the MSCAN08 is synchronized to the CAN bus and as such can participate in the communication process.

- 1 = MSCAN08 synchronized to the CAN bus
- 0 = MSCAN08 not synchronized to the CAN bus

TLNKEN — Timer Enable

This flag is used to establish a link between the MSCAN08 and the on-chip timer (see 12.9 Timer Link).

- 1 = The MSCAN08 timer signal output is connected to the timer input.
- 0 = The port is connected to the timer input.

SLPAK — Sleep Mode Acknowledge

This flag indicates whether the MSCAN08 is in module internal sleep mode. It shall be used as a handshake for the sleep mode request (see 12.8.1 MSCAN08 Sleep Mode). If the MSCAN08 detects bus activity while in sleep mode, it clears the flag.

- 1 = Sleep – MSCAN08 in internal sleep mode
- 0 = Wakeup – MSCAN08 is not in sleep mode

SLPRQ — Sleep Request, Go to Internal Sleep Mode

This flag requests the MSCAN08 to go into an internal power-saving mode (see 12.8.1 MSCAN08 Sleep Mode).

- 1 = Sleep — The MSCAN08 will go into internal sleep mode.
- 0 = Wakeup — The MSCAN08 will function normally.

IDAM2–IDAM0— Identifier Acceptance Mode

The CPU sets these flags to define the identifier acceptance filter organization (see 12.5 Identifier Acceptance Filter). Table 12-9 summarizes the different settings. In “filter closed” mode no messages will be accepted so that the foreground buffer will never be reloaded.

Table 12-9. Identifier Acceptance Mode Settings

IDAM2	IDAM1	IDAM0	Identifier Acceptance Mode
0	0	0	Single 32-bit acceptance filter
0	0	1	Two 16-bit acceptance filter
0	1	0	Four 8-bit acceptance filters
0	1	1	Filter closed
1	X	X	Reserved

IDHIT2–IDHIT0— Identifier Acceptance Hit Indicator

The MSCAN08 sets these flags to indicate an identifier acceptance hit (see 12.5 Identifier Acceptance Filter). Table 12-10 summarizes the different settings.

Table 12-10. Identifier Acceptance Hit Indication

IDHIT2	IDHIT1	IDHIT0	Identifier Acceptance Hit
0	0	0	Filter 0 hit
0	0	1	Filter 1 hit
0	1	0	Filter 2 hit
0	1	1	Filter 3 hit
1	X	X	Reserved

The IDHIT indicators are always related to the message in the foreground buffer. When a message gets copied from the background to the foreground buffer, the indicators are updated as well.

NOTE

The CIDAC register can be written only if the SFTRES bit in the CMCR0 is set.

12.13.10 MSCAN08 Receive Error Counter



Figure 12-25. Receiver Error Counter (CRXERR)

This read-only register reflects the status of the MSCAN08 receive error counter.

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 14-3 summarizes the results of the data bit samples.

Table 14-3. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit.

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 14-4 summarizes the results of the stop bit samples.

Table 14-4. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

14.4.3.4 Framing Errors

If the data recovery logic does not detect a 1 where the stop bit should be in an incoming character, it sets the framing error bit, FE, in SCS1. A break character also sets the FE bit because a break character has no stop bit. The FE bit is set at the same time that the SCRF bit is set.

14.5.2 Stop Mode

The ESCI module is inactive in stop mode. The STOP instruction does not affect ESCI register states. ESCI module operation resumes after the MCU exits stop mode.

Because the internal clock is inactive during stop mode, entering stop mode during an ESCI transmission or reception results in invalid data.

14.6 ESCI During Break Module Interrupts

The BCFE bit in the break flag control register (SBFCR) enables software to clear status bits during the break state. See 20.2 Break Module (BRK).

To allow software to clear status bits during a break interrupt, write a 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at 0. After the break, doing the second step clears the status bit.

14.7 I/O Signals

Port E shares two of its pins with the ESCI module. The two ESCI I/O pins are:

- PTE0/TxD — transmit data
- PTE1/RxD — receive data

14.7.1 PTE0/TxD (Transmit Data)

The PTE0/TxD pin is the serial data output from the ESCI transmitter. The ESCI shares the PTE0/TxD pin with port E. When the ESCI is enabled, the PTE0/TxD pin is an output regardless of the state of the DDRE0 bit in data direction register E (DDRE).

14.7.2 PTE1/RxD (Receive Data)

The PTE1/RxD pin is the serial data input to the ESCI receiver. The ESCI shares the PTE1/RxD pin with port E. When the ESCI is enabled, the PTE1/RxD pin is an input regardless of the state of the DDRE1 bit in data direction register E (DDRE).

14.8 I/O Registers

These I/O registers control and monitor ESCI operation:

- ESCI control register 1, SCC1
- ESCI control register 2, SCC2
- ESCI control register 3, SCC3
- ESCI status register 1, SCS1
- ESCI status register 2, SCS2
- ESCI data register, SCDR

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- ESCI baud rate register, SCBR
- ESCI prescaler register, SCPSC
- ESCI arbiter control register, SCIACTL
- ESCI arbiter data register, SCIADAT

14.8.1 ESCI Control Register 1

ESCI control register 1 (SCC1):

- Enables loop mode operation
- Enables the ESCI
- Controls output polarity
- Controls character length
- Controls ESCI wakeup method
- Controls idle character detection
- Enables parity function
- Controls parity type

Address: \$0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LOOPS	ENSCI	TXINV	M	WAKE	ILTY	PEN	PTY
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 14-10. ESCI Control Register 1 (SCC1)

LOOPS — Loop Mode Select Bit

This read/write bit enables loop mode operation. In loop mode the RxD pin is disconnected from the ESCI, and the transmitter output goes into the receiver input. Both the transmitter and the receiver must be enabled to use loop mode. Reset clears the LOOPS bit.

- 1 = Loop mode enabled
- 0 = Normal operation enabled

ENSCI — Enable ESCI Bit

This read/write bit enables the ESCI and the ESCI baud rate generator. Clearing ENSCI sets the SCTE and TC bits in ESCI status register 1 and disables transmitter interrupts. Reset clears the ENSCI bit.

- 1 = ESCI enabled
- 0 = ESCI disabled

TXINV — Transmit Inversion Bit

This read/write bit reverses the polarity of transmitted data. Reset clears the TXINV bit.

- 1 = Transmitter output inverted
- 0 = Transmitter output not inverted

NOTE

Setting the TXINV bit inverts all transmitted values including idle, break, start, and stop bits.

IDLE — Receiver Idle Bit

This clearable, read-only bit is set when 10 or 11 consecutive 1s appear on the receiver input. IDLE generates an ESCI receiver CPU interrupt request if the ILIE bit in SCC2 is also set. Clear the IDLE bit by reading SCS1 with IDLE set and then reading the SCDR. After the receiver is enabled, it must receive a valid character that sets the SCRF bit before an idle condition can set the IDLE bit. Also, after the IDLE bit has been cleared, a valid character must again set the SCRF bit before an idle condition can set the IDLE bit. Reset clears the IDLE bit.

- 1 = Receiver input idle
- 0 = Receiver input active (or idle since the IDLE bit was cleared)

OR — Receiver Overrun Bit

This clearable, read-only bit is set when software fails to read the SCDR before the receive shift register receives the next character. The OR bit generates an ESCI error CPU interrupt request if the ORIE bit in SCC3 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading SCS1 with OR set and then reading the SCDR. Reset clears the OR bit.

- 1 = Receive shift register full and SCRF = 1
- 0 = No receiver overrun

Software latency may allow an overrun to occur between reads of SCS1 and SCDR in the flag-clearing sequence. Figure 14-14 shows the normal flag-clearing sequence and an example of an overrun caused by a delayed flag-clearing sequence. The delayed read of SCDR does not clear the OR bit because OR was not set when SCS1 was read. Byte 2 caused the overrun and is lost. The next flag-clearing sequence reads byte 3 in the SCDR instead of byte 2.

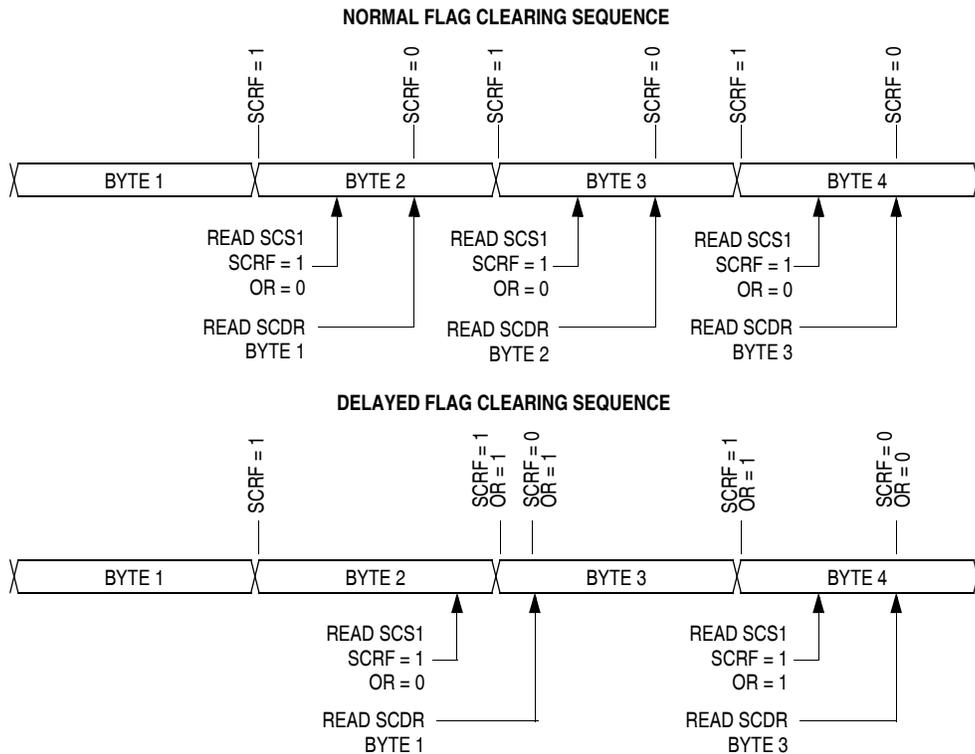


Figure 14-14. Flag Clearing Sequence

15.5.2 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

15.5.3 Break Interrupts

The break module can stop normal program flow at a software-programmable break point by asserting its break interrupt output (see Chapter 18 Timer Interface Module (TIM1) and Chapter 19 Timer Interface Module (TIM2)). The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

15.5.4 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the SIM break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

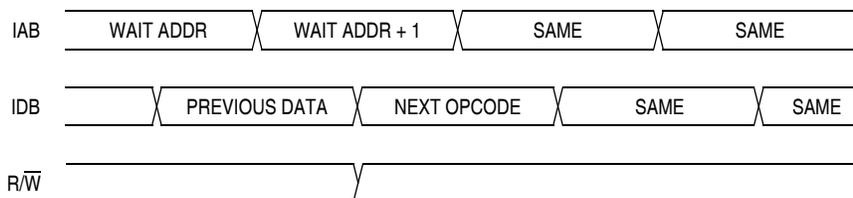
Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a 2-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

15.6 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described in the following subsections. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

15.6.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. Figure 15-16 shows the timing for wait mode entry.



Note: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 15-16. Wait Mode Entry Timing

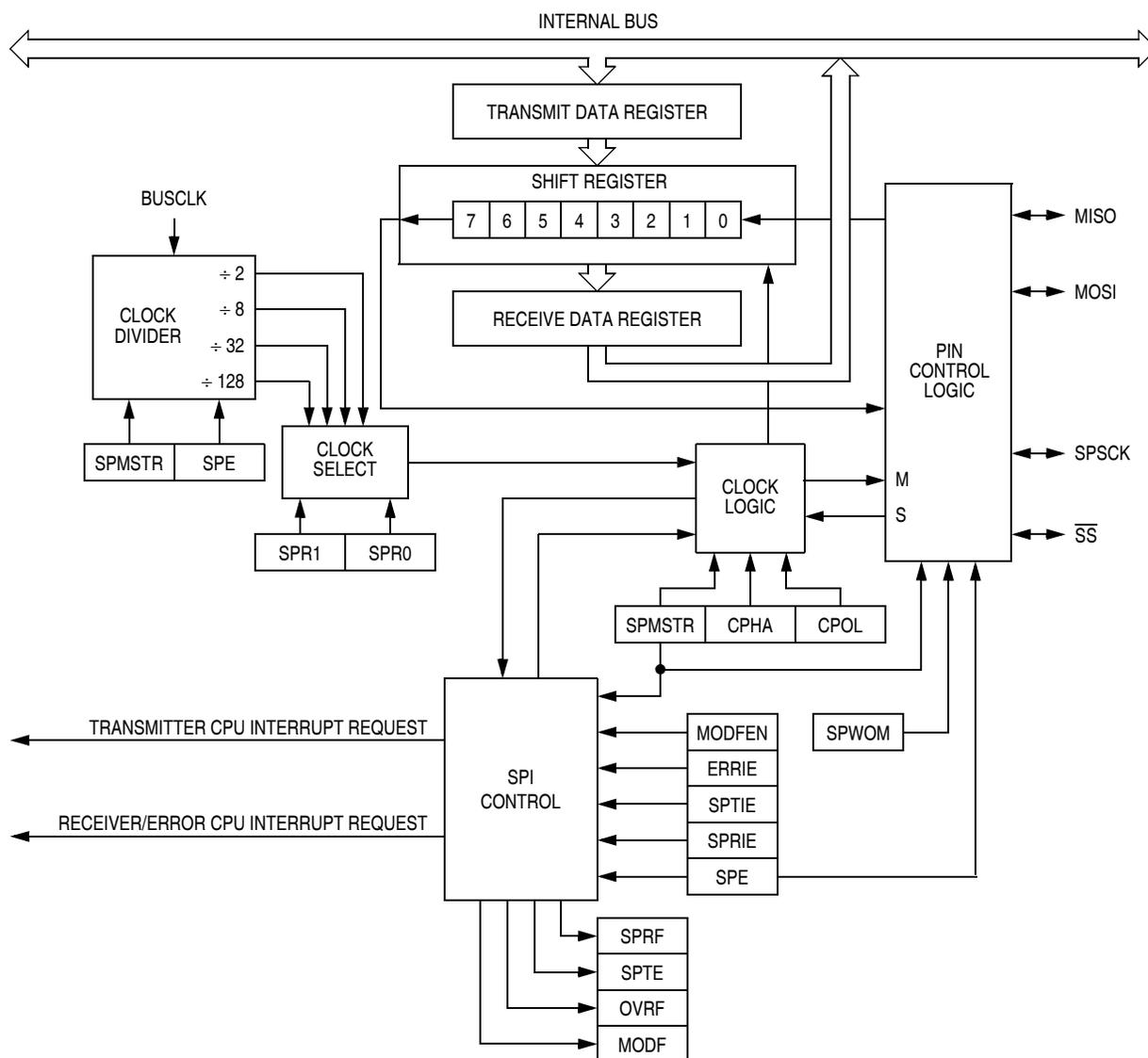


Figure 16-2. SPI Module Block Diagram

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$0010	SPI Control Register (SPCR) See page 255.	Read:	SPRIE	R	SPMSTR	CPOL	CPHA	SPWOM	SPE	SPTIE
		Write:								
	Reset:	0	0	1	0	1	0	0	0	
\$0011	SPI Status and Control Register (SPSCR) See page 256.	Read:	SPRF	ERRIE	OVRF	MODF	SPTIE	MODFEN	SPR1	SPR0
		Write:								
	Reset:	0	0	0	0	1	0	0	0	
\$0012	SPI Data Register (SPDR) See page 258.	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0
	Reset:	Unaffected by reset								
		R = Reserved		= Unimplemented						

Figure 16-3. SPI I/O Register Summary

pin of the master must be high or must be reconfigured as general-purpose I/O not affecting the SPI. (See 16.6.2 Mode Fault Error.) When CPHA = 1, the master begins driving its MOSI pin on the first SPSCCK edge. Therefore, the slave uses the first SPSCCK edge as a start transmission signal. The \overline{SS} pin can remain low between transmissions. This format may be preferable in systems having only one master and only one slave driving the MISO data line.

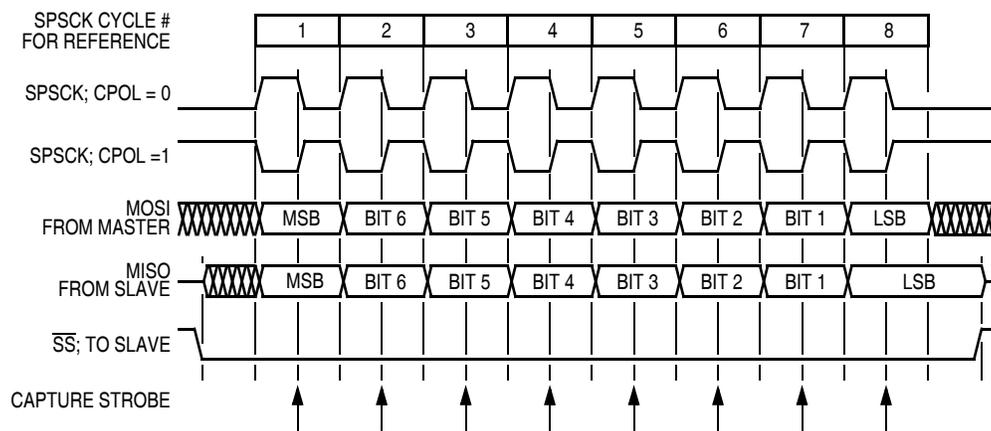


Figure 16-7. Transmission Format (CPHA = 1)

When CPHA = 1 for a slave, the first edge of the SPSCCK indicates the beginning of the transmission. This causes the SPI to leave its idle state and begin driving the MISO pin with the MSB of its data. Once the transmission begins, no new data is allowed into the shift register from the transmit data register. Therefore, the SPI data register of the slave must be loaded with transmit data before the first edge of SPSCCK. Any data written after the first edge is stored in the transmit data register and transferred to the shift register after the current transmission.

16.4.4 Transmission Initiation Latency

When the SPI is configured as a master (SPMSTR = 1), writing to the SPDR starts a transmission. CPHA has no effect on the delay to the start of the transmission, but it does affect the initial state of the SPSCCK signal. When CPHA = 0, the SPSCCK signal remains inactive for the first half of the first SPSCCK cycle. When CPHA = 1, the first SPSCCK cycle begins with an edge on the SPSCCK line from its inactive to its active level. The SPI clock rate (selected by SPR1:SPR0) affects the delay from the write to SPDR and the start of the SPI transmission. (See Figure 16-8.) The internal SPI clock in the master is a free-running derivative of the internal MCU clock. To conserve power, it is enabled only when both the SPE and SPMSTR bits are set. Since the SPI clock is free-running, it is uncertain where the write to the SPDR occurs relative to the slower SPSCCK. This uncertainty causes the variation in the initiation delay shown in Figure 16-8. This delay is no longer than a single SPI bit time. That is, the maximum delay is two MCU bus cycles for DIV2, eight MCU bus cycles for DIV8, 32 MCU bus cycles for DIV32, and 128 MCU bus cycles for DIV128.

Serial Peripheral Interface (SPI) Module

CPOL — Clock Polarity Bit

This read/write bit determines the logic state of the SPSCCK pin between transmissions. (See Figure 16-5 and Figure 16-7.) To transmit data between SPI modules, the SPI modules must have identical CPOL values. Reset clears the CPOL bit.

CPHA — Clock Phase Bit

This read/write bit controls the timing relationship between the serial clock and SPI data. (See Figure 16-5 and Figure 16-7.) To transmit data between SPI modules, the SPI modules must have identical CPHA values. When CPHA = 0, the \overline{SS} pin of the slave SPI module must be high between bytes. (See Figure 16-13.) Reset sets the CPHA bit.

SPWOM — SPI Wired-OR Mode Bit

This read/write bit disables the pullup devices on pins SPSCCK, MOSI, and MISO so that those pins become open-drain outputs.

- 1 = Wired-OR SPSCCK, MOSI, and MISO pins
- 0 = Normal push-pull SPSCCK, MOSI, and MISO pins

SPE — SPI Enable

This read/write bit enables the SPI module. Clearing SPE causes a partial reset of the SPI. (See 16.8 Resetting the SPI.) Reset clears the SPE bit.

- 1 = SPI module enabled
- 0 = SPI module disabled

SPTIE— SPI Transmit Interrupt Enable

This read/write bit enables CPU interrupt requests generated by the SPTIE bit. SPTIE is set when a byte transfers from the transmit data register to the shift register. Reset clears the SPTIE bit.

- 1 = SPTIE CPU interrupt requests enabled
- 0 = SPTIE CPU interrupt requests disabled

16.12.2 SPI Status and Control Register

The SPI status and control register contains flags to signal these conditions:

- Receive data register full
- Failure to clear SPRF bit before next byte is received (overflow error)
- Inconsistent logic level on \overline{SS} pin (mode fault error)
- Transmit data register empty

The SPI status and control register also contains bits that perform these functions:

- Enable error interrupts
- Enable mode fault error detection
- Select master SPI baud rate

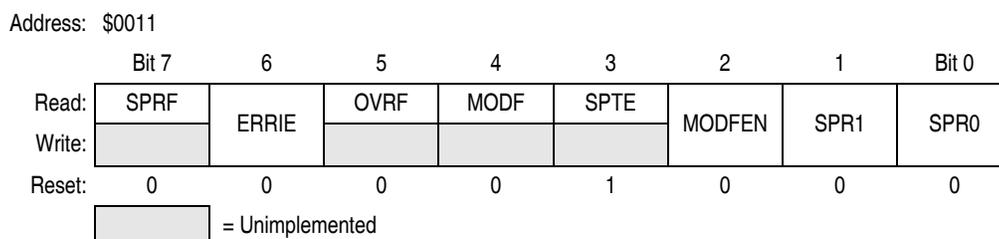


Figure 16-15. SPI Status and Control Register (SPSCR)

18.7 Input/Output Signals

Port D shares two of its pins with the TIM1. The two TIM1 channel I/O pins are PTD4/T1CH0 and PTD5/T1CH1.

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. PTD4/T1CH0 can be configured as a buffered output compare or buffered PWM pin.

18.8 Input/Output Registers

The following I/O registers control and monitor operation of the TIM:

- TIM1 status and control register (T1SC)
- TIM1 counter registers (T1CNTH:T1CNTL)
- TIM1 counter modulo registers (T1MODH:T1MODL)
- TIM1 channel status and control registers (T1SC0 and T1SC1)
- TIM1 channel registers (T1CH0H:T1CH0L and T1CH1H:T1CH1L)

18.8.1 TIM1 Status and Control Register

The TIM1 status and control register (T1SC) does the following:

- Enables TIM1 overflow interrupts
- Flags TIM1 overflows
- Stops the TIM1 counter
- Resets the TIM1 counter
- Prescales the TIM1 counter clock

Address: \$0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

 = Unimplemented

Figure 18-5. TIM1 Status and Control Register (T1SC)

TOF — TIM1 Overflow Flag Bit

This read/write flag is set when the TIM1 counter reaches the modulo value programmed in the TIM1 counter modulo registers. Clear TOF by reading the TIM1 status and control register when TOF is set and then writing a 0 to TOF. If another TIM1 overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

1 = TIM1 counter has reached modulo value

0 = TIM1 counter has not reached modulo value

TOIE — TIM1 Overflow Interrupt Enable Bit

This read/write bit enables TIM1 overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM1 overflow interrupts enabled

0 = TIM1 overflow interrupts disabled

18.8.4 TIM1 Channel Status and Control Registers

Each of the TIM1 channel status and control registers does the following:

- Flags input captures and output compares
- Enables input capture and output compare interrupts
- Selects input capture, output compare, or PWM operation
- Selects high, low, or toggling output on output compare
- Selects rising edge, falling edge, or any edge as the active input capture trigger
- Selects output toggling on TIM1 overflow
- Selects 0% and 100% PWM duty cycle
- Selects buffered or unbuffered output compare/PWM operation

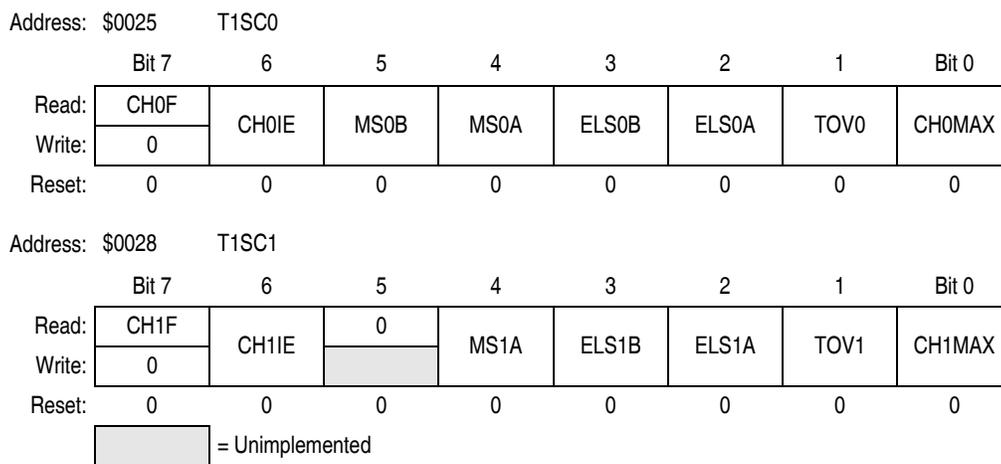


Figure 18-8. TIM1 Channel Status and Control Registers (T1SC0:T1SC1)

CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM1 counter registers matches the value in the TIM1 channel x registers.

Clear CHxF by reading the TIM1 channel x status and control register with CHxF set and then writing a 0 to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing 0 to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a 1 to CHxF has no effect.

- 1 = Input capture or output compare on channel x
- 0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM1 CPU interrupt service requests on channel x. Reset clears the CHxIE bit.

- 1 = Channel x CPU interrupt requests enabled
- 0 = Channel x CPU interrupt requests disabled

Electrical Specifications

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Pullup/pulldown resistors (as input only) Ports PTA7/KBD7–PTA0/KBD0, PTC6–PTC0/CAN _{TX} , PTD7/T2CH1–PTD0/ \overline{SS}	R _{PU}	20	45	65	k Ω
Capacitance Ports (as input or output)	C _{Out} C _{In}	— —	— —	12 8	pF
Monitor mode entry voltage	V _{TST}	V _{DD} + 2.5	—	V _{DD} + 4.0	V
Low-voltage inhibit, trip falling voltage	V _{TRIPF}	3.90	4.25	4.50	V
Low-voltage inhibit, trip rising voltage	V _{TRIPR}	4.0	4.35	4.60	V
Low-voltage inhibit reset/recover hysteresis (V _{TRIPF} + V _{HYS} = V _{TRIPR})	V _{HYS}	—	100	—	mV
POR rearm voltage ⁽¹²⁾	V _{POR}	0	—	100	mV
POR reset voltage ⁽¹³⁾	V _{PORRST}	0	700	800	mV
POR rise time ramp rate ⁽¹⁴⁾	R _{POR}	0.035	—	—	V/ms

- V_{DD} = 5.0 Vdc \pm 10%, V_{SS} = 0 Vdc, T_A = T_A (min) to T_A (max), unless otherwise noted
- Typical values reflect average measurements at midpoint of voltage range, 25°C only.
- Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 32 MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
- Wait I_{DD} measured using external square wave clock source (f_{OSC} = 32 MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait I_{DD}. Measured with CGM and LVI enabled.
- Stop I_{DD} is measured with OSC1 = V_{SS}. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Typical values at midpoint of voltage range, 25°C only.
- Stop I_{DD} with TBM enabled is measured using an external square wave clock source (f_{OSC} = 8 MHz). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All inputs configured as inputs.
- This parameter is characterized and not tested on each device.
- All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
- Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
- Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
- Pullups and pulldowns are disabled. Port B leakage is specified in 21.10 5.0-Volt ADC Characteristics.
- Maximum is highest voltage that POR is guaranteed.
- Maximum is highest voltage that POR is possible.
- If minimum V_{DD} is not reached before the internal POR reset is released, \overline{RST} must be driven low externally until minimum V_{DD} is reached.