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NXP USA Inc. - MC908GZ60VFUE Datasheet



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Details

Product Status	Not For New Designs
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	53
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gz60vfue

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2.6.2.2 FLASH-1 Block Protect Register

The FLASH-1 block protect register (FL1BPR) is implemented as a byte within the FLASH-1 memory; therefore, it can only be written during a FLASH programming sequence. The value in this register determines the starting location of the protected range within the FLASH-1 memory.





FL1BPR[7:0] — Block Protect Register Bits 7 to 0

These eight bits represent bits [14:7] of a 16-bit memory address. Bit 15 is a 1 and bits [6:0] are 0s.

The resultant 16-bit address is used for specifying the start address of the FLASH-1 memory for block protection. FLASH-1 is protected from this start address to the end of FLASH-1 memory at \$FFFF. With this mechanism, the protect start address can be \$XX00 and \$XX80 (128 byte page boundaries) within the FLASH-1 array.



Figure 2-5. FLASH-1 Block Protect Start Address

FL1BPR[7:0]	Protected Range
\$FF	No protection
\$FE	\$FF00-\$FFFF
\$FD ↓	\$FE80–\$FFFF ↓
\$0B	\$8580-\$FFFF
\$0A	\$8500-\$FFFF
\$09	\$8480-\$FFFF
\$08 ↓ \$04	\$8400–\$FFFF ↓ \$8200–\$FFFF
\$03	\$8180-\$FFFF
\$02	\$8100-\$FFFF
\$01	\$8080-\$FFFF
\$00	\$8000-\$FFFF

Table 2-2. FLASH-1 Protected Ranges

Decreasing the value in FL1BPR by one increases the protected range by one page (128 bytes). However, programming the block protect register with \$FE protects a range twice that size, 256 bytes, in the corresponding array. \$FE means that locations \$FF00–\$FFFF are protected in FLASH-1.

The FLASH memory does not exist at some locations. The block protection range configuration is unaffected if FLASH memory does not exist in that range. Refer to Figure 2-1 and make sure that the desired locations are protected.



Clock Generator Module (CGM)

4.3.9 CGM External Connections

In its typical configuration, the CGM requires external components. Five of these are for the crystal oscillator and two or four are for the PLL.

The crystal oscillator is normally connected in a Pierce oscillator configuration, as shown in Figure 4-2. Figure 4-2 shows only the logical representation of the internal components and may not represent actual circuitry. The oscillator configuration uses five components:

- Crystal, X₁
- Fixed capacitor, C₁
- Tuning capacitor, C₂ (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_S

The series resistor (R_S) is included in the diagram to follow strict Pierce oscillator guidelines. Refer to the crystal manufacturer's data for more information regarding values for C1 and C2.

Figure 4-2 also shows the external components for the PLL:

- Bypass capacitor, C_{BYP}
- Filter network

Routing should be done with great care to minimize signal cross talk and noise.



Note: Filter network in box can be replaced with a single capacitor, but will degrade stability.

Figure 4-2. CGM External Connections



Clock Generator Module (CGM)

External factors, however, can cause drastic changes in the operation of the PLL. These factors include noise injected into the PLL through the filter capacitor, filter capacitor leakage, stray impedances on the circuit board, and even humidity or circuit board contamination.

4.8.3 Choosing a Filter

As described in 4.8.2 Parametric Influences on Reaction Time, the external filter network is critical to the stability and reaction time of the PLL. The PLL is also dependent on reference frequency and supply voltage.

Figure 4-9 shows two types of filter circuits. In low-cost applications, where stability and reaction time of the PLL are not critical, the three component filter network shown in Figure 4-9 (B) can be replaced by a single capacitor, C_F, as shown in shown in Figure 4-9 (A). Refer to Table 4-5 for recommended filter components at various reference frequencies. For reference frequencies between the values listed in the table, extrapolate to the nearest common capacitor value. In general, a slightly larger capacitor provides more stability at the expense of increased lock time.



Figure 4-9. PLL Filter

f _{RCLK}	C _{F1}	C _{F2}	R _{F1}	C _F
1 MHz	8.2 nF	820 pF	2k	18 nF
2 MHz	4.7 nF	470 pF	2k	6.8 nF
3 MHz	3.3 nF	330 pF	2k	5.6 nF
4 MHz	2.2 nF	220 pF	2k	4.7 nF
5 MHz	1.8 nF	180 pF	2k	3.9 nF
6 MHz	1.5 nF	150 pF	2k	3.3 nF
7 MHz	1.2 nF	120 pF	2k	2.7 nF
8 MHz	1 nF	100 pF	2k	2.2 nF

Table 4-5. Example Filter Component Values



Computer Operating Properly (COP) Module

The COP counter is a free-running 6-bit counter preceded by the 12-bit SIM counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after 262,128 or 8176 CGMXCLK cycles, depending on the state of the COP rate select bit, COPRS, in the configuration register. With a 262,128 CGMXCLK cycle overflow option, a 4.9152-MHz crystal gives a COP timeout period of 53.3 ms. Writing any value to location \$FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12–5 of the SIM counter.

NOTE

Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.

A COP reset pulls the RST pin low for 32 CGMXCLK cycles and sets the COP bit in the reset status register (RSR).

In monitor mode, the COP is disabled if the \overline{RST} pin or the \overline{IRQ} is held at V_{TST}. During the break state, V_{TST} on the \overline{RST} pin disables the COP.

NOTE

Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.

6.3 I/O Signals

The following paragraphs describe the signals shown in Figure 6-1.

6.3.1 CGMXCLK

CGMXCLK is the crystal oscillator output signal. CGMXCLK frequency is equal to the crystal frequency.

6.3.2 STOP Instruction

The STOP instruction clears the SIM counter.

6.3.3 COPCTL Write

Writing any value to the COP control register (COPCTL) clears the COP counter and clears stages 12–5 of the SIM counter. Reading the COP control register returns the low byte of the reset vector. See 6.4 COP Control Register.

6.3.4 Power-On Reset

The power-on reset (POR) circuit clears the SIM counter 4096 CGMXCLK cycles after power-up.

6.3.5 Internal Reset

An internal reset clears the SIM counter and the COP counter.



Central Processor Unit (CPU)

.

Course					Effect				SS	de	pu	s
Form	Operation	Description						6	ddre ode	bco	pera	/cle
			v	п	•	IN	2	C	Ă	ō	ō	С С
PULA	Pull A from Stack	$SP \leftarrow (SP + 1); Pull (A)$				-	-	-	INH	86		2
	Pull H from Stack	$SP \leftarrow (SP + 1); Pull (H)$	-	-	-	-	-	-		8A		2
PULX	Pull X from Stack	$SP \leftarrow (SP + 1); Pull(X)$	-	-	-	-	-	-		88	44	2
ROLA ROLX ROL <i>opr</i> ,X ROL ,X ROL <i>opr</i> ,SP	Rotate Left through Carry	C ← \to _	ţ	_	_	1	ţ	ţ	INH INH IX1 IX SP1	49 59 69 79 9E69	ff ff	4 1 4 3 5
ROR <i>opr</i> RORA RORX ROR <i>opr</i> ,X ROR ,X ROR <i>opr</i> ,SP	Rotate Right through Carry	b7 b0	ţ	_	_	\$	ţ	ţ	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	$SP \leftarrow \$FF$	-	-	-	-	-	-	INH	9C		1
RTI	Return from Interrupt	$\begin{array}{l} SP \leftarrow (SP) + 1; \ Pull \ (CCR) \\ SP \leftarrow (SP) + 1; \ Pull \ (A) \\ SP \leftarrow (SP) + 1; \ Pull \ (X) \\ SP \leftarrow (SP) + 1; \ Pull \ (PCH) \\ SP \leftarrow (SP) + 1; \ Pull \ (PCL) \end{array}$	t	ţ	ţ	1	ţ	ţ	INH	80		7
RTS	Return from Subroutine	$SP \leftarrow SP + 1$; Pull (PCH) $SP \leftarrow SP + 1$; Pull (PCL)	-	-	-	I	_	-	INH	81		4
SBC #opr SBC opr SBC opr SBC opr,X SBC opr,X SBC ,X SBC opr,SP SBC opr,SP	Subtract with Carry	$A \leftarrow (A) - (M) - (C)$	ţ	_	_	ţ	ţ	ţ	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh II ee ff ff ee ff	23443245
SEC	Set Carry Bit	C ← 1 -		-	-	-	-	1	INH	99		1
SEI	Set Interrupt Mask	upt Mask I ← 1 ·		-	1	-	-	-	INH	9B		2
STA opr STA opr STA opr,X STA opr,X STA op,SP STA opr,SP	Store A in M	M ← (A)		_	_	ţ	ţ	_	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh II ee ff ff ee ff	3443245
STHX opr	Store H:X in M	$(M{:}M+1) \leftarrow (H{:}X)$	0	-	-	1	\$	-	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	$I \leftarrow 0$; Stop Processing		-	0	1	-	-	INH	8E		1
STX opr STX opr STX opr,X STX opr,X STX,X STX,X STX opr,SP STX opr,SP	Store X in M	M ← (X)		_	_	ţ	ţ	_	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh II ee ff ff ee ff	344 324 5
SUB #opr SUB opr SUB opr SUB opr,X SUB opr,X SUB ,X SUB opr,SP SUB opr,SP	Subtract	A ← (A) – (M)	ţ	_	_	ţ	ţ	ţ	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh II ee ff ff ee ff	23443245

Table 7-1.	Instruction	Set Summary	(Sheet 5 of 6)
------------	-------------	-------------	----------------



Low-Power Modes

10.9 Low-Voltage Inhibit Module (LVI)

10.9.1 Wait Mode

If enabled, the low-voltage inhibit (LVI) module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

10.9.2 Stop Mode

If enabled, the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

10.10 Enhanced Serial Communications Interface Module (ESCI)

10.10.1 Wait Mode

The enhanced serial communications interface (ESCI), or SCI module for short, module remains active in wait mode. Any enabled CPU interrupt request from the SCI module can bring the MCU out of wait mode.

If SCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

10.10.2 Stop Mode

The SCI module is inactive in stop mode. The STOP instruction does not affect SCI register states. SCI module operation resumes after the MCU exits stop mode.

Because the internal clock is inactive during stop mode, entering stop mode during an SCI transmission or reception results in invalid data.

10.11 Serial Peripheral Interface Module (SPI)

10.11.1 Wait Mode

The serial peripheral interface (SPI) module remains active in wait mode. Any enabled CPU interrupt request from the SPI module can bring the MCU out of wait mode.

If SPI module functions are not required during wait mode, reduce power consumption by disabling the SPI module before executing the WAIT instruction.

10.11.2 Stop Mode

The SPI module is inactive in stop mode. The STOP instruction does not affect SPI register states. SPI operation resumes after an external interrupt. If stop mode is exited by reset, any transfer in progress is aborted, and the SPI is reset.



10.12 Timer Interface Module (TIM1 and TIM2)

10.12.1 Wait Mode

The timer interface modules (TIM) remain active in wait mode. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

10.12.2 Stop Mode

The TIM is inactive in stop mode. The STOP instruction does not affect register states or the state of the TIM counter. TIM operation resumes when the MCU exits stop mode after an external interrupt.

10.13 Timebase Module (TBM)

10.13.1 Wait Mode

The timebase module (TBM) remains active after execution of the WAIT instruction. In wait mode, the timebase register is not accessible by the CPU.

If the timebase functions are not required during wait mode, reduce the power consumption by stopping the timebase before enabling the WAIT instruction.

10.13.2 Stop Mode

The timebase module may remain active after execution of the STOP instruction if the oscillator has been enabled to operate during stop mode through the OSCENINSTOP bit in the CONFIG2 register. The timebase module can be used in this mode to generate a periodic wakeup from stop mode.

If the oscillator has not been enabled to operate in stop mode, the timebase module will not be active during stop mode. In stop mode, the timebase register is not accessible by the CPU.

If the timebase functions are not required during stop mode, reduce the power consumption by stopping the timebase before enabling the STOP instruction.

10.14 Scalable Controller Area Network Module (MSCAN)

10.14.1 Wait Mode

The scalable controller area network (MSCAN) module remains active after execution of the WAIT instruction. In wait mode, the MSCAN08 registers are not accessible by the CPU.

If the MSCAN08 functions are not required during wait mode, reduce the power consumption by disabling the MSCAN08 module before enabling the WAIT instruction.

10.14.2 Stop Mode

The MSCAN08 module is inactive in stop mode. The STOP instruction does not affect MSCAN08 register states.

Because the internal clock is inactive during stop mode, entering stop mode during an MSCAN08 transmission or reception results in invalid data.

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Freescale Semiconductor



11.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR} . This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF} . V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS} .

11.3.4 LVI Trip Selection

The LVI5OR3 bit in the configuration register selects whether the LVI is configured for 5-V or 3-V protection.

NOTE

The microcontroller is guaranteed to operate at a minimum supply voltage. The trip point (V_{TRIPF} [5 V] or V_{TRIPF} [3 V]) may be lower than this. See Chapter 21 Electrical Specifications for the actual trip point voltages.

11.4 LVI Status Register

The LVI status register (LVISR) indicates if the V_{DD} voltage was detected below the V_{TRIPF} level.

Address:	\$FE0C							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0
		= Unimplem	ented					

Figure 11-3. LVI Status Register (LVISR)

LVIOUT — LVI Output Bit

This read-only flag becomes set when the V_{DD} voltage falls below the V_{TRIPF} trip voltage (see Table 11-1). Reset clears the LVIOUT bit.

V _{DD}	LVIOUT
$V_{DD} > V_{TRIPR}$	0
$V_{DD} < V_{TRIPF}$	1
$V_{TRIPF} < V_{DD} < V_{TRIPR}$	Previous value

Table 11-1. LVIOUT Bit Indication

11.5 LVI Interrupts

The LVI module does not generate interrupt requests.





The above parameters can be set by programming the bus timing registers, CBTR0 and CBTR1. See 12.13.3 MSCAN08 Bus Timing Register 0 and 12.13.4 MSCAN08 Bus Timing Register 1.

NOTE

It is the user's responsibility to make sure that the bit timing settings are in compliance with the CAN standard,

Table 12-8 gives an overview on the CAN conforming segment settings and the related parameter values.



Figure 12-9. Segments Within the Bit Time

Table 12-3. Time Segment Syntax

SYNC_SEG	System expects transitions to occur on the bus during this period.
Transmit point	A node in transmit mode will transfer a new value to the CAN bus at this point.
Sample point	A node in receive mode will sample the bus at this point. If the three samples per bit option is selected then this point marks the position of the third sample.

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchronized Jump Width	SJW
5 10	49	2	1	12	01
4 11	3 10	3	2	13	02
5 12	4 11	4	3	14	03
6 13	5 12	5	4	14	03
7 14	6 13	6	5	14	03
8 15	7 14	7	6	14	03
9 16	8 15	8	7	14	03



AC7–AC0 — Acceptance Code Bits

AC7–AC0 comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

NOTE

The CIDAR0–CIDAR3 registers can be written only if the SFTRES bit in CMCR0 is set

12.13.13 MSCAN08 Identifier Mask Registers (CIDMR0–CIDMR3)

The identifier mask registers specify which of the corresponding bits in the identifier acceptance register are relevant for acceptance filtering. For standard identifiers it is required to program the last three bits (AM2–AM0) in the mask register CIDMR1 to 'don't care'.



Figure 12-28. Identifier Mask Registers (CIDMR0–CIDMR3)

AM7–AM0 — Acceptance Mask Bits

If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match will be detected. The message will be accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register will not affect whether or not the message is accepted.

1 = Ignore corresponding acceptance code register bit.

0 = Match corresponding acceptance code register and identifier bits.

NOTE

The CIDMR0–CIDMR3 registers can be written only if the SFTRES bit in the CMCR0 is set



Chapter 14 Enhanced Serial Communications Interface (ESCI) Module

14.1 Introduction

The enhanced serial communications interface (ESCI) module allows asynchronous communications with peripheral devices and other microcontroller units (MCU).

14.2 Features

Features include:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Programmable baud rates
- Programmable 8-bit or 9-bit character length
- Separately enabled transmitter and receiver
- Separate receiver and transmitter central processor unit (CPU) interrupt requests
- Programmable transmitter output polarity
- Two receiver wakeup methods:
 - Idle line wakeup
 - Address mark wakeup
- Interrupt-driven operation with eight interrupt flags:
 - Transmitter empty
 - Transmission complete
 - Receiver full
 - Idle receiver input
 - Receiver overrun
 - Noise error
 - Framing error
 - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection



Error Conditions

In this case, an overflow can be missed easily. Since no more SPRF interrupts can be generated until this OVRF is serviced, it is not obvious that bytes are being lost as more transmissions are completed. To prevent this, either enable the OVRF interrupt or do another read of the SPSCR following the read of the SPDR. This ensures that the OVRF was not set before the SPRF was cleared and that future transmissions can set the SPRF bit. Figure 16-11 illustrates this process. Generally, to avoid this second SPSCR read, enable the OVRF to the CPU by setting the ERRIE bit.



Figure 16-11. Clearing SPRF When OVRF Interrupt Is Not Enabled

16.6.2 Mode Fault Error

Setting SPMSTR selects master mode and configures the SPSCK and MOSI pins as outputs and the MISO pin as an input. Clearing SPMSTR selects slave mode and configures the SPSCK and MOSI pins as inputs and the MISO pin as an output. The mode fault bit, MODF, becomes set any time the state of the slave select pin, SS, is inconsistent with the mode selected by SPMSTR.

To prevent SPI pin contention and damage to the MCU, a mode fault error occurs if:

- The SS pin of a slave SPI goes high during a transmission
- The SS pin of a master SPI goes low at any time

For the MODF flag to be set, the mode fault error enable bit (MODFEN) must be set. Clearing the MODFEN bit does not clear the MODF flag but does prevent MODF from being set again after MODF is cleared.

MODF generates a receiver/error CPU interrupt request if the error interrupt enable bit (ERRIE) is also set. The SPRF, MODF, and OVRF interrupts share the same CPU interrupt vector. (See Figure 16-12.) It is not possible to enable MODF or OVRF individually to generate a receiver/error CPU interrupt request. However, leaving MODFEN low prevents MODF from being set.



			Divider		
TRD2 TRD1		TRDO	TMBCLKSEL		
TDNZ	IDNI	IDNV	0	1	
0	0	0	32,768	4,194,304	
0	0	1	8192	1,048,576	
0	1	0	2048	262144	
0	1	1	128	16,384	
1	0	0	64	8192	
1	0	1	32	4096	
1	1	0	16	2048	
1	1	1	8	1024	

Table 17-1. Timebase Divider Selection

As an example, a 4.9152 MHz crystal, with the TMBCLKSEL set for divide-by-128 and the TBR2–TBR0 set to {011}, the divider is 16,384 and the interrupt rate calculates to:

 $\frac{16,384}{4.9152 \text{ x } 10^6} = 3.33 \text{ ms}$

NOTE

Do not change TBR2–TBR0 bits while the timebase is enabled (TBON = 1).

17.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power- consumption standby modes.

17.6.1 Wait Mode

The timebase module remains active after execution of the WAIT instruction. In wait mode the timebase register is not accessible by the CPU.

If the timebase functions are not required during wait mode, reduce the power consumption by stopping the timebase before executing the WAIT instruction.

17.6.2 Stop Mode

The timebase module may remain active after execution of the STOP instruction if the oscillator has been enabled to operate during stop mode through the OSCENINSTOP bit in the configuration register. The timebase module can be used in this mode to generate a periodic wakeup from stop mode.

If the oscillator has not been enabled to operate in stop mode, the timebase module will not be active during stop mode. In stop mode, the timebase register is not accessible by the CPU.

If the timebase functions are not required during stop mode, reduce power consumption by disabling the timebase module before executing the STOP instruction.



Functional Description

Use the following methods to synchronize unbuffered changes in the output compare value on channel x:

- When changing to a smaller value, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current output compare pulse. The interrupt routine has until the end of the counter overflow period to write the new value.
- When changing to a larger output compare value, enable TIM1 overflow interrupts and write the new value in the TIM1 overflow interrupt routine. The TIM1 overflow interrupt occurs at the end of the current counter overflow period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same counter overflow period.

18.3.3.2 Buffered Output Compare

Channels 0 and 1 can be linked to form a buffered output compare channel whose output appears on the T1CH0 pin. The TIM1 channel registers of the linked pair alternately control the output.

Setting the MS0B bit in TIM1 channel 0 status and control register (TSC0) links channel 0 and channel 1. The output compare value in the TIM1 channel 0 registers initially controls the output on the T1CH0 pin. Writing to the TIM1 channel 1 registers enables the TIM1 channel 1 registers to synchronously control the output after the TIM1 overflows. At each subsequent overflow, the TIM1 channel registers (0 or 1) that control the output are the ones written to last. T1SC0 controls and monitors the buffered output compare function, and TIM1 channel 1 status and control register (T1SC1) is unused. While the MS0B bit is set, the channel 1 pin, T1CH1, is available as a general-purpose I/O pin.

NOTE

In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.

18.3.4 Pulse Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM1 can generate a PWM signal. The value in the TIM1 counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM1 counter modulo registers. The time between overflows is the period of the PWM signal.

As Figure 18-4 shows, the output compare value in the TIM1 channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM1 to clear the channel pin on output compare if the polarity of the PWM pulse is 1 (ELSxA = 0). Program the TIM1 to set the pin if the polarity of the PWM pulse is 0 (ELSxA = 1).

The value in the TIM1 counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing \$00FF (255) to the TIM1 counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is 000. See 18.8.1 TIM1 Status and Control Register.

The value in the TIM1 channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing \$0080 (128) to the TIM1 channel registers produces a duty cycle of 128/256 or 50%.





20.2.2.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.



Figure 20-4. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a 0 to bit

7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match

0 = Breaks disabled

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a 1 to BRKA generates a break interrupt. Clear BRKA by writing a 0 to it before exiting the break routine. Reset clears the BRKA bit.

1 = Break address match

0 = No break address match

20.2.2.2 Break Address Registers

The break address registers (BRKH and BRKL) contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.







Figure 20-6. Break Address Register Low (BRKL)



21.11 3.3-Volt ADC Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Max	Unit	Comments
Supply voltage	V _{DDAD}	3.0	3.6	V	V_{DDAD} should be tied to the same potential as V_{DD} via separate traces.
Input voltages	V _{ADIN}	0	V _{DDAD}	V	V _{ADIN} <= V _{DDAD}
Resolution	B _{AD}	10	10	Bits	
Absolute accuracy	A _{AD}	-6	+6	LSB	Includes quantization
ADC internal clock	f _{ADIC}	500 k	1.048 M	Hz	$t_{AIC} = 1/f_{ADIC}$
Conversion range	R _{AD}	V _{SSAD}	V _{DDAD}	V	
Power-up time	t _{ADPU}	16	—	t _{AIC} cycles	
Conversion time	t _{ADC}	16	17	t _{AIC} cycles	
Sample time	t _{ADS}	5	—	t _{AIC} cycles	
Monotonicity	M _{AD}	Guaranteed			
Zero input reading	Z _{ADI}	000	005	Hex	$V_{ADIN} = V_{SSA}$
Full-scale reading	F _{ADI}	3FA	3FF	Hex	$V_{ADIN} = V_{DDA}$
Input capacitance	C _{ADI}	—	30	pF	Not tested
V _{DDAD} /V _{REFH} current	I _{VREF}	—	1.2	mA	
Absolute accuracy (8-bit truncation mode)	A _{AD}	-1	+1	LSB	Includes quantization
Quantization error (8-bit truncation mode)	_	-1/8	+7/8	LSB	

1. V_{DD} = 3.3 Vdc \pm 10%, V_{SS} = 0 Vdc, $V_{DDAD/}V_{REFH}$ = 3.3 Vdc \pm 10%, $V_{SSAD/}V_{REFL}$ = 0 Vdc



Chapter 22 Ordering Information and Mechanical Specifications

22.1 Introduction

This section contains ordering numbers for the MC68HC908GZ60 and gives the dimensions for:

- 32-pin low-profile quad flat pack (case 873A)
- 48-pin low-profile quad flat pack (case 932-03)
- 64-pin quad flat pack (case 840B)

The following figures show the latest package drawings at the time of this publication. To make sure that you have the latest package specifications, contact your local Freescale Sales Office.

22.2 MC Order Numbers

MC Order Number	Operating Temperature Range	Package	
MC908GZ60CFJ	–40°C to +85°C	32-pin low-profile	
MC908GZ60VFJ	-40°C to +105°C	quad flat package	
MC908GZ60MFJ	-40°C to +125°C	(LQFP)	
MC908GZ60CFA	-40°C to +85°C	48-pin low-profile	
MC908GZ60VFA	-40°C to +105°C	quad flat package	
MC908GZ60MFA	-40°C to +125°C	(LQFP)	
MC908GZ60CFU	-40°C to +85°C	64-pin quad flat	
MC908GZ60VFU	-40°C to +105°C	package	
MC908GZ60MFU	-40°C to +125°C	(QFP)	

Table 22-1. MC Order Numbers

Temperature designators:

 $C = -40^{\circ}C$ to $+85^{\circ}C$

 $\label{eq:V} \begin{array}{l} \mathsf{V} = -40^\circ \mathsf{C} \mbox{ to } +105^\circ \mathsf{C} \\ \mathsf{M} = -40^\circ \mathsf{C} \mbox{ to } +125^\circ \mathsf{C} \end{array}$



Figure 22-1. Device Numbering System

22.3 Package Dimensions

Refer to the following pages for detailed package dimensions.



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994.

 $\overline{3}$ datums a, b, and d to be determined at datum plane H.

 $\overline{/4.}$ dimensions to be determined at seating plane datum c.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THZ LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

<u>6</u> DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

/7.\ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

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TITLE:	DOCUMENT NO: 98ASH70029A		RE∨: C	
LOW PROFILE QUAD FLAT P,	CASE NUMBER: 873A-04 0		01 APR 2005	
32 LEAD, 0.8 PITCH (7 X 7 X 1.4)		STANDARD: JEDEC MS-026 BBA		



1. Pin contains integrated pullup device.

2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.

3. Higher current drive port pins

Figure B-1. MC68HC908GZ32 Block Diagram