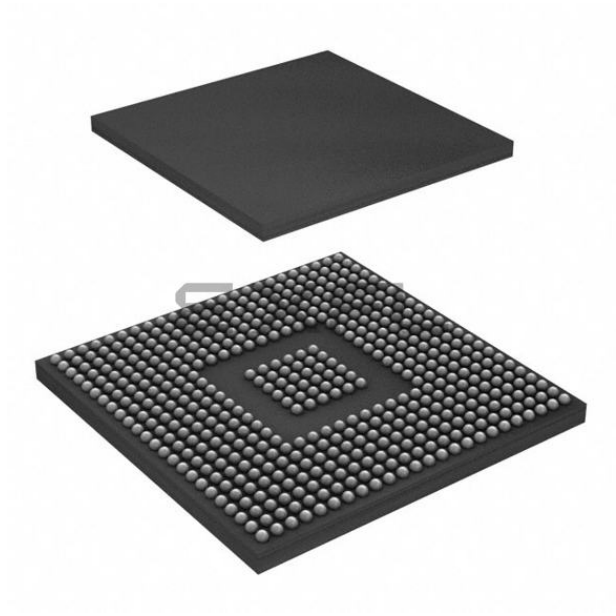

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XCore
Core Size	32-Bit Quad-Core
Speed	400MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	256
Program Memory Size	256KB (64K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	512-LFBGA
Supplier Device Package	512-PBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-g04b-fb512-i4

Table of Contents

1 Features

- **Quad-Tile Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
  - Up to 1600 MIPS shared between up to 32 real-time logical cores
  - Each logical core has:
    - Guaranteed throughput of between 1/4 and 1/8 of tile MIPS
    - 16x32bit dedicated registers
  - 159 high-density 16/32-bit instructions
    - All have single clock-cycle execution (except for divide)
    - 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions
- **Programmable I/O**
  - 256 general-purpose I/O pins, configurable as input or output
  - Port sampling rates of up to 60 MHz with respect to an external clock
  - 128 channel ends for communication with other cores, on or off-chip
- **Memory**
  - 256KB internal single-cycle SRAM (max 64KB per tile) for code and data storage
  - 32KB internal OTP (max 8KB per tile) for application boot code
- **JTAG Module for On-Chip Debug**
- **Security Features**
  - Programming lock disables debug and prevents read-back of memory contents
  - AES bootloader ensures secrecy of IP held on external flash memory
- **Ambient Temperature Range**
  - Commercial qualification: 0 °C to 70 °C
  - Industrial qualification: -40 °C to 85 °C
- **Speed Grade**
  - 400 MHz part: 400 MIPS
- **512-pin PBGA package 0.8 mm pitch**

2 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	IO VDD	IO VDD	X0D61	X0D63	X0D65	VSS	X0D67	X0D69	NC	IO VDD	NC	NC	NC	NC	VSS	NC	X3D69	X3D67	IO VDD	X3D65	X3D63	X3D61	VSS	VSS
B	IO VDD	IO VDD	NC	X0D62	X0D64	VSS	X0D66	X0D68	X0D70	IO VDD	NC	NC	NC	NC	VSS	X3D70	X3D68	X3D66	IO VDD	X3D64	X3D62	NC	VSS	VSS
C	NC	X0D58	IO VDD	X0D37	X0D39	X0D41	VSS	X0D43	NC	NC	IO VDD	NC	NC	VSS	NC	NC	X3D43	IO VDD	X3D41	X3D39	X3D37	VSS	X3D58	NC
D	X0D57	X0D56	X0D35	IO VDD	X0D36	X0D38	X0D40	VSS	X0D42	NC	NC	NC	NC	NC	NC	X3D42	IO VDD	X3D40	X3D38	X3D36	VSS	X3D35	X3D56	X3D57
E	X0D55	X0D54	X0D33	X0D34	IO VDD	X0D13	X0D15	X0D17	VSS	X0D19	X0D21	X0D23	X3D23	X3D21	X3D19	IO VDD	X3D17	X3D15	X3D13	VSS	X3D34	X3D33	X3D54	X3D55
F	VSS	VSS	X0D31	X0D32	X0D11	IO VDD	X0D12	X0D14	X0D16	X0D18	X0D20	X0D22	X3D22	X3D20	X3D18	X3D16	X3D14	X3D12	VSS	X3D11	X3D32	X3D31	IO VDD	IO VDD
G	X0D53	X0D52	VSS	X0D30	X0D09	X0D10	IO VDD	SS_PLL_BYPASS	SS_BYPASS_PLL_LOCK	VDD	VDD	SS_RESET	SS_OTP_VREF	VDD	VDD	VDD	SS_OTP_PWR_UP	VSS	X3D10	X3D09	X3D30	IO VDD	X3D52	X3D53
H	X0D51	X0D50	X0D29	VSS	X0D07	X0D08	SS_CLK											SS_XC0_BS[0]	X3D08	X3D07	IO VDD	X3D29	X3D50	X3D51
J	X0D49	NC	X0D27	X0D28	VSS	X0D06	SS_PLL_LOCK											SS_XC0_BS[1]	X3D06	IO VDD	X3D28	X3D27	NC	X3D49
K	IO VDD	IO VDD	X0D25	X0D26	X0D05	X0D04	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X3D04	X3D05	X3D26	X3D25	VSS	VSS
L	NC	NC	IO VDD	X0D24	X0D03	X0D02	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X3D02	X3D03	X3D24	NC	SS_XC_CFG[0]	SS_XC1_BS[0]
M	NC	NC	NC	NC	X0D01	X0D00	SS_EXT_OSC_CONFIG			VSS	VSS	VSS	VSS	VSS	VSS			SS_DEBUG	X3D00	X3D01	NC	NC	SS_XC_CFG[1]	SS_XC1_BS[1]
N	NC	NC	NC	NC	X1D01	X1D00	SS_EXT_OSC_HS_MODE			VSS	VSS	VSS	VSS	VSS	VSS			SS_RESERVED	X2D00	X2D01	NC	NC	SS_XC0_BS[2]	SS_XC1_BS[2]
P	NC	NC	VSS	X1D24	X1D03	X1D02	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X2D02	X2D03	X2D24	NC	SS_XC0_BS[3]	SS_XC1_BS[3]
R	VSS	VSS	X1D25	X1D26	X1D05	X1D04	VDD			VSS	VSS	VSS	VSS	VSS	VSS			VDD	X2D04	X2D05	X2D26	X2D25	IO VDD	IO VDD
T	X1D49	NC	X1D27	X1D28	IO VDD	X1D06	SS_PLL_TEST											SS_TEST_ENA	X2D06	VSS	X2D28	X2D27	NC	X2D49
U	X1D51	X1D50	X1D29	IO VDD	X1D07	X1D08	SS_PLL_AGND											SS_TCK	X2D08	X2D07	VSS	X2D29	X2D50	X2D51
V	X1D53	X1D52	IO VDD	X1D30	X1D09	X1D10	VSS	SS_PLL_AVDD	SS_OTP_VPP	VDD	VDD	SS_TMS	SS_TDO	VDD	VDD	SS_TDI	SS_TRST	IO VDD	X2D10	X2D09	X2D30	VSS	X2D52	X2D53
W	IO VDD	IO VDD	X1D31	X1D32	X1D11	VSS	X1D12	X1D14	X1D16	X1D18	X1D20	X1D22	X2D22	X2D20	X2D18	X2D16	X2D14	X2D12	IO VDD	X2D11	X2D32	X2D31	VSS	VSS
Y	X1D55	X1D54	X1D33	X1D34	VSS	X1D13	X1D15	X1D17	IO VDD	X1D19	X1D21	X1D23	X2D23	X2D21	X2D19	VSS	X2D17	X2D15	X2D13	IO VDD	X2D34	X2D33	X2D54	X2D55
AA	X1D57	X1D56	X1D35	VSS	X1D36	X1D38	X1D40	IO VDD	X1D42	NC	NC	NC	NC	NC	NC	X2D42	VSS	X2D40	X2D38	X2D36	IO VDD	X2D35	X2D56	X2D57
AB	NC	X1D58	VSS	X1D37	X1D39	X1D41	IO VDD	X1D43	NC	NC	VSS	NC	NC	IO VDD	NC	NC	X2D43	VSS	X2D41	X2D39	X2D37	IO VDD	X2D58	NC
AC	VSS	VSS	NC	X1D62	X1D64	IO VDD	X1D66	X1D68	X1D70	VSS	NC	NC	NC	NC	IO VDD	X2D70	X2D68	X2D66	VSS	X2D64	X2D62	NC	IO VDD	IO VDD
AD	VSS	VSS	X1D61	X1D63	X1D65	IO VDD	X1D67	X1D69	NC	VSS	NC	NC	NC	NC	IO VDD	NC	X2D69	X2D67	VSS	X2D65	X2D63	X2D61	IO VDD	IO VDD

3 Signal Description

Module	Signal	Function	Type	Active	Properties
	PU=Pull Up, PD=Pull Down, ST=Schmitt Trigger Input, OT=Output Tristate, S=Switchable R_S=Required for SPI boot (§5.6), R_U=Required for USB-enabled devices (§10)				
Power	VSS	Digital ground	GND	—	
	VDD	Digital tile power	PWR	—	
	IO VDD	Digital I/O power	PWR	—	
	SS_PLL_AGND	Analog ground for PLL	GND	—	
	SS_PLL_AVDD	Analog PLL power	PWR	—	
	SS_OTP_VPP	OTP programming voltage	PWR	—	
	SS_RESET	Global reset input	Input	—	
PLL	SS_CLK	PLL reference clock	Input	—	PD, ST
	SS_PLL_BYPASS	PLL bypass	Input	—	PD
	SS_EXT_OSC_CONFIG	Oscillator config	Input	—	PD
	SS_EXT_OSC_HS_MODE	Oscillator high-speed mode	Input	—	PD
	SS_XC0_BS[3:0]	Boot status (tile 0)	I/O	—	PU
	SS_XC1_BS[3:0]	Boot status (tile 1)	I/O	—	PU
JTAG	SS_TDI	Test data input	Input	—	PU, ST
	SS_TDO	Test data output	Output	—	PD
	SS_TMS	Test mode select	Input	—	PU, ST
	SS_TRST	Test reset input	Input	—	PU, ST
	SS_TCK	Test clock	Input	—	PU, ST
	SS_DEBUG	Multi-chip debug	I/O	—	PU
Tile 0 I/O	X0D00	$P1A^0$	I/O	—	PD_S, R_S
	X0D01	$X0LA^{4i}_{5b}$ $P1B^0$	I/O	—	PD_S, R_S
	X0D02	$X0LA^{3i}_{5b}$ $P4A^0$ $P8A^0$ $P16A^0$ $P32A^{20}$	I/O	—	PD_S, R_U
	X0D03	$X0LA^{2i}_{5b}$ $P4A^1$ $P8A^1$ $P16A^1$ $P32A^{21}$	I/O	—	PD_S, R_U
	X0D04	$X0LA^{1i}_{2b/5b}$ $P4B^0$ $P8A^2$ $P16A^2$ $P32A^{22}$	I/O	—	PD_S, R_U
	X0D05	$X0LA^{0i}_{2b/5b}$ $P4B^1$ $P8A^3$ $P16A^3$ $P32A^{23}$	I/O	—	PD_S, R_U
	X0D06	$X0LA^{0o}_{2b/5b}$ $P4B^2$ $P8A^4$ $P16A^4$ $P32A^{24}$	I/O	—	PD_S, R_U
	X0D07	$X0LA^{1o}_{2b/5b}$ $P4B^3$ $P8A^5$ $P16A^5$ $P32A^{25}$	I/O	—	PD_S, R_U
	X0D08	$X0LA^{2o}_{5b}$ $P4A^2$ $P8A^6$ $P16A^6$ $P32A^{26}$	I/O	—	PD_S, R_U
	X0D09	$X0LA^{3o}_{5b}$ $P4A^3$ $P8A^7$ $P16A^7$ $P32A^{27}$	I/O	—	PD_S, R_U
	X0D10	$X0LA^{4o}_{5b}$ $P1C^0$	I/O	—	PD_S, R_S
	X0D11	$P1D^0$	I/O	—	PD_S, R_S
	X0D12	$P1E^0$	I/O	—	PD_S, R_U
	X0D13	$X0LB^{4i}_{5b}$ $P1F^0$	I/O	—	PD_S, R_U
	X0D14	$X0LB^{3i}_{5b}$ $P4C^0$ $P8B^0$ $P16A^8$ $P32A^{28}$	I/O	—	PD_S, R_U
	X0D15	$X0LB^{2i}_{5b}$ $P4C^1$ $P8B^1$ $P16A^9$ $P32A^{29}$	I/O	—	PD_S, R_U
	X0D16	$X0LB^{1i}_{2b/5b}$ $P4D^0$ $P8B^2$ $P16A^{10}$	I/O	—	PD_S, R_U
	X0D17	$X0LB^{0i}_{2b/5b}$ $P4D^1$ $P8B^3$ $P16A^{11}$	I/O	—	PD_S, R_U
	X0D18	$X0LB^{0o}_{2b/5b}$ $P4D^2$ $P8B^4$ $P16A^{12}$	I/O	—	PD_S, R_U

(continued)

Module	Name	Function	Type	Active	Properties
Tile 0 I/O	X0D69	$X0LD^{3o}_{5b}$ $P32A^{18}$	I/O	—	PD_S
	X0D70	$X0LD^{4o}_{5b}$ $P32A^{19}$	I/O	—	PD_S
Tile 1 I/O	X1D00	$P1A^0$	I/O	—	PD_S
	X1D01	$X1LA^{4o}_{5b}$ $P1B^0$	I/O	—	PD_S
	X1D02	$X1LA^{3o}_{5b}$ $P4A^0$ $P8A^0$ $P16A^0$ $P32A^{20}$	I/O	—	PD_S, R_U
	X1D03	$X1LA^{2o}_{5b}$ $P4A^1$ $P8A^1$ $P16A^1$ $P32A^{21}$	I/O	—	PD_S, R_U
	X1D04	$X1LA^{1o}_{2b/5b}$ $P4B^0$ $P8A^2$ $P16A^2$ $P32A^{22}$	I/O	—	PD_S, R_U
	X1D05	$X1LA^{0o}_{2b/5b}$ $P4B^1$ $P8A^3$ $P16A^3$ $P32A^{23}$	I/O	—	PD_S, R_U
	X1D06	$X1LA^{0i}_{2b/5b}$ $P4B^2$ $P8A^4$ $P16A^4$ $P32A^{24}$	I/O	—	PD_S, R_U
	X1D07	$X1LA^{1i}_{2b/5b}$ $P4B^3$ $P8A^5$ $P16A^5$ $P32A^{25}$	I/O	—	PD_S, R_U
	X1D08	$X1LA^{2i}_{5b}$ $P4A^2$ $P8A^6$ $P16A^6$ $P32A^{26}$	I/O	—	PD_S, R_U
	X1D09	$X1LA^{3i}_{5b}$ $P4A^3$ $P8A^7$ $P16A^7$ $P32A^{27}$	I/O	—	PD_S, R_U
	X1D10	$X1LA^{4i}_{5b}$ $P1C^0$	I/O	—	PD_S
	X1D11	$P1D^0$	I/O	—	PD_S
	X1D12	$P1E^0$	I/O	—	PD_S, R_U
	X1D13	$X1LB^{4o}_{5b}$ $P1F^0$	I/O	—	PD_S, R_U
	X1D14	$X1LB^{3o}_{5b}$ $P4C^0$ $P8B^0$ $P16A^8$ $P32A^{28}$	I/O	—	PD_S, R_U
	X1D15	$X1LB^{2o}_{5b}$ $P4C^1$ $P8B^1$ $P16A^9$ $P32A^{29}$	I/O	—	PD_S, R_U
	X1D16	$X1LB^{1o}_{2b/5b}$ $P4D^0$ $P8B^2$ $P16A^{10}$	I/O	—	PD_S, R_U
	X1D17	$X1LB^{0o}_{2b/5b}$ $P4D^1$ $P8B^3$ $P16A^{11}$	I/O	—	PD_S, R_U
	X1D18	$X1LB^{0i}_{2b/5b}$ $P4D^2$ $P8B^4$ $P16A^{12}$	I/O	—	PD_S, R_U
	X1D19	$X1LB^{1i}_{2b/5b}$ $P4D^3$ $P8B^5$ $P16A^{13}$	I/O	—	PD_S, R_U
	X1D20	$X1LB^{2i}_{5b}$ $P4C^2$ $P8B^6$ $P16A^{14}$ $P32A^{30}$	I/O	—	PD_S, R_U
	X1D21	$X1LB^{3i}_{5b}$ $P4C^3$ $P8B^7$ $P16A^{15}$ $P32A^{31}$	I/O	—	PD_S, R_U
	X1D22	$X1LB^{4i}_{5b}$ $P1G^0$	I/O	—	PD_S, R_U
	X1D23	$P1H^0$	I/O	—	PD_S, R_U
	X1D24	$P1I^0$	I/O	—	PD_S
	X1D25	$P1J^0$	I/O	—	PD_S
	X1D26	$P4E^0$ $P8C^0$ $P16B^0$	I/O	—	PD_S, R_U
	X1D27	$P4E^1$ $P8C^1$ $P16B^1$	I/O	—	PD_S, R_U
	X1D28	$P4F^0$ $P8C^2$ $P16B^2$	I/O	—	PD_S, R_U
	X1D29	$P4F^1$ $P8C^3$ $P16B^3$	I/O	—	PD_S, R_U
	X1D30	$P4F^2$ $P8C^4$ $P16B^4$	I/O	—	PD_S, R_U
	X1D31	$P4F^3$ $P8C^5$ $P16B^5$	I/O	—	PD_S, R_U
	X1D32	$P4E^2$ $P8C^6$ $P16B^6$	I/O	—	PD_S, R_U
	X1D33	$P4E^3$ $P8C^7$ $P16B^7$	I/O	—	PD_S, R_U
	X1D34	$P1K^0$	I/O	—	PD_S, R_U
	X1D35	$P1L^0$	I/O	—	PD_S, R_U
	X1D36	$P1M^0$ $P8D^0$ $P16B^8$	I/O	—	PD_S, R_U
	X1D37	$P1N^0$ $P8D^1$ $P16B^9$	I/O	—	PD_S, R_U
	X1D38	$P1O^0$ $P8D^2$ $P16B^{10}$	I/O	—	PD_S, R_U
	X1D39	$P1P^0$ $P8D^3$ $P16B^{11}$	I/O	—	PD_S, R_U
	X1D40	$P8D^4$ $P16B^{12}$	I/O	—	PD_S, R_U

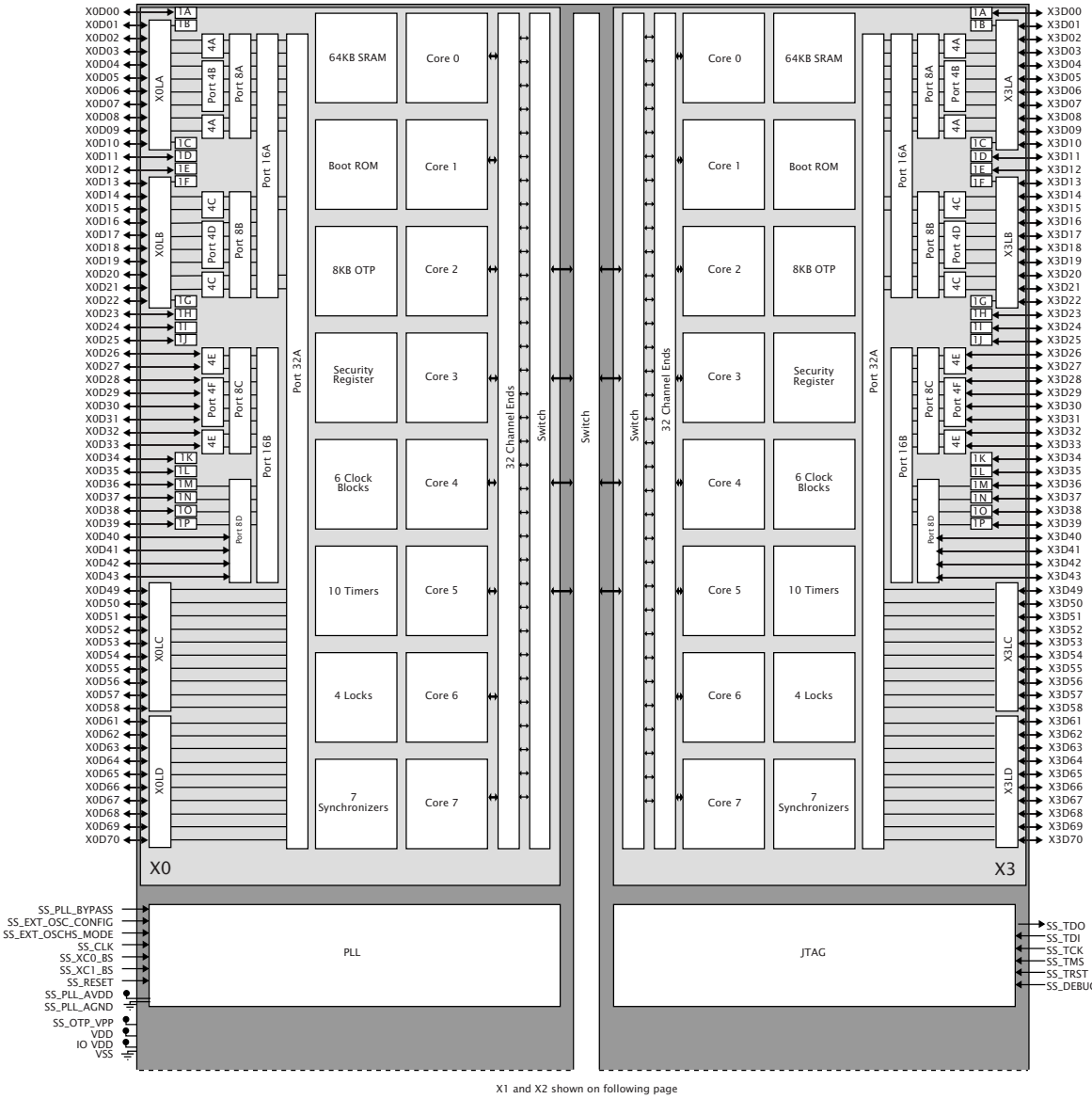
(continued)

Module	Name	Function	Type	Active	Properties
Tile 1 I/O	X1D41	$P8D^5$ $P16B^{13}$	I/O	—	PD_S, R_U
	X1D42	$P8D^6$ $P16B^{14}$	I/O	—	PD_S, R_U
	X1D43	$P8D^7$ $P16B^{15}$	I/O	—	PU_S, R_U
	X1D49	$X1LC^{4o}_{5b}$ $P32A^0$	I/O	—	PD_S
	X1D50	$X1LC^{3o}_{5b}$ $P32A^1$	I/O	—	PD_S
	X1D51	$X1LC^{2o}_{5b}$ $P32A^2$	I/O	—	PD_S
	X1D52	$X1LC^{1o}_{2b/5b}$ $P32A^3$	I/O	—	PD_S
	X1D53	$X1LC^{0o}_{2b/5b}$ $P32A^4$	I/O	—	PD_S
	X1D54	$X1LC^{0i}_{2b/5b}$ $P32A^5$	I/O	—	PD_S
	X1D55	$X1LC^{1i}_{2b/5b}$ $P32A^6$	I/O	—	PD_S
	X1D56	$X1LC^{2i}_{5b}$ $P32A^7$	I/O	—	PD_S
	X1D57	$X1LC^{3i}_{5b}$ $P32A^8$	I/O	—	PD_S
	X1D58	$X1LC^{4i}_{5b}$ $P32A^9$	I/O	—	PD_S
	X1D61	$X1LD^{4o}_{5b}$ $P32A^{10}$	I/O	—	PD_S
	X1D62	$X1LD^{3o}_{5b}$ $P32A^{11}$	I/O	—	PD_S
	X1D63	$X1LD^{2o}_{5b}$ $P32A^{12}$	I/O	—	PD_S
	X1D64	$X1LD^{1o}_{2b/5b}$ $P32A^{13}$	I/O	—	PD_S
	X1D65	$X1LD^{0o}_{2b/5b}$ $P32A^{14}$	I/O	—	PD_S
	X1D66	$X1LD^{0i}_{2b/5b}$ $P32A^{15}$	I/O	—	PD_S
	X1D67	$X1LD^{1i}_{2b/5b}$ $P32A^{16}$	I/O	—	PD_S
	X1D68	$X1LD^{2i}_{5b}$ $P32A^{17}$	I/O	—	PD_S
	X1D69	$X1LD^{3i}_{5b}$ $P32A^{18}$	I/O	—	PD_S
	X1D70	$X1LD^{4i}_{5b}$ $P32A^{19}$	I/O	—	PD_S
Tile 2 I/O	X2D00	$P1A^0$	I/O	—	PD_S
	X2D01	$X2LA^{4i}_{5b}$ $P1B^0$	I/O	—	PD_S
	X2D02	$X2LA^{3i}_{5b}$ $P4A^0$ $P8A^0$ $P16A^0$ $P32A^{20}$	I/O	—	PD_S, R_U
	X2D03	$X2LA^{2i}_{5b}$ $P4A^1$ $P8A^1$ $P16A^1$ $P32A^{21}$	I/O	—	PD_S, R_U
	X2D04	$X2LA^{1i}_{2b/5b}$ $P4B^0$ $P8A^2$ $P16A^2$ $P32A^{22}$	I/O	—	PD_S, R_U
	X2D05	$X2LA^{0i}_{2b/5b}$ $P4B^1$ $P8A^3$ $P16A^3$ $P32A^{23}$	I/O	—	PD_S, R_U
	X2D06	$X2LA^{0o}_{2b/5b}$ $P4B^2$ $P8A^4$ $P16A^4$ $P32A^{24}$	I/O	—	PD_S, R_U
	X2D07	$X2LA^{1o}_{2b/5b}$ $P4B^3$ $P8A^5$ $P16A^5$ $P32A^{25}$	I/O	—	PD_S, R_U
	X2D08	$X2LA^{2o}_{5b}$ $P4A^2$ $P8A^6$ $P16A^6$ $P32A^{26}$	I/O	—	PD_S, R_U
	X2D09	$X2LA^{3o}_{5b}$ $P4A^3$ $P8A^7$ $P16A^7$ $P32A^{27}$	I/O	—	PD_S, R_U
	X2D10	$X2LA^{4o}_{5b}$ $P1C^0$	I/O	—	PD_S
	X2D11	$P1D^0$	I/O	—	PD_S
	X2D12	$P1E^0$	I/O	—	PD_S, R_U
	X2D13	$X2LB^{4i}_{5b}$ $P1F^0$	I/O	—	PD_S, R_U
	X2D14	$X2LB^{3i}_{5b}$ $P4C^0$ $P8B^0$ $P16A^8$ $P32A^{28}$	I/O	—	PD_S, R_U
	X2D15	$X2LB^{2i}_{5b}$ $P4C^1$ $P8B^1$ $P16A^9$ $P32A^{29}$	I/O	—	PD_S, R_U
	X2D16	$X2LB^{1i}_{2b/5b}$ $P4D^0$ $P8B^2$ $P16A^{10}$	I/O	—	PD_S, R_U
	X2D17	$X2LB^{0i}_{2b/5b}$ $P4D^1$ $P8B^3$ $P16A^{11}$	I/O	—	PD_S, R_U
	X2D18	$X2LB^{0o}_{2b/5b}$ $P4D^2$ $P8B^4$ $P16A^{12}$	I/O	—	PD_S, R_U
	X2D19	$X2LB^{1o}_{2b/5b}$ $P4D^3$ $P8B^5$ $P16A^{13}$	I/O	—	PD_S, R_U

(continued)

Module	Name	Function	Type	Active	Properties
Tile 3 I/O	X3D42	P8D^{6} P16B^{14}	I/O	—	PD_S, R_U
	X3D43	P8D^{7} P16B^{15}	I/O	—	PU_S, R_U
	X3D49	$X3LC^{4o}_{5b}$ P32A^{0}	I/O	—	PD_S
	X3D50	$X3LC^{3o}_{5b}$ P32A^{1}	I/O	—	PD_S
	X3D51	$X3LC^{2o}_{5b}$ P32A^{2}	I/O	—	PD_S
	X3D52	$X3LC^{1o}_{2b/5b}$ P32A^{3}	I/O	—	PD_S
	X3D53	$X3LC^{0o}_{2b/5b}$ P32A^{4}	I/O	—	PD_S
	X3D54	$X3LC^{0i}_{2b/5b}$ P32A^{5}	I/O	—	PD_S
	X3D55	$X3LC^{1i}_{2b/5b}$ P32A^{6}	I/O	—	PD_S
	X3D56	$X3LC^{2i}_{5b}$ P32A^{7}	I/O	—	PD_S
	X3D57	$X3LC^{3i}_{5b}$ P32A^{8}	I/O	—	PD_S
	X3D58	$X3LC^{4i}_{5b}$ P32A^{9}	I/O	—	PD_S
	X3D61	$X3LD^{4o}_{5b}$ P32A^{10}	I/O	—	PD_S
	X3D62	$X3LD^{3o}_{5b}$ P32A^{11}	I/O	—	PD_S
	X3D63	$X3LD^{2o}_{5b}$ P32A^{12}	I/O	—	PD_S
	X3D64	$X3LD^{1o}_{2b/5b}$ P32A^{13}	I/O	—	PD_S
	X3D65	$X3LD^{0o}_{2b/5b}$ P32A^{14}	I/O	—	PD_S
	X3D66	$X3LD^{0i}_{2b/5b}$ P32A^{15}	I/O	—	PD_S
	X3D67	$X3LD^{1i}_{2b/5b}$ P32A^{16}	I/O	—	PD_S
	X3D68	$X3LD^{2i}_{5b}$ P32A^{17}	I/O	—	PD_S
	X3D69	$X3LD^{3i}_{5b}$ P32A^{18}	I/O	—	PD_S
	X3D70	$X3LD^{4i}_{5b}$ P32A^{19}	I/O	—	PD_S
Reserved	SS_PLL_LOCK	Reserved (do not connect)	Output	—	PD
	SS_BYPASS_PLL_LOCK	Reserved (tie to VSS)	Input	—	PD
	SS_PLL_TEST	Reserved (do not connect)	Input	—	
	SS_OTP_VREF	Reserved (do not connect)	Output	—	
	SS_OTP_PWR_UP	Reserved (do not connect)	Output	—	
	SS_TEST_ENA	Reserved (tie to VSS)	Input	—	PD
	SS_XC_CFG[1:0]	Reserved (tie to VSS)	Input	—	PD
	SS_RESERVED	Reserved (do not connect)	Output	—	
	NC	Not connected	I/O	—	

4 Block Diagram



X1 and X2 shown on following page

5 Product Overview

The XMOS XS1-G04B-FB512 is a powerful device that provides a simple design process and highly-flexible solution to many applications. The device consists of four xCORE Tiles, each comprising a flexible multicore microcontroller with tightly integrated I/O and on-chip memory. The processors run mutiple tasks simultaneously using logical cores, each of which is guaranteed a slice of processing power and can execute computational code, control software and I/O interfaces. Logical cores use channels to exchange data within a tile or across tiles. The tiles are connected via an integrated switch network, which uses a proprietary physical layer protocol, and which can also be used to add additional resources to a design. The I/O pins are driven using intelligent ports that can serialize data, interpret strobe signals and wait for scheduled times or events, making the device ideal for real-time control applications.

The device can be configured using a set of software components that are rapidly customized and composed. XMOS provides source code libraries for many standard components. The device can be programmed using high-level languages such as C/C++ and XMOS-originated extensions to C, called XC, that simplify the control over concurrency, I/O and time.

The XMOS toolchain includes compilers, a simulator, debugger and static timing analyzer. The combination of real-time software, a compiler and timing analyzer enables the programmer to close timings on components of the design without a detailed understanding of the hardware characteristics.

5.1 Logical cores, Synchronizers and Locks

Each xCORE Tile has up to eight active logical cores, which issue instructions down a shared four-stage pipeline. Instructions from the active cores are issued round-robin. If up to four logical cores are active, each core is allocated a quarter of the processing cycles. If more than four logical cores are active, each core is allocated at least $1/n$ cycles (for n cores). Figure 1 shows the guaranteed core performance depending on the number of cores used.

Figure 1: Core performance

Speed Grade	Minimum MIPS per core (for *n* cores)							
	1	2	3	4	5	6	7	8
400 MHz	100	100	100	100	80	67	57	50

There is no way that the performance of a logical core can be reduced below these predicted levels. Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than four logical cores, the performance of each core is often higher than the predicted minimum.

5.2 Channel Ends, Links and Switch

Logical cores communicate using point-to-point connections formed between two channel ends. Between tiles, channel communications are implemented over

xConnect Links and routed through switches. The links operate in either 2bit/direction or 5bit/direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link. A total of eight 5bit links are available between every pair of cores.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-G Link Performance and Design Guide, X7561.

5.3 Ports and Clock Blocks

Ports provide an interface between the logical cores and I/O pins. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

The operation of each port is synchronized to a clock block. A clock block can be connected to an external clock input, or it can be run from the divided reference clock. A clock block can also output its signal to a pin. On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

The ports and links are multiplexed, allowing the pins to be configured for use by ports of different widths or links. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

5.4 Timers

Timers are 32-bit counters that are relative to the xCORE Tile reference clock. A timer is defined to tick every 10 ns. This value is derived from the reference clock, which is configured to tick at 100 MHz by default.

5.5 PLL

The PLL is used to generate all on-chip clocks. SS_CLK is the reference clock input. It should be supplied with a clock with monotonic rising edges and should be stable before SS_RESET is taken high.

Many standard clock frequencies can be used with appropriate settings configured into the PLL. At boot time, before the PLL can be reconfigured, the PLL multiplier is set using the pins specified in the table in Figure 2. The PLL increases the clock frequency to the tile frequency used to run the processor data path and the switch.

Clock frequencies of betweeen 20 MHz and 25 MHz are not supported.

Further details on configuring the clock can be found in the XS1-G Clock Frequency Control document, X3221.

SS_PLL_BYPASS	SS_EXT_OSC_CONFIG	SS_EXT_OSC_HS_MODE	PLL multiplier ratio	CLK Input (MHz)	Boot Frequency (MHz)
0	0	X	20	12.5–20	250–400
0	1	0	5	25–50	125–250
0	1	1	2.5	50–100	125–250
1	X	X	0.5	<100	<50

Figure 2: PLL boot modes

5.6 Boot ROM

The boot procedure is illustrated in Figure 3. If bit 5 of the security register is set (*see* §5.7.1), the device boots from OTP. Otherwise, SS_XC0_BS[1:0] controls the boot source.

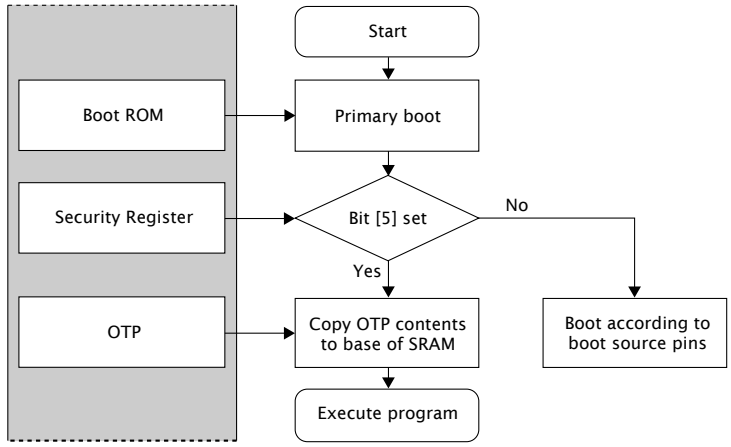


Figure 3: Boot procedure

SS_XC0_BS[1:0] operates as an input prior to the de-assertion of SS_RESET. The device latches the value driven onto these pins on the rising edge (de-assertion) of SS_RESET. The value driven should be static and configured using pullup or pulldown resistors, as the device drives the boot status on these pins after reset. The value configured on these two pins defines the boot mode, as described in Figure 4.

After reset is complete, SS_XC0_BS[3:0] becomes an output and indicates the boot mode, as described in Figure 5. SS_XC1_BS[3:0] also becomes an output after reset, indicating the tile 1 boot mode. SS_XC*n*_BS[3] indicates that the boot on tile *n* has completed.

5.7 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in 2k rows x 32-bit configuration which can be used to implement secure

SS_XC0_BS[1]	SS_XC0_BS[0]	Boot Mode		
0	0	Reserved		
0	1	Reserved		
1	0	X0 boots from SPI, X1..X3 from channel end 0 via X0		
		Pin[A]	**Signal**	**Description**
		X0D00	MISO	Master In Slave Out
		X0D01	SS	Slave Select
		X0D10	SCLK	Clock
		X0D11	MOSI	Master Out Slave In
1	1	None: Device waits to be booted via JTAG		

Figure 4: Boot source pins

A The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. An SPI boot program can be burned into OTP and used at any time.

SS_XC*n*_BS[2]	SS_XC*n*_BS[1]	SS_XC*n*_BS[0]	Boot Mode
0	0	1	X*n* booted from OTP
0	1	0	Reserved
0	1	1	X*n* booted from chanend 0
1	0	0	X*n* booted from SPI
1	0	1	X*n* booted from JTAG

Figure 5: Boot mode indication pins

bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

5.7.1 Security Register

The security register enables the following security features:

- **Secure Boot**: The xCORE Tile is forced to boot from address 0 of the OTP, allowing the xCORE Tile boot ROM to be bypassed (*see* §5.6). This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.
- **Disable JTAG**: The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
- **Disable Link access**: Other tiles are forbidden access to the processor state via the system switch.

TAP and the chip TAP. The boundary scan TAP is a standard 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. The chip TAP provides access into the xCORE Tile, switch and OTP for loading code and debugging.

The SS_TRST pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the SS_TRST pin can be tied to ground to hold the JTAG module in reset.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 7.

Figure 7: IDCODE return value

Bit31																												Bit0
Version				Part Number																Manufacturer Identity								1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	1	1
0				0				1				0				4				6				3				3			

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 8. The OTP User ID field is read from bits [22:31] of the security register on xCORE Tile 0 (all zero on unprogrammed devices).

Figure 8: USERCODE return value

Bit31																												Bit0
OTP User ID										Unused				Silicon Revision														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0				0				0				2				8				0				0				0			

5.10 Power Supplies

The device has the following types of power supply pins:

- VDD pins for the xCORE Tile tile
- IO VDD pins for the I/O lines
- SS_PLL_AVDD pins for the PLL
- SS_OTP_VPP pins for faster programming the OTP (optional)

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0 V to its final value within 10 ms to ensure correct startup.

The IO VDD supply must ramp to its final value before VDD reaches 0.4 V.

The SS_PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 Ω resistor and 1 µF multi-layer ceramic capacitor) is recommended on this pin.

The SS_OTP_VPP supply can be optionally provided for faster OTP programming times, otherwise an internal charge pump is used.

The following ground pins are provided:

- PLL_AGND for PLL_AVDD
- GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and IO VDD supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 4x100nF 0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

SS_RESET is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §5.6). SS_RESET and must be asserted low during and after power up for 100 ns.

6.4 Reset Timing

Figure 12: Reset timing

Symbol	Parameters	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	100			ns	
T(PLLLOCK)	PLL lock			1	ms	
T(INIT)	Initialization time			<100	µs	A

A Shows the time taken to start booting after SS_RESET has gone high.

6.5 Quiescent Current

Figure 13: Quiescent current

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		120		mA	
I(PLLQ)	Quiescent PLL current		4		mA	

6.6 Power Consumption

Figure 14: xCORE Tile currents

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
PD	Tile power dissipation		1.6		Watts	A, B, C, D

A Use for budgetary purposes only.

B Assumes typical tile and I/O voltages operating at 400 MHz with nominal activity on all tiles.

C PD(TYP) value is the usage power consumption under typical operating conditions.

D PD(TYP) value includes quiescent current.

The tile power consumption of the device is highly application dependent and should be used for budgetary purposes only.

More detailed power analysis can be found in the XS1-G Power Consumption document, X7561.

6.7 Clock

Figure 15: Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	12.5	20	20	MHz	
SR	Slew rate	1		2	ns	
f(MAX)	Processor clock frequency			400	MHz	

Further details can be found in the XS1-G Clock Frequency Control document, X3221.

6.8 xCORE Tile I/O AC Characteristics

Figure 16: I/O AC characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOVALID)	Input data valid window	8			ns	
T(XOINVALID)	Output data invalid window	9			ns	
T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

6.9 xConnect Link Performance

Figure 17: Link performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	A, B
B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	A, B
B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	B
B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	B

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of SS_CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

6.10 JTAG Timing

Figure 18: JTAG timing

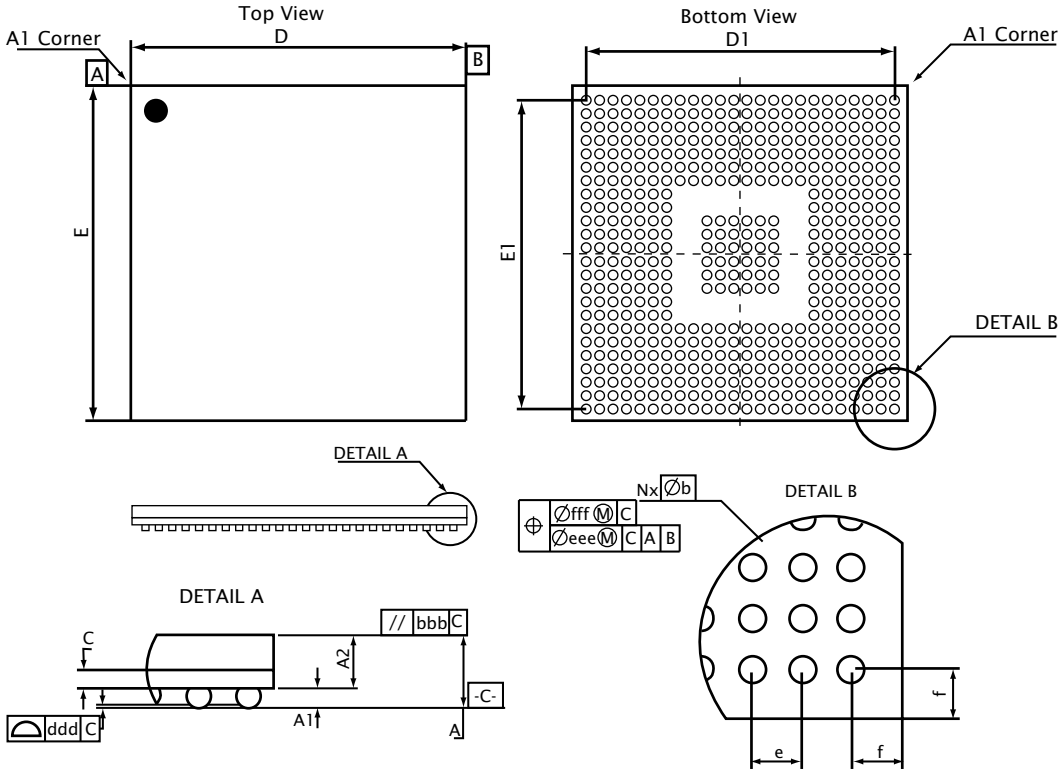
Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(TCK)	TCK period	30			ns	
T(SETUP)	TDO to TCK setup time	5			ns	A
T(HOLD)	TDO to TCK hold time			10	ns	A
T(DELAY)	TCK to output delay			15	ns	B

A Timing applies to SS_TMS, SS_TRST and SS_TDI inputs.

B Timing applies to SS_TDO output.

All JTAG operations are synchronous to SS_TCK apart from the global asynchronous reset SS_TRST.

7 Package Information



Dimensional Ref			
REF	Min	Nom	Max
A			1.6
A1	0.27		
A2	1.02	1.06	1.1
D		20.0	
D1		18.4	
E		20.0	
E1		18.4	
b		0.5	
c	0.32	0.36	0.40
e		0.8	
f		0.8	
m		24	
n		512	

Dimensional Tol	
aaa	0.15
bbb	0.10
ddd	0.20
eee	0.15
fff	0.08

Notes

1. All dimensions in mm.
2. ‘e’ represents the basic solder ball pitch.
3. ‘m’ represents the basic solder ball matrix size. ‘n’ is the number of attached solder balls.
4. ‘b’ is measurable at the maximum solder ball diameter parallel the primary datum – C –.
5. Dimension ‘aaa’ is measured parallel to primary datum – C –.
6. Primary datum – C – and the seating plane are defined by the spherical crowns of the solder balls.
7. The package surface shall be matte finish charmilles 24 to 27.
8. The over package thickness ‘A’ already considers collapse balls.

12 Related Documentation

Document Title	Information	Document Number
The XMOS XS1 Architecture	ISA manual	X7879
XS1 Port I/O Timing	Port timings	X5821
XS1-G System Specification	Link, switch and system information	X2725
XS1-G Link Performance and Design Guidelines	Link timings	X7561
XS1-G Clock Frequency Control	Advanced clock control	X3221

13 Revision History

The page numbers in this section refer to this document.

Rev. X1066I-10/12

1. Renamed XCore to xCORE Tile, and Thread to Core.
2. Instruction description updated - page 2.

Rev. X1066H-05/12-B

1. Block diagram updated: pins listed sequentially, 4-bit ports updated - page 11.

Rev. X1066G-05/12

1. SS_XC0_CFG and SS_PLL_BYPASS tied to VSS on page 4.
2. OTP section updated and moved before SRAM on page 17.

Rev. X1066F-03/12

1. Removed “Volatile” from Memory description on page 2.
2. Updated 32-bit port connection in block diagram on page 11.

Rev. X1066E-10/11

1. Updated “Part Marking” on page 24.

Rev. X1066D-05/11-B

1. Revised format.
2. Standard XMOS Link format XnLn on page 4.

Rev. X1066C-01/11

1. Replaced “Port Pin Table” with “Signal Description” on page 4.
2. Updated “ULPI” on page 24 with set of disabled signals.
3. Removed “Device Configuration”.
4. Added “Associated Design Documentation” on page 25.
5. Clock frequencies of betweeen 20 MHz and 25 MHz are **not** supported.
6. Removed documentation of numerous JTAG commands, which were incorrect.
7. Updated Figure 10 in “DC Characteristics” on page 20 by removing rows for I(OH) and I(OL).
8. Updated Figure 17 in “xConnect Link Performance’ on page 22 by removing rows for B(2link) and B(5link), and adding rows for B(2linkP), B(5linkP), B(2linkS) and B(5linkS).
9. Renamed IO VSS signals to VSS.

Rev. X1066B-06/10

1. Updated pin list on page 4.
2. Updated “Power Consumption” on page 21.

Rev. X1066A-12/09

1. Revised format.