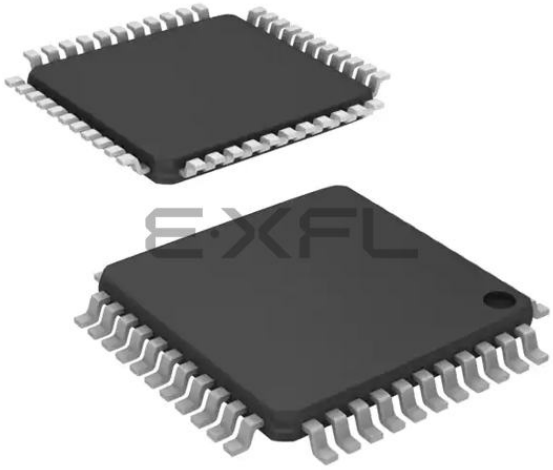

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj32gb004t-i-pt

4.0 MEMORY ORGANIZATION

As Harvard architecture devices, PIC24F microcontrollers feature separate program and data memory spaces and busses. This architecture also allows the direct access of program memory from the data space during code execution.

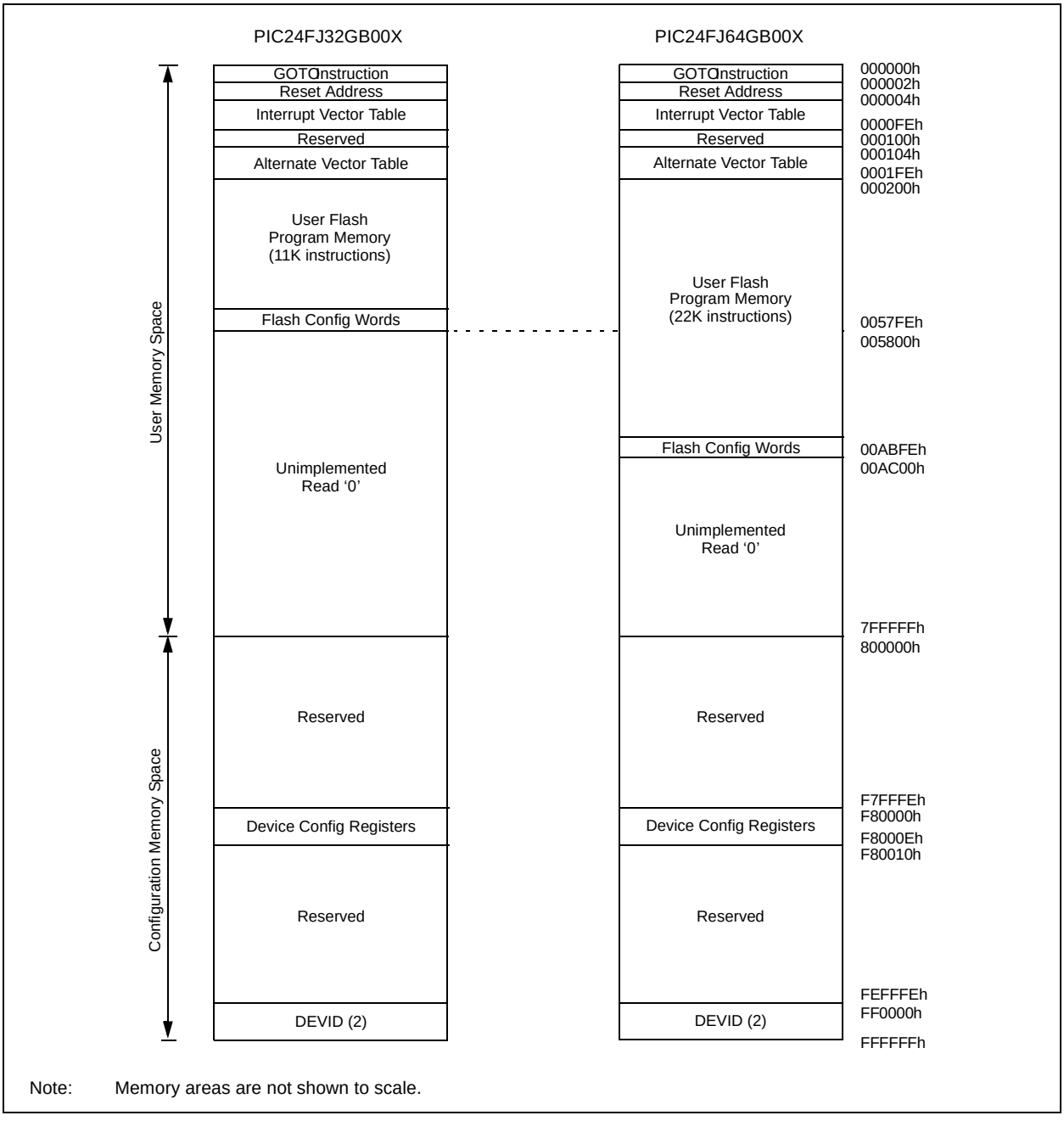
4.1 Program Address Space

The program address memory space of the PIC24FJ64GB004 family devices is 4M instructions. The space is addressable by a 24-bit value derived from either the 23-bit Program Counter (PC) during program execution, or from table operation or data space remapping, as described in Section 4.3 “Interfacing Program and Data Memory Spaces” .

User access to the program memory space is restricted to the lower half of the address range (000000h to 7FFFFFh). The exception is the use of TBLRD/TBLWT operations which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

Memory maps for the PIC24FJ64GB004 family of devices are shown in Figure 4-1.

FIGURE 4-1: PROGRAM SPACE MEMORY MA P FOR PIC24FJ64GB004 FAMILY DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-6: TIMER REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Timer1 Period Register																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																0000
TMR3	010A	Timer3 Register																0000
PR2	010C	Timer2 Period Register																FFFF
PR3	010E	Timer3 Period Register																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (for 32-bit operations only)																0000
TMR5	0118	Timer5 Register																0000
PR4	011A	Timer4 Period Register																FFFF
PR5	011C	Timer5 Period Register																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
ALTIVT	DISI	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 ALTIVT: Enable Alternate Interrupt Vector Table (AIVT) bit
1 = Use Alternate Interrupt Vector Table
0 = Use standard (default) Interrupt Vector Table (IVT)

bit 14 DISI: DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13-3 Unimplemented: Read as ‘0’

bit 2 INT2EP: External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 INT1EP: External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 INT0EP: External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

10.4.6 PERIPHERAL PIN SELECT REGISTERS

The PIC24FJ64GB004 family of devices implements a total of 27 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (14)
- Output Remappable Peripheral Registers (13)

Note:	Input and output register values can only be changed if IOLOCK (OSCCON<6>) = 0. See Section 10.4.4.1 “Control Register Lock” for a specific command sequence.

REGISTER 10-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as ‘0’

bit 12-8 INT1R<4:0>: Assign External Interrupt 1 (INT1) to Corresponding RPn or RPIn Pin bits

bit 7-0 Unimplemented: Read as ‘0’

REGISTER 10-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 Unimplemented: Read as ‘0’

bit 4-0 INT1R<4:0>: Assign External Interrupt 2 (INT2) to Corresponding RPn or RPIn Pin bits

18.1.2 HOST AND OTG MODES

18.1.2.1 D+ and D- Pull-down Resistors

PIC24FJ64GB004 family devices have built-in 15 k : pull-down resistor on the D+ and D- lines. These are used in tandem to signal to the bus that the microcontroller is operating in Host mode. They are engaged by setting the HOSTEN bit (U1CON<3>). If the OTGEN bit (U1OTGCON<2>) is set, then these pull-downs are enabled by setting the DPPULDWN and DMPULDWN bits (U1OTGCON<5:4>).

18.1.2.2 Power Configurations

In Host mode, as well as Host mode in On-the-Go operation, the USB 2.0 specification requires that the Host application supply power on VBUS. Since the microcontroller is running below VBUS and is not able to source sufficient current, a separate power supply must be provided.

When the application is always operating in Host mode, a simple circuit can be used to supply VBUS and regulate current on the bus (Figure 18-6). For OTG operation, it is necessary to be able to turn VBUS on or off as needed, as the microcontroller switches between Device and Host modes. A typical example using an external charge pump is shown in Figure 18-7.

FIGURE 18-6: HOST INTERFACE EXAMPLE

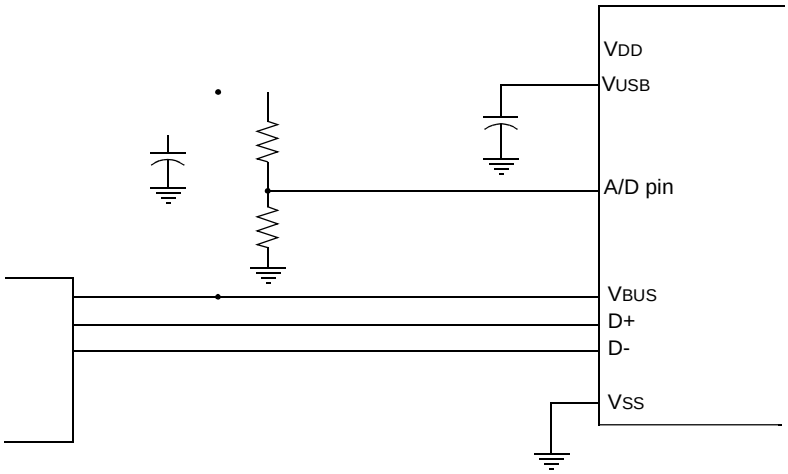


FIGURE 18-7: OTG INTERFACE EXAMPLE

18.5.3 SEND A FULL-SPEED BULK DATA TRANSFER TO A TARGET DEVICE

1. Follow the procedure described in Section 18.5.1 “Enable Host Mode and Discover a Connected Device” and Section 18.5.2 “Complete a Control Transaction to a Connected Device” to discover and configure a device.
2. To enable transmit and receive transfers with handshaking enabled, write 1Dh to U1EP0. If the target device is a low-speed device, also set the LSPD bit (U1EP0<7>). If you want the hardware to automatically retry indefinitely if the target device asserts a NAK on the transfer, clear the Retry Disable bit, RETRYDIS (U1EP0<6>).
3. Set up the BD for the current (EVEN or ODD) Tx EP0 to transfer up to 64 bytes.
4. Set the USB device address of the target device in the address register (U1ADDR<6:0>).
5. Write an OUT token to the desired endpoint to U1TOK. This triggers the module’s transmit state machines to begin transmitting the token and the data.
6. Wait for the Transfer Done Interrupt Flag, TRNIF. This indicates that the BD has been released back to the microprocessor, and the transfer has completed. If the retry disable bit is set, the handshake (ACK, NAK, STALL or ERROR (0Fh)) is returned in the BD PID field. If a STALL interrupt occurs, the pending packet must be dequeued and the error condition in the target device cleared. If a detach interrupt occurs (SE0 for more than 2.5 µs), then the target has detached (U1IR<0> is set).
7. Once the transfer done interrupt occurs (TRNIF is set), the BD can be examined and the next data packet queued by returning to step 2.

Note:	USB speed, transceiver and pull-ups should only be configured during the module setup phase. It is not recommended to change these settings while the module is enabled.

18.6 OTG Operation

18.6.1 SESSION REQUEST PROTOCOL (SRP)

An OTG A-device may decide to power down the VBUS supply when it is not using the USB link through the Session Request Protocol (SRP). Software may do this by clearing VBUSON (U1OTGCON<3>). When the VBUS supply is powered down, the A-device is said to have ended a USB session.

An OTG A-device or Embedded Host may re-power the VBUS supply at any time (initiate a new session). An OTG B-device may also request that the OTG A-device re-power the VBUS supply (initiate a new session). This is accomplished via Session Request Protocol (SRP).

Prior to requesting a new session, the B-device must first check that the previous session has definitely ended. To do this, the B-device must check for two conditions:

1. VBUS supply is below the Session Valid voltage, and

2. Both D+ and D- have been low for at least 2 ms.

The B-device will be notified of condition 1 by the SESENDIF (U1OTGIR<2>) interrupt. Software will have to manually check for condition 2.

Note:	When the A-device powers down the VBUS supply, the B-device must disconnect its pull-up resistor from power. If the device is self-powered, it can do this by clearing DPPULUP (U1OTGCON<7>) and DMPULUP (U1OTGCON<6>).

The B-device may aid in achieving condition 1 by discharging the VBUS supply through a resistor. Software may do this by setting VBUSDIS (U1OTGCON<0>).

After these initial conditions are met, the B-device may begin requesting the new session. The B-device begins by pulsing the D+ data line. Software should do this by setting DPPULUP (U1OTGCON<7>). The data line should be held high for 5 to 10 ms.

18.7.1 USB OTG MODULE CONTROL REGISTERS

REGISTER 18-3: U1OTGSTAT: USB OTG ST ATUS REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HSC	U-0	R-0, HSC	U-0	R-0, HSC	R-0, HSC	U-0	R-0, HSC
ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD
bit 7							bit 0

Legend:	U = Unimplemented bit, read as ‘0’		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as ‘0’

bit 7 ID: ID Pin State Indicator bit
1 = No plug is attached, or a type B cable has been plugged into the USB receptacle
0 = A type A plug has been plugged into the USB receptacle

bit 6 Unimplemented: Read as ‘0’

bit 5 LSTATE: Line State Stable Indicator bit
1 = The USB line state (as defined by SE0 and JSTATE) has been stable for the previous 1 ms
0 = The USB line state has NOT been stable for the previous 1 ms

bit 4 Unimplemented: Read as ‘0’

bit 3 SESVD: Session Valid Indicator bit
1 = The V_{BUS} voltage is above $V_{A\_SESS\_VLD}$ (as defined in the USB OTG Specification) on the A or B-device
0 = The V_{BUS} voltage is below $V_{A\_SESS\_VLD}$ on the A or B-device

bit 2 SESEND: B-Session End Indicator bit
1 = The V_{BUS} voltage is below $V_{B\_SESS\_END}$ (as defined in the USB OTG Specification) on the B-device
0 = The V_{BUS} voltage is above $V_{B\_SESS\_END}$ on the B-device

bit 1 Unimplemented: Read as ‘0’

bit 0 VBUSVD: A-V_{BUS} Valid Indicator bit
1 = The V_{BUS} voltage is above $V_{A\_VBUS\_VLD}$ (as defined in the USB OTG Specification) on the A-device
0 = The V_{BUS} voltage is below $V_{A\_VBUS\_VLD}$ on the A-device

22.0 10-BIT HIGH-SPEED A/D CONVERTER

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the "PIC24F Family Reference Manual", Section 17. "10-Bit A/D Converter" (DS39705).

The 10-bit A/D Converter has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 500 ksps
- 13 analog input pins
- External voltage reference input pins
- Internal band gap reference inputs
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable Buffer Fill modes
- Four result alignment options
- Operation during CPU Sleep and Idle modes

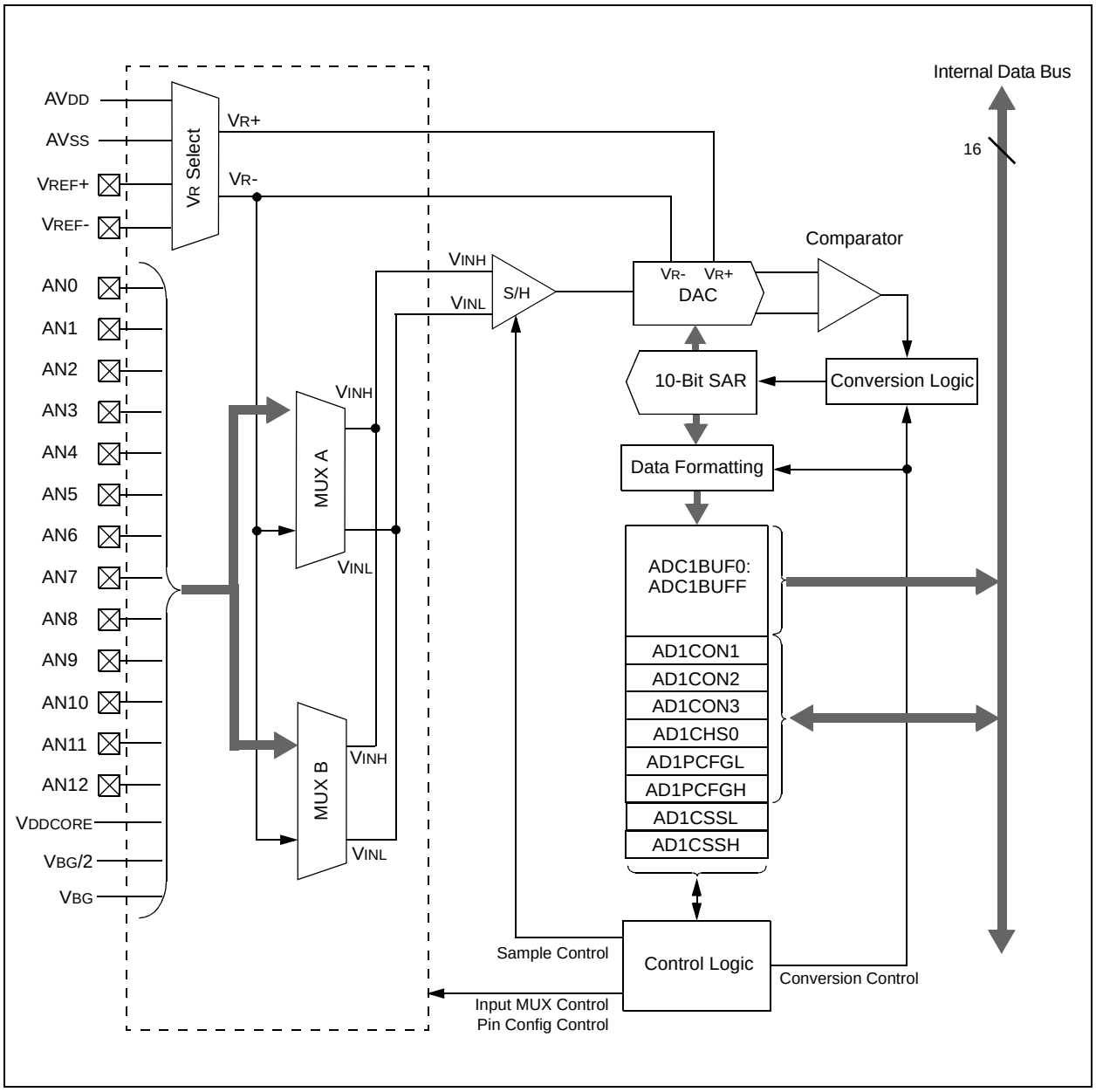
On all PIC24FJ64GB004 family devices, the 10-bit A/D Converter has 13 analog input pins, designated AN0 through AN12. In addition, there are two analog input pins for external voltage reference connections (V_{REF+} and V_{REF-}). These voltage reference inputs may be shared with other analog input pins.

A block diagram of the A/D Converter is shown in Figure 22-1.

To perform an A/D conversion:

1. Configure the A/D module:
   a) Configure port pins as analog inputs and/or select band gap reference inputs (AD1PCFGL<15:0> and AD1PCFGH<1:0>).
   b) Select voltage reference source to match expected range on analog inputs (AD1CON2<15:13>).
   c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
   d) Select the appropriate sample/conversion sequence (AD1CON1<7:5> and AD1CON3<12:8>).
   e) Select how conversion results are presented in the buffer (AD1CON1<9:8>).
   f) Select interrupt rate (AD1CON2<5:2>).
   g) Turn on A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
   a) Clear the AD1IF bit.
   b) Select A/D interrupt priority.

FIGURE 22-1: 10-BIT HIGH-SPEED A/D CONVERTER BLOCK DIAGRAM



23.0 TRIPLE COMPARATOR MODULE

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the associated "PIC24F Family Reference Manual", Section 46. "Scalable Comparator Module" (DS39734).

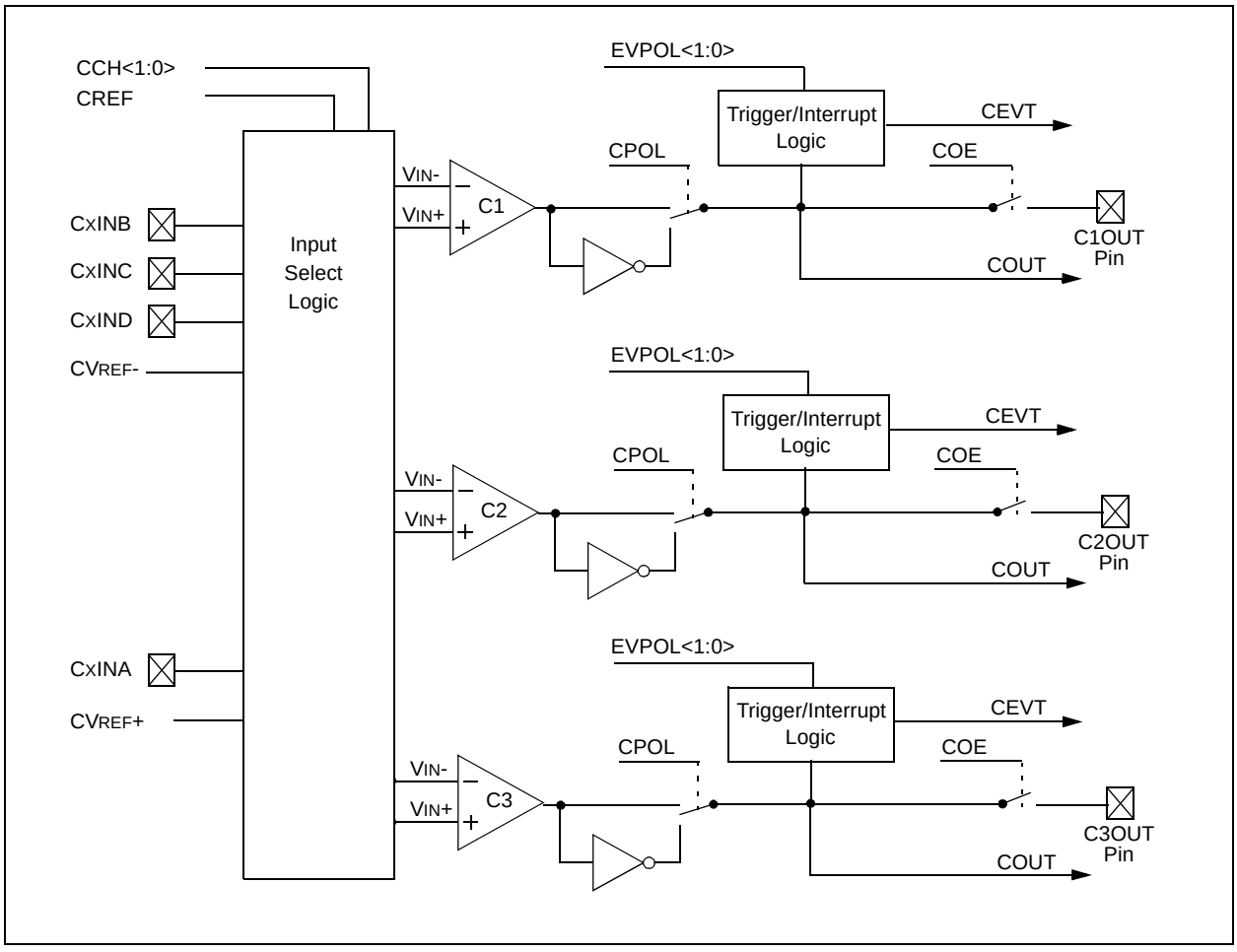
The triple comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of four external analog inputs, as well as voltage reference inputs from the voltage reference generator and band gap reference.

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module in shown in Figure 23-1. Diagrams of the possible individual comparator configurations are shown in Figure 23-2.

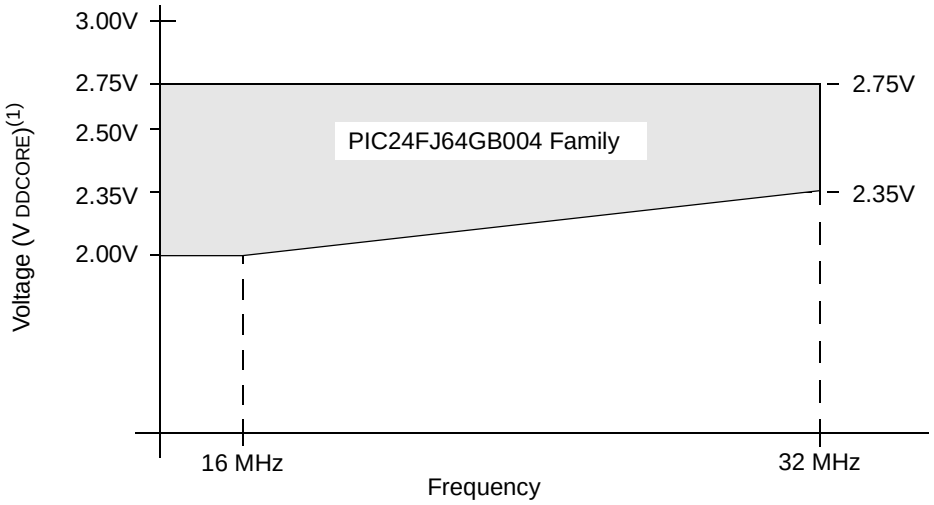
Each comparator has its own control register, CMxCON (Register 23-1), for enabling and configuring its operation. The output and event status of all three comparators are provided in the CMSTAT register (Register 23-2).

FIGURE 23-1: TRIPLE COMPARATOR MODULE BLOCK DIAGRAM



29.1 DC Characteristics

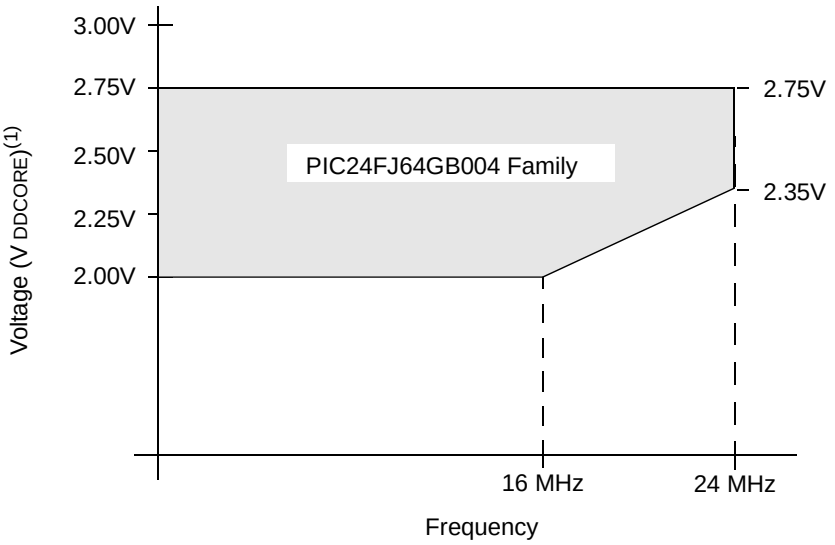
FIGURE 29-1: PIC24FJ64GB004 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



For frequencies between 16 MHz and 32 MHz, FMAX = (45.7 MHz/V) * (VDDCORE – 2V) + 16 MHz.

Note 1: When the voltage regulator is disabled, VDD and VDDCORE must be maintained so that VDDCORE ≤ VDD ≤ 3.6V.

FIGURE 29-2: PIC24FJ64GB004 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED TEMPERATURE)



For frequencies between 16 MHz and 24 MHz, FMAX = (22.9 MHz/V) * (VDDCORE – 2V) + 16 MHz.

Note 1: WHEN the voltage regulator is disabled, VDD and VDDCORE must be maintained so that VDDCORE ≤ VDD ≤ 3.6V.

TABLE 29-7: DC CHARACTERISTICS: POWER-DOWN PERIPHERAL MODULE ' CURRENT (IPD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C dTA d+85°C for Industrial -40°C dTA d+125°C for Extended			
Parameter No.	Typical (1)	Max	Units	Conditions		
' Power-Down Current (I PD): PMD Bits are Set, PMSLP Bit is ' 0'(2)						
DC63	1.8	2.3	PA	-40°C	2.0V(3)	32 kHz Crystal with RTCC, DSWDT or Timer1: 'ISOSC; SOSCSEL = 11(5)
DC63a	1.8	2.7	PA	+25°C		
DC63i	1.8	3.0	PA	+60°C		
DC63b	1.8	3.0	PA	+85°C		
DC63m	2.2	3.3	PA	+125C		
DC63c	2	2.7	PA	-40°C	2.5V(3)	
DC63d	2	2.9	PA	+25°C		
DC63j	2	3.2	PA	+60°C		
DC63e	2	3.5	PA	+85°C		
DC63n	2.5	3.8	PA	+125C		
DC63f	2.25	3.0	PA	-40°C	3.3V(4)	
DC63g	2.25	3.0	PA	+25°C		
DC63k	2.25	3.3	PA	+60°C		
DC63h	2.25	3.5	PA	+85°C		
DC63p	2.8	4.0	PA	+125C		
DC71c	0.001	0.25	PA	-40°C	2.5V(4)	Deep Sleep BOR: 'IDSBOR(5)
DC71d	0.03	0.25	PA	+25°C		
DC71j	0.05	0.60	PA	+60°C		
DC71e	0.08	2.0	PA	+85°C		
DC71a	3.9	10	PA	+125C		
DC71f	0.001	0.50	PA	-40°C	3.3V(4)	
DC71g	0.03	0.50	PA	+25°C		
DC71k	0.05	0.75	PA	+60°C		
DC71h	0.08	2.5	PA	+85°C		
DC71b	3.9	12.5	PA	+125C		

Note 1: Data in the Typical column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Peripheral IPD deltas are measured with the device in Sleep mode (all peripherals and clocks shut down). All I/Os are configured as inputs and pulled high. Only the peripheral or clock being measured is enabled. PMSLP bit is clear and the Peripheral Module Disable bits (PMD) for all unused peripherals are set.

3: On-chip voltage regulator disabled (DISVREG tied to VDD).

4: On-chip voltage regulator enabled (DISVREG tied to VSS). Low-Voltage Detect (LVD) and Brown-out Detect (BOD) are enabled.

5: The ' current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

FIGURE 29-4: EXTERNAL CLOCK TIMING

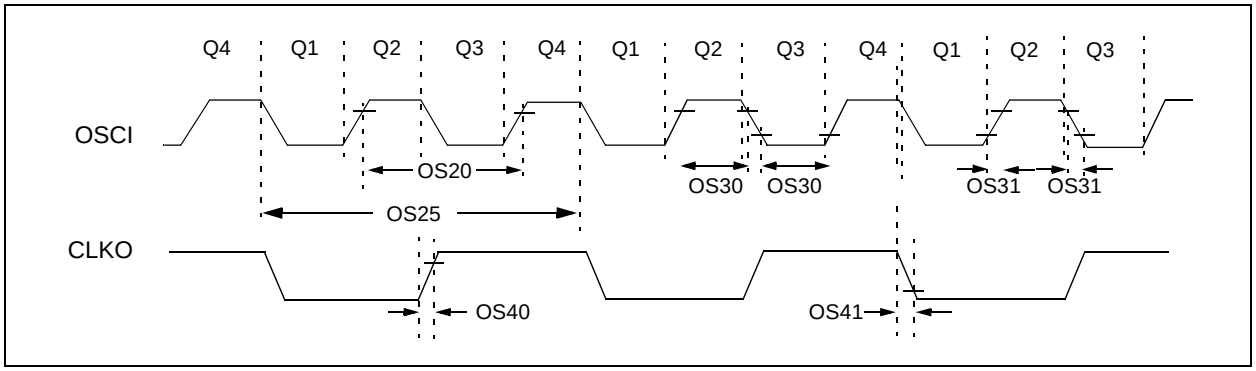


TABLE 29-16: EXTERNAL CLO CK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.50 to 3.6V (unless otherwise stated) Operating temperature -40°C dTA d+85°C for Industrial -40°C dTA d+125°C for Extended				
Param No.	Sym	Characteristic	Min	Typ (1)	Max	Units	Conditions
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC mode)	DC 4 DC 4	— — — —	32 8 24 6	MHz MHz MHz MHz	EC, -40°C dTA d+85°C ECPLL, -40°C dTA d+85°C EC, -40°C dTA d+125°C ECPLL, -40°C dTA d+125°C
		Oscillator Frequency	3 3 10 31 3 10	— — — — — —	10 8 32 33 6 24	MHz MHz MHz kHz MHz MHz	XT XTPLL, -40°C dTA d+85°C HS, -40°C dTA d+85°C SOSC XTPLL, -40°C dTA d+125°C HS, -40°C dTA d+125°C
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See parameter OS10 for FOSC value
OS25	TCY	Instruction Cycle Time(2)	62.5	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSCI) High or Low Time	0.45 x TOSC	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSCI) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	6	10	ns	
OS41	TckF	CLKO Fall Time(3)	—	6	10	ns	

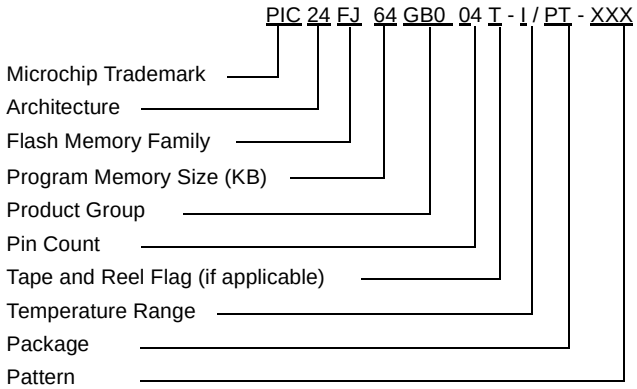
Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Min.” values with an external clock applied to the OSCI/CLKI pin. When an external clock input is used, the “Max.” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSCO pin. CLKO is low for the Q1-Q2 period (1/2 TCY) and high for the Q3-Q4 period (1/2 TCY).

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture	24	= 16-bit modified Harvard without DSP
Flash Memory Family	FJ	= Flash program memory
Product Group	GB0	= General purpose microcontrollers with USB On-The-Go
Pin Count	02	= 28-pin
	04	= 44-pin
Temperature Range	I	= -40 ¢ to +85 ¢ (Industrial)
	E	= -40 ¢ to +125 ¢ (Extended)
Package	ML	= 28-lead (6x6 mm) or 44-lead (8x8 mm) QFN (Quad Flat)
	PT	= 44-lead (10x10x1 mm) TQFP (Thin Quad Flatpack)
	SO	= 28-lead 7.50 mm wide) SOIC (Small Outline)
	SP	= 28-lead (300 mil) SPDIP (Skinny Plastic Dual In-Line)
	SS	= 28-lead (530 mm) SSOP (Plastic Shrink Small)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)	
	ES	= Engineering Sample

Examples:

a) PIC24FJ64GB004-I/PT:
PIC24F device with USB On-The-Go, 64-Kbyte program memory, 44-pin, Industrial temp.,TQFP package.

b) PIC24FJ32GB002-I/ML:
PIC24F device with USB On-The-Go, 32-Kbyte program memory, 28-pin, Industrial temp.,QFN package.