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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64gb002t-i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC24FJ32GB002 PIC24FJ32GB004
- PIC24FJ64GB002 PIC24FJ64GB004

This family expands on the existing line of Microchip's 16-bit microcontrollers, combining an expanded peripheral feature set and enhanced computational performance with a new connectivity option: USB On-The-Go (OTG). The PIC24FJ64GB004 family provides a new platform for high-performance USB applications which may need more than an 8-bit platform, but do not require the power of a digital signal processor.

1.1 Core Features

1.1.1 16-BIT ARCHITECTURE

Central to all PIC24F devices is the 16-bit modified Harvard architecture, first introduced with Microchip's dsPIC[®] digital signal controllers. The PIC24F CPU core offers a wide range of enhancements, such as:

- 16-bit data and 24-bit address paths with the ability to move information between data and memory spaces
- Linear addressing of up to 12 Mbytes (program space) and 64 Kbytes (data)
- A 16-element working register array with built-in software stack support
- A 17 x 17 hardware multiplier with support for integer math
- Hardware support for 32 by 16-bit division
- An instruction set that supports multiple addressing modes and is optimized for high-level languages, such as 'C'
- Operational performance up to 16 MIPS

1.1.2 POWER-SAVING TECHNOLOGY

All of the devices in the PIC24FJ64GB004 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **On-the-Fly Clock Switching:** The device clock can be changed under software control to the Timer1 source or the internal, Low-Power Internal RC Oscillator during operation, allowing the user to incorporate power-saving ideas into their software designs.
- Doze Mode Operation: When timing-sensitive applications, such as serial communications, require the uninterrupted operation of peripherals, the CPU clock speed can be selectively reduced, allowing incremental power savings without missing a beat.

- Instruction-Based Power-Saving Modes: There are three instruction-based power-saving modes:
 - Idle Mode The core is shut down while leaving the peripherals active.
 - Sleep Mode The core and peripherals that require the system clock are shut down, leaving the peripherals active that use their own clock or the clock from other devices.
 - Deep Sleep Mode The core, peripherals (except RTCC and DSWDT), Flash and SRAM are shut down for optimal current savings to extend battery life for portable applications.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC24FJ64GB004 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes using crystals or ceramic resonators.
- Two External Clock modes offering the option of a divide-by-2 clock output.
- A Fast Internal RC Oscillator (FRC) with a nominal 8 MHz output, which can also be divided under software control to provide clock speeds as low as 31 kHz.
- A Phase Lock Loop (PLL) frequency multiplier available to the external oscillator modes and the FRC Oscillator, which allows clock speeds of up to 32 MHz.
- A separate Low-Power Internal RC Oscillator (LPRC) with a fixed 31 kHz output, which provides a low-power option for timing-insensitive applications.

The internal oscillator block also provides a stable reference source for the Fail-Safe Clock Monitor. This option constantly monitors the main clock source against a reference signal provided by the internal oscillator and enables the controller to switch to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve. The consistent pinout scheme used throughout the entire family also aids in migrating from one device to the next larger device.

The PIC24F family is pin-compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30 devices. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

PIC24FJ64GB004 FAMILY

	Р	in Numbe	r	 I/O Input Description				
Function	28-Pin SPDIP/ SOIC/SSOP	28-Pin QFN	44-Pin QFN/TQFP	I/O	Input Buffer	Description		
RA0	2	27	19	I/O	ST	PORTA Digital I/O.		
RA1	3	28	20	I/O	ST			
RA2	9	6	30	I/O	ST			
RA3	10	7	31	I/O	ST			
RA4	12	9	34	I/O	ST			
RA7	_	_	13	I/O	ST			
RA8	—		32	I/O	ST			
RA9	_	_	35	I/O	ST			
RA10	_	_	12	I/O	ST			
RB0	4	1	21	I/O	ST	PORTB Digital I/O.		
RB1	5	2	22	I/O	ST			
RB2	6	3	23	I/O	ST			
RB3	7	4	24	I/O	ST			
RB4	11	8	33	I/O	ST			
RB5	14	11	41	I/O	ST			
RB7	16	13	43	I/O	ST			
RB8	17	14	44	I/O	ST			
RB9	18	15	1	I/O	ST			
RB10	21	18	8	I/O	ST			
RB11	22	19	9	I/O	ST			
RB13	24	21	11	I/O	ST			
RB14	25	22	14	I/O	ST			
RB15	26	23	15	I/O	ST			
RC0	—	_	25	I/O	ST	PORTC Digital I/O.		
RC1	—		26	I/O	ST			
RC2	—	_	27	I/O	ST			
RC3	—	_	36	I/O	ST			
RC4	—	_	37	I/O	ST			
RC5	—	_	38	I/O	ST			
RC6	—	_	2	I/O	ST			
RC7	—		3	I/O	ST			
RC8	—	_	4	I/O	ST			
RC9	—	_	5	I/O	ST			
RCV	18	15	1	I	ST	USB Receive Input (from external transceiver).		
REFO	24	21	11	0	_	Reference Clock Output.		
Logondy T		thuffor			ет -	Sobmitt Triggor input buffor		

TABLE 1-2: PIC24FJ64GB004 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Legend: TTL = TTL input buffer ANA = Analog level input/output ST = Schmitt Trigger input buffer $I^2C^{\text{TM}} = I^2C/\text{SMBus}$ input buffer

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2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1 μ F (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μ F in parallel with 0.001 μ F).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including microcontrollers to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Overstress (EOS). Ensure that the MCLR pin

VIH and VIL specifications are met.

TABLE 4-4: ICN REGISTER MAP

	File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
(CNEN1	0060	CN15IE		CN13IE	CN12IE	CN11IE	CN10IE ⁽¹⁾	CN9IE ⁽¹⁾	CN8IE ⁽¹⁾	CN7IE	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
C	ONEN2	0062	_	CN30IE	CN29IE	CN28IE ⁽¹⁾	CN27IE	CN26IE ⁽¹⁾	CN25IE ⁽¹⁾	_	CN23IE	CN22IE	CN21IE	CN20IE ⁽¹⁾	CN19IE ⁽¹⁾	CN18IE ⁽¹⁾	CN17IE ⁽¹⁾	CN16IE	0000
C	CNPU1	0068	CN15PUE	_	CN13PUE	CN12PUE	CN11PUE	CN10PUE ⁽¹⁾	CN9PUE ⁽¹⁾	CN8PUE ⁽¹⁾	CN7PUE	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
C	ONPU2	006A	_	CN30PUE	CN29PUE	CN28PUE ⁽¹⁾	CN27PUE	CN26PUE ⁽¹⁾	CN25PUE ⁽¹⁾	_	CN23PUE	CN22PUE	CN21PUE	CN20PUE ⁽¹⁾	CN19PUE ⁽¹⁾	CN18PUE ⁽¹⁾	CN17PUE ⁽¹⁾	CN16PUE	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Unimplemented in 28-pin devices; read as '0'.

TABLE 4-18: USB OTG REGISTER MAP (CONTINUED)

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1EP0	04AA	_	_	-	_	_	—	-	—	LSPD ⁽¹⁾	RETRYDIS ⁽¹⁾	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP1	04AC	_	_	_	_	_	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP2	04AE	_	_	_	_	_	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP3	04B0								_		—	-	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP4	04B2	-	_	-	-	-	-	-	—	-	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP5	04B4	-	-			_			—	-	—	-	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP6	04B6								_		—	-	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP7	04B8	-	_	-	-	-	-	-	—	-	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP8	04BA	_	_	_	_	_	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP9	04BC								_		—	-	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP10	04BE	-	_	-	-	-	-	-	—	-	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP11	04C0	_	_	_	_	_	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP12	04C2								_		—	-	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP13	04C4	_	_	_	_	_	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP14	04C6	_	_	_	_	_	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1EP15	04C8	_	_	_	_	_	_	_	_	_	—	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
U1PWMRRS	04CC		U	SB Power	Supply PV	VM Duty C	ycle Regi	ster				USB F	Power Supply P	NM Period Re	egister			0000
U1PWMCON	04CE	PWMEN	_	_	_	_	_	PWMPOL	CNTEN	_	_	_	_	_	_	_	_	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Alternate register or bit definitions when the module is operating in Host mode.

2: This register is available in Host mode only.

TABLE 4-19: PARALLEL MASTER/SLAVE PORT REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON	0600	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN	CSF1	CSF0	ALP	_	CS1P	BEP	WRSP	RDSP	0000
PMMODE	0602	BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0	WAITB1	WAITB0	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1	WAITE0	0000
PMADDR	0604	_	CS1	_	_	_	ADDR10 ⁽¹⁾	ADDR9 ⁽¹⁾	ADDR8 ⁽¹⁾	ADDR7 ⁽¹⁾	ADDR6 ⁽¹⁾	ADDR5 ⁽¹⁾	ADDR4 ⁽¹⁾	ADDR3 ⁽¹⁾	ADDR2 ⁽¹⁾	ADDR1	ADDR0	0000
PMDOUT1			Parallel Port Data Out Register 1 (Buffers 0 and 1) 0000															
PMDOUT2	0606						Pa	rallel Port D	ata Out Reo	gister 2 (Buf	fers 2 and 3)						0000
PMDIN1	0608						Р	arallel Port I	Data In Reg	ister 1 (Buff	ers 0 and 1)							0000
PMDIN2	060A		Parallel Port Data In Register 2 (Buffers 2 and 3) 0000															
PMAEN	060C		PTEN14	_	_	_	PTEN10 ⁽¹⁾	PTEN9 ⁽¹⁾	PTEN8 ⁽¹⁾	PTEN7 ⁽¹⁾	PTEN6 ⁽¹⁾	PTEN5 ⁽¹⁾	PTEN4 ⁽¹⁾	PTEN3 ⁽¹⁾	PTEN2 ⁽¹⁾	PTEN1	PTEN0	0000
PMSTAT	060E	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF		_	OB3E	OB2E	OB1E	OB0E	0000

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Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits are not available on 28-pin devices; read as '0'.

TABLE 4-24: SYSTEM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	_	_	—	DPSLP	CM	PMSLP	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	_	COSC2	COSC1	COSC0	_	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK	LOCK	_	CF	POSCEN	SOSCEN	OSWEN	Note 2
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	RCDIV2	RCDIV1	RCDIV0	CPDIV1	CPDIV0	PLLEN	_	_	_	_	_	0100
OSCTUN	0748	_	_	_	_	_	_	_	_	_	_	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000
REFOCON	074E	ROEN	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	-	—	—	_	_		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The Reset value of the RCON register is dependent on the type of Reset event. See Section 6.0 "Resets" for more information.

2: The Reset value of the OSCCON register is dependent on both the type of Reset event and the device configuration. See Section 8.0 "Oscillator Configuration" for more information.

TABLE 4-25: DEEP SLEEP REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets ⁽¹
DSCON	758	DSEN	—	—	—	—	—	—	—	—	—	—	_	—	—	DSBOR	RELEASE	0000
DSWAKE	075A	_	—	—	—	_	_	_	DSINT0	DSFLT	—	_	DSWDT	DSRTC	DSMCLR	—	DSPOR	0001
DSGPR0	075C		Deep Sleep General Purpose Register 0 0000															
DSGPR1	075E		Deep Sleep General Purpose Register 1 0000															
Legend:	gend: — = unimplemented read as '0'. Reset values are shown in hexadecimal																	

Note 1: The Deep Sleep registers are only reset on a VDD POR event.

TABLE 4-26: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	_	—	—	—	ERASE		_	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000(1)
NVMKEY	0766	_		—	-	—	_	—	_			1	VMKEY R	egister<7:0	>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

8.5 Oscillator Modes and USB Operation

Because of the timing requirements imposed by USB, an internal clock of 48 MHz is required at all times while the USB module is enabled. Since this is well beyond the maximum CPU clock speed, a method is provided to internally generate both the USB and system clocks from a single oscillator source. PIC24FJ64GB004 family devices use the same clock structure as other PIC24FJ devices, but include a two-branch PLL system to generate the two clock signals.

The USB PLL block is shown in Figure 8-2. In this system, the input from the primary oscillator is divided down by a PLL prescaler to generate a 4 MHz output. This is used to drive an on-chip 96 MHz PLL frequency multiplier to drive the two clock branches. One branch uses a fixed, divide-by-2 frequency divider to generate the 48 MHz USB clock. The other branch uses a fixed, divide-by-3 frequency divider and configurable PLL prescaler/divider to generate a range of system clock frequencies. The CPDIV bits select the system clock speed; available clock options are listed in Table 8-2.

The USB PLL prescaler does not automatically sense the incoming oscillator frequency. The user must manually configure the PLL divider to generate the required 4 MHz output using the PLLDIV<2:0> Configuration bits. This limits the choices for primary oscillator frequency to a total of 8 possibilities, shown in Table 8-3.

FIGURE 8-2: USB PLL BLOCK

TABLE 8-2:SYSTEM CLOCK OPTIONS
DURING USB OPERATION

MCU Clock Division (CPDIV<1:0>)	Microcontroller Clock Frequency
None (00)	32 MHz
÷2(01)	16 MHz
÷4 (10)	8 MHz
÷8 (11)	4 MHz

TABLE 8-3:	VALID PRIMARY OSCILLATOR
	CONFIGURATIONS FOR USB
	OPERATIONS

Input Oscillator Frequency	Clock Mode	PLL Division (PLLDIV<2:0>)
48 MHz	ECPLL	÷ 12 (111)
32 MHz	ECPLL	÷8(110)
24 MHz	HSPLL, ECPLL	÷6(101)
20 MHz	HSPLL, ECPLL	÷5(100)
16 MHz	HSPLL, ECPLL	÷4(011)
12 MHz	HSPLL, ECPLL	÷3(010)
8 MHz	XTPLL, ECPLL	÷2(001)
4 MHz	XTPLL, ECPLL	÷1 (000)



8.5.1 CONSIDERATIONS FOR USB OPERATION

When using the USB On-The-Go module in PIC24FJ64GB004 family devices, users must always observe these rules in configuring the system clock:

- For USB operation, the selected clock source (EC, HS or XT) must meet the USB clock tolerance requirements.
- The Primary Oscillator/PLL modes are the only oscillator configurations that permit USB operation. There is no provision to provide a separate external clock source to the USB module.
- All oscillator modes are available; however, USB operation is not possible when these modes are selected. They may still be useful in cases where other power levels of operation are desirable and the USB module is not needed (e.g., the application is Sleeping and waiting for bus attachment).

9.2.4.3 Exiting Deep Sleep Mode

Deep Sleep mode exits on any one of the following events:

- POR event on VDD supply. If there is no DSBOR circuit to re-arm the VDD supply POR circuit, the external VDD supply must be lowered to the natural arming voltage of the POR circuit.
- DSWDT time-out. When the DSWDT timer times out, the device exits Deep Sleep.
- RTCC alarm (if RTCEN = 1).
- Assertion ('0') of the $\overline{\text{MCLR}}$ pin.
- Assertion of the INT0 pin (if the interrupt was enabled before Deep Sleep mode was entered). The polarity configuration is used to determine the assertion level ('0' or '1') of the pin that will cause an exit from Deep Sleep mode. Exiting from Deep Sleep mode requires a change on the INT0 pin while in Deep Sleep mode.

Note: Any interrupt pending when entering Deep Sleep mode is cleared.

Exiting Deep Sleep mode generally does not retain the state of the device and is equivalent to a Power-on Reset (POR) of the device. Exceptions to this include the RTCC (if present), which remains operational through the wake-up, the DSGPRx registers and DSWDT.

Wake-up events that occur from the time Deep Sleep exits, until the time that the POR sequence completes, are ignored and are not captured in the DSWAKE register.

The sequence for exiting Deep Sleep mode is:

- 1. After a wake-up event, the device exits Deep Sleep and performs a POR. The DSEN bit is cleared automatically. Code execution resumes at the Reset vector.
- To determine if the device exited Deep Sleep, read the Deep Sleep bit, DPSLP (RCON<10>). This bit will be set if there was an exit from Deep Sleep mode. If the bit is set, clear it.
- 3. Determine the wake-up source by reading the DSWAKE register.
- 4. Determine if a DSBOR event occurred during Deep Sleep mode by reading the DSBOR bit (DSCON<1>).
- If application context data has been saved, read it back from the DSGPR0 and DSGPR1 registers.
- 6. Clear the RELEASE bit (DSCON<0>).

9.2.4.4 Deep Sleep Wake-up Time

Since wake-up from Deep Sleep results in a POR, the wake-up time from Deep Sleep is the same as the device POR time. Also, because the internal regulator is turned off, the voltage on VCAP may drop depending on how long the device is asleep. If VCAP has dropped below 2V, then there will be additional wake-up time while the regulator charges VCAP.

Deep Sleep wake-up time is specified in **Section 29.0 "Electrical Characteristics"** as TDSWU. This specification indicates the worst case wake-up time, including the full POR Reset time (including TPOR and TRST), as well as the time to fully charge a 10 μ F capacitor on VCAP which has discharged to 0V. Wake-up may be significantly faster if VCAP has not discharged.

9.2.4.5 Saving Context Data with the DSGPR0/DSGPR1 Registers

As exiting Deep Sleep mode causes a POR, most Special Function Registers reset to their default POR values. In addition, because VDDCORE power is not supplied in Deep Sleep mode, information in data RAM may be lost when exiting this mode.

Applications which require critical data to be saved prior to Deep Sleep may use the Deep Sleep General Purpose registers, DSGPR0 and DSGPR1, or data EEPROM (if available). Unlike other SFRs, the contents of these registers are preserved while the device is in Deep Sleep mode. After exiting Deep Sleep, software can restore the data by reading the registers and clearing the RELEASE bit (DSCON<0>).

9.2.4.6 I/O Pins During Deep Sleep Mode

During Deep Sleep, the general purpose I/O pins retain their previous states and the Secondary Oscillator (SOSC) will remain running, if enabled. Pins that are configured as inputs (TRIS bit set) prior to entry into Deep Sleep remain high-impedance during Deep Sleep. Pins that are configured as outputs (TRIS bit clear) prior to entry into Deep Sleep remain as output pins during Deep Sleep. While in this mode, they continue to drive the output level determined by their corresponding LAT bit at the time of entry into Deep Sleep.

16.2 Setting Baud Rate When Operating as a Bus Master

To compute the Baud Rate Generator (BRG) reload value, use Equation 16-1.

EQUATION 16-1: COMPUTING BAUD RATE RELOAD VALUE^(1,2)

 $FSCL = \frac{FCY}{I2CxBRG + 1 + \frac{FCY}{10,000,000}}$ or $I2CxBRG = \left(\frac{FCY}{FSCL} - \frac{FCY}{10,000,000}\right) - 1$

Note 1: Based on FCY = FOSC/2, Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system level parameters. The actual clock rate should be measured in its intended application.

TABLE 16-1: I²C[™] CLOCK RATES^(1,2)

16.3 Slave Address Masking

The I2CxMSK register (Register 16-3) designates address bit positions as "don't care" for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= 1) in the I2CxMSK register causes the slave module to respond whether the corresponding address bit value is a '0' or a '1'. For example, when I2CxMSK is set to '00100000', the slave module will detect both addresses: '0000000' and '0100000'.

To enable address masking, the IPMI (Intelligent Peripheral Management Interface) must be disabled by clearing the IPMIEN bit (I2CxCON<11>).

Note: As a result of changes in the I²C[™] protocol, the addresses in Table 16-2 are reserved and will not be Acknowledged in Slave mode. This includes any address mask settings that include any of these addresses.

Dequired System Fool	For	I2CxBF	RG Value	
Required System FSCL	FCT	(Decimal)	(Hexadecimal)	
100 kHz	16 MHz	157	9D	100 kHz
100 kHz	8 MHz	78	4E	100 kHz
100 kHz	4 MHz	39	27	99 kHz
400 kHz	16 MHz	37	25	404 kHz
400 kHz	8 MHz	18	12	404 kHz
400 kHz	4 MHz	9	9	385 kHz
400 kHz	2 MHz	4	4	385 kHz
1 MHz	16 MHz	13	D	1.026 MHz
1 MHz	8 MHz	6	6	1.026 MHz
1 MHz	4 MHz	3	3	0.909 MHz

Note 1: Based on FCY = FOSC/2, Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system level parameters. The actual clock rate should be measured in its intended application.

TABLE 16-2: I²C[™] RESERVED ADDRESSES⁽¹⁾

Slave Address	R/W Bit	Description
0000 000	0	General Call Address ⁽²⁾
0000 000	1	Start Byte
0000 001	x	Cbus Address
0000 010	x	Reserved
0000 011	x	Reserved
0000 1xx	x	HS Mode Master Code
1111 1xx	x	Reserved
1111 0xx	x	10-Bit Slave Upper Byte ⁽³⁾

Note 1: The address bits listed here will never cause an address match, independent of address mask settings.

2: The address will be Acknowledged only if GCEN = 1.

3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

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REGISTER 18-18: U1IE: USB INTERRUPT ENABLE REGISTER (ALL USB MODES)

					<u>.</u>			
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	—	—	—	—	—	—	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
STALLIE	ATTACHIE ⁽¹⁾ RESUMEIE IDLEIE TRNIE SOFIE UERRIE URST							
							DETACHIE	
bit 7							bit 0	
L								
Legend:								
R = Readable	e bit	W = Writable b	bit	U = Unimplem	nented bit, read	d as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown	
			,					
DIT 15-8		ted: Read as '0	Intornet E	able bit				
	SIALLIE: STALL Handshake Interrupt Enable bit							
	0 = Interrupt is disabled							
bit 6	ATTACHIE: Peripheral Attach Interrupt bit (Host mode only) ⁽¹⁾							
	1 = Interrupt is enabled							
	0 = Interrupt is disabled							
bit 5	RESUMEIE: Resume Interrupt bit							
	1 = Interrupt	is enabled						
hit 4		is uisauleu Detect Interrunt	hit					
		is enabled	DIL					
	0 = Interrupt is disabled							
bit 3	TRNIE: Toker	n Processing Co	mplete Interru	upt bit				
	1 = Interrupt	is enabled						
	0 = Interrupt	is disabled						
bit 2	SOFIE: Start-	of-Frame Toker	Interrupt bit					
	1 = Interrupt	is enabled disabled						
bit 1		B Frror Conditio	n Interrunt hit					
	1 = Interrupt	is enabled						
	0 = Interrupt	is disabled						
bit 0	URSTIE or D Enable bit	ETACHIE: USI	B Reset Interi	rupt (Device mo	ode) or USB [Detach Interrup	t (Host mode)	
	1 = Interrupt	is enabled						
	0 = Interrupt	is disabled						

Note 1: Unimplemented in Device mode; read as '0'.

REGISTER 20-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾ (CONTINUED)

bit 7-0	CAL<7:0>: RTC Drift Calibration bits
	01111111 = Maximum positive adjustment; adds 508 RTC clock pulses every one minute
	01111111 = Minimum positive adjustment; adds 4 RTC clock pulses every one minute 00000000 = No adjustment
	11111111 = Minimum negative adjustment; subtracts 4 RTC clock pulses every one minute
	•
	10000000 = Maximum negative adjustment; subtracts 512 RTC clock pulses every one minute

- Note 1: The RCFGCAL register is only affected by a POR.
 - 2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
 - 3: This bit is read-only; it is cleared to '0' on a write to the lower half of the MINSEC register.

REGISTER 20-2: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	_	—	_	—	RTSECSEL1 ⁽¹⁾	RTSECSEL0 ⁽¹⁾	PMPTTL
bit 7					•		bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	

-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3	Unimplemented: Read as '0'
----------	----------------------------

bit 2-1	RTSECSEL<1:0>: RTCC Seconds Clock Output Select bits ⁽¹⁾
---------	---

- 11 = Reserved; do not use
 - 10 = RTCC source clock is selected for the RTCC pin (clock can be LPRC or SOSC, depending on the setting of the RTCOSC bit (CW4<5>))
 - 01 = RTCC seconds clock is selected for the RTCC pin
- 00 = RTCC alarm pulse is selected for the RTCC pin

bit 0 **PMPTTL:** PMP Module TTL Input Buffer Select bit

- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffers



21.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the "PIC24F Family Reference Manual", Section 41. "32-Bit Programmable Cyclic Redundancy Check (CRC)" (DS39729). The programmable CRC generator provides a hardware-implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- · Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- · Configurable Interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 21-1. A simple version of the CRC shift engine is shown in Figure 21-2.



FIGURE 21-2: CRC SHIFT ENGINE DETAIL



FIGURE 21-1: CRC BLOCK DIAGRAM

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R/W-0	R/W-0	R/W-0	R/W-0 ⁽¹⁾	R/W-0	R/W-0	R/W-0	R/W-0
CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8 ⁽¹⁾
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0
bit 7	7 bi						bit 0
Legend:							
R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'					l as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unki	nown
bit 15	CSSL15: A/D Input Band Gap Scan Enable bit						
	 1 = Internal band gap (VBG) channel is enabled for input scan 0 = Analog channel is disabled from input scan 						
bit 14	CSSL14: A/D Input Half Band Gap Scan Enable bit						
	1 = Internal half band gap (VBG/2) channel is enabled for input scan						
	0 = Analog channel is disabled from input scan						
bit 13	CSSL13: A/D Input Voltage Regulator Output Scan Enable bit						
	 1 = Internal voltage regulator output (VDDCORE) is enabled for input scan 0 = Analog channel is disabled from input scan 						
bit 12-0	CSSL<12:0>	: A/D Input Pin	Scan Selection	n bits ⁽¹⁾			
	 1 = Corresponding analog channel is selected for input scan 0 = Analog channel is omitted from input scan 						

REGISTER 22-6: AD1CSSL: A/D INPUT SCAN SELECT REGISTER

Note 1: Analog channels, AN6, AN7, AN8 and AN12, are unavailable on 28-pin devices; leave these corresponding bits cleared.

25.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's internal capacitor (CAD) and a precision resistor for current calibration. Figure 25-2 shows the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTEDG pins, but other configurations using internal edge sources are possible. For the smallest time measurements, select the internal A/D Channel 31, CH0S<4:0> = 11111. This minimizes any stray capacitance that may otherwise be associated with using an input pin, thus keeping the total capacitance to that of the A/D Converter itself (4-5 pF). A detailed discussion on measuring capacitance and time with the CTMU module is provided in the "PIC24F Family Reference Manual".

25.3 Pulse Generation and Delay

The CTMU module can also generate an output pulse with edges that are not synchronous with the device's system clock. More specifically, it can generate a pulse with a programmable delay from an edge event input to the module.

When the module is configured for pulse generation delay by setting the TGEN bit (CTMUCON<12>), the internal current source is connected to the B input of Comparator 2. A capacitor (CDELAY) is connected to the Comparator 2 pin, C2INB, and the comparator voltage reference, CVREF, is connected to C2INA. CVREF is then configured for a specific trip point. The module begins to charge CDELAY when an edge event is detected. When CDELAY charges above the CVREF trip point, a pulse is output on CTPLS. The length of the pulse delay is determined by the value of CDELAY and the CVREF trip point.

Figure 25-3 shows the external connections for pulse generation, as well as the relationship of the different analog modules required. While CTEDG1 is shown as the input pulse source, other options are available. A detailed discussion on pulse generation with the CTMU module is provided in the "*PIC24F Family Reference Manual*".

FIGURE 25-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT



FIGURE 25-3: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR PULSE DELAY GENERATION



REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

- bit 3-2
 EDG1SEL<1:0>: Edge 1 Source Select bits

 11 = CTED1 pin
 10 = CTED2 pin

 01 = OC1 module
 00 = Timer1 module

 bit 1
 EDG2STAT: Edge 2 Status bit

 1 = Edge 2 event has occurred
 0 = Edge 2 event has not occurred

 bit 0
 EDG1STAT: Edge 1 Status bit

 1 = Edge 1 event has occurred
 0 = Edge 1 event has not occurred
- **Note 1:** If TGEN = 1, the peripheral inputs and outputs must be configured to an available RPn pin. For more information, see Section 10.4 "Peripheral Pin Select (PPS)".

REGISTER 25-2: CTMUICON: CTMU CURRENT CONTROL REGIST
--

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 15						•	bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—		—	—	—	—
bit 7			•			•	bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown			nown	
bit 15-10 ITRIM<5:0>: Current Source Trim bits 011111 = Maximum positive change from nominal current 011110 000001 = Minimum positive change from nominal current 000000 = Nominal current output specified by IRNG<1:0> 111111 = Minimum negative change from nominal current 100010							
bit 9-8 bit 7-0	IRNG<1:0>: Current Source Range Select bits 11 = 100 × Base Current 10 = 10 × Base Current 01 = Base current level (0.55 μ A nominal) 00 = Current source disabled Unimplemented: Read as '0'						

26.0 SPECIAL FEATURES

- Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the following sections of the "PIC24F Family Reference Manual":
 Section 9. "Watchdog Timer (WDT)" (DS39697)
 - Section 32. "High-Level Device Integration" (DS39719)
 - Section 33. "Programming and Diagnostics" (DS39716)

PIC24FJ64GB004 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection
- · JTAG Boundary Scan Interface
- In-Circuit Serial Programming
- In-Circuit Emulation

26.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location F80000h. A detailed explanation of the various bit functions is provided in Register 26-1 through Register 26-6.

Note that address F80000h is beyond the user program memory space. In fact, it belongs to the configuration memory space (800000h-FFFFFFh) which can only be accessed using table reads and table writes.

26.1.1 CONSIDERATIONS FOR CONFIGURING PIC24FJ64GB004 FAMILY DEVICES

In PIC24FJ64GB004 family devices, the configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in the three words at the top of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 26-1. These are packed representations of the actual device Configuration bits, whose actual locations are distributed among several locations in configuration space. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Word for configuration data. This is to make certain that program code is not stored in this address when the code is compiled.

The upper byte of all Flash Configuration Words in program memory should always be '1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

TABLE 26-1: FLASH CONFIGURATION WORD LOCATIONS FOR PIC24FJ64GB004 FAMILY DEVICES DEVICES

Daviaa	Configuration Word Addresses						
Device	1	2	3	4			
PIC24FJ32GB00X	57FEh	57FCh	57FAh	57F8h			
PIC24FJ64GB00X	ABFEh	ABFCh	ABFAh	ABF8h			

REGISTER 26-2: CW2: FLASH CONFIGURATION WORD 2 (CONTINUED)

- bit 4 IOL1WAY: IOLOCK One-Way Set Enable bit
 - 1 = The IOLOCK bit (OSCCON<6>) can be set once, provided the unlock sequence has been completed. Once set, the Peripheral Pin Select registers cannot be written to a second time.
 - 0 = The IOLOCK bit can be set and cleared as needed, provided the unlock sequence has been completed
- bit 3 Unimplemented: Read as '1'
- bit 2 I2C1SEL: I2C1 Pin Select bit
 - 1 = Use default SCL1/SDA1 pins
 - 0 = Use alternate SCL1/SDA1 pins
- bit 1-0 **POSCMD<1:0>:** Primary Oscillator Configuration bits
 - 11 = Primary Oscillator is disabled
 - 10 = HS Oscillator mode is selected
 - 01 = XT Oscillator mode is selected
 - 00 = EC Oscillator mode is selected

PIC24FJ64GB004 FAMILY

29.1 DC Characteristics





FIGURE 29-2: PIC24FJ64GB004 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED TEMPERATURE)



DC CH/	ARACT	ERISTICS	Standard Operating Conditions: 2.0V to 3.6V (unless stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Inc $-40^{\circ}C \le TA \le +125^{\circ}C$ for E			V (unless otherwise C for Industrial 5°C for Extended	
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Мах	Units	Conditions
-	VIL	Input Low Voltage ⁽⁴⁾					
DI10		I/O Pins with ST Buffer	Vss	—	0.2 VDD	V	
DI11		I/O Pins with TTL Buffer	Vss	—	0.15 VDD	V	
DI15		MCLR	Vss	_	0.2 VDD	V	
DI16		OSC1 (XT mode)	Vss	—	0.2 VDD	V	
DI17		OSC1 (HS mode)	Vss	_	0.2 VDD	V	
DI18		I/O Pins with I ² C™ Buffer:	Vss	—	0.3 VDD	V	
DI19		I/O Pins with SMBus Buffer:	Vss	_	0.8	V	SMBus enabled
	VIH	Input High Voltage ⁽⁴⁾					
DI20		I/O Pins with ST Buffer:	0.01/5-5) <i>(</i> = =		
		with Analog Functions,		_	VDD 55	V	
121		I/O Pins with TTL Buffer	0.0 100		0.0	v	
		with Analog Functions,	0.25 VDD + 0.8	_	Vdd	V	
		Digital Only	0.25 VDD + 0.8	—	5.5	V	
DI25		MCLR	0.8 VDD	—	Vdd	V	
DI26		OSC1 (XT mode)	0.7 VDD	—	Vdd	V	
DI27		OSC1 (HS mode)	0.7 VDD	—	Vdd	V	
DI28		I/O Pins with I ² C Buffer:					
		with Analog Functions,		—	VDD	V	
0120		Digital Office	0.7 VDD	_	5.5	v	
DI29		with Analog Functions.	2.1		VDD	V	$2.5V \leq VPIN \leq VDD$
		Digital Only	2.1		5.5	V	
DI30	ICNPU	CNx Pull-up Current	50	250	400	μA	VDD = 3.3V, VPIN = VSS
	lı∟	Input Leakage Current ^(2,3)					
DI50		I/O Ports	—	—	<u>+</u> 50	nA	$VSS \leq VPIN \leq VDD,$
							Pin at high-impedance
DI51		Analog Input Pins	—	—	<u>+</u> 50	nA	$Vss \le VPIN \le VDD$, Pin at high-impedance
DI52		USB Differential Pins	—	—	<u>+</u> 50	nA	$V \text{USB} \geq V \text{DD}$
DI55		MCLR	_	_	<u>+</u> 50	nA	$VSS \leq VPIN \leq VDD$
DI56		OSC1	—	—	<u>+</u> 50	nA	$Vss \le VPIN \le VDD,$ XT and HS modes

TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Refer to Table 1-2 for I/O pins buffer types.

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