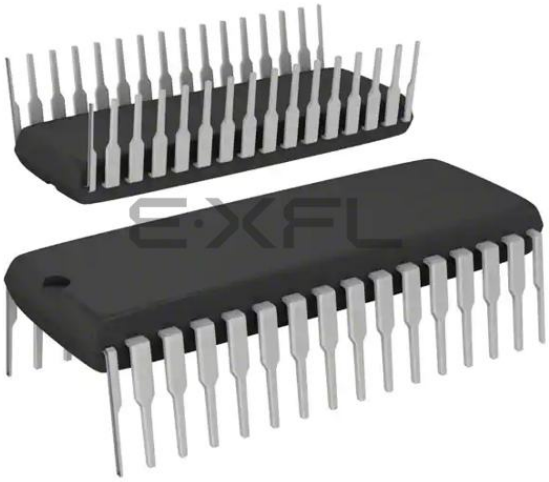

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite49k2b6

List of tables

3 Register and memory mapping

As shown in *Figure 4*, the MCU is capable of addressing 64 Kbytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, 384 bytes of RAM, 256 bytes of data EEPROM and 8 Kbytes of Flash program memory. The RAM space includes up to 128 bytes for the stack from 180h to 1FFh.

The highest address bytes contain the user reset and interrupt vectors.

The Flash memory contains two sectors (see) mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (FFE0h-FFFFh).

The size of Flash Sector 0 and other device options are configurable by option bytes (refer to *Section 14.1 on page 230*).

Caution: Memory locations marked as “Reserved” must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Table 3. Hardware register map(1)

Address	Block	Register label	Register name	Reset status	Remarks
0000h 0001h 0002h	Port A	PADR PADDR PAOR	Port A Data register Port A Data Direction register Port A Option register	00h 00h 00h	R/W R/W R/W
0003h 0004h 0005h	Port B	PBDR PBDDR PBOR	Port B Data register Port B Data Direction register Port B Option register	00h 00h 00h	R/W R/W R/W
0006h 0007h 0008h	Port C	PCDR PCDDR PCOR	Port C Data register Port C Data Direction register Port C Option register	00h 00h 08h	R/W R/W R/W
0009h to 000Bh	Reserved area (3 bytes)				
000Ch 000Dh 000Eh 000Fh 0010h	LITE TIMER	LTCSR2 LTARR LTCNTR LTCSR1 LTICR	Lite Timer Control/Status register 2 Lite Timer Auto-reload register Lite Timer Counter register Lite Timer Control/Status register 1 Lite Timer Input Capture register	0Fh 00h 00h 0x00 0000b xxh	R/W R/W Read Only R/W Read Only

Bit 3 = **I** *Interrupt mask bit*

This bit is set by hardware when entering in interrupt or by software to disable all interrupts except the TRAP software interrupt. This bit is cleared by software.

0: Interrupts are enabled.

1: Interrupts are disabled.

This bit is controlled by the RIM, SIM and IRET instructions and is tested by the JRM and JRNM instructions.

Note: Interrupts requested while I is set are latched and can be processed when I is cleared. By default an interrupt routine is not interruptible because the I bit is set by hardware at the start of the routine and reset by the IRET instruction at the end of the routine. If the I bit is cleared by software in the interrupt routine, pending interrupts are serviced regardless of the priority level of the current interrupt routine.

Bit 2 = **N** *Negative bit*

This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It is a copy of the 7^{th} bit of the result.

0: The result of the last operation is positive or null.

1: The result of the last operation is negative (that is, the most significant bit is a logic 1).

This bit is accessed by the JRMI and JRPL instructions.

Bit 1 **= Z** *Zero bit*

This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

0: The result of the last operation is different from zero.

1: The result of the last operation is zero.

This bit is accessed by the JREQ and JRNE test instructions.

Bit 0 = **C** *Carry/borrow bit*

This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.

0: No overflow or underflow has occurred.

1: An overflow or underflow has occurred.

This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the “bit test and branch”, shift and rotate instructions.

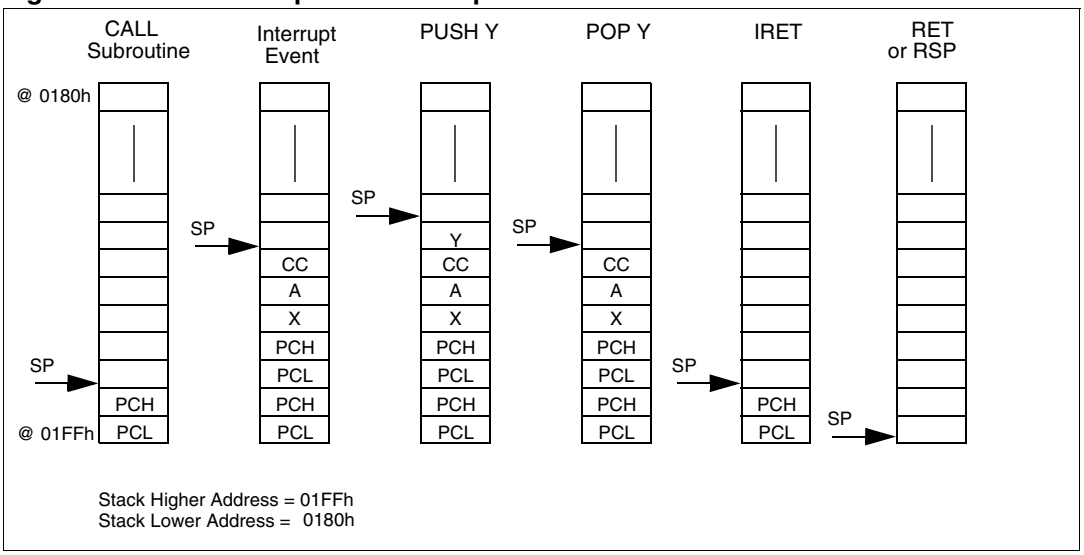
Interrupt management bits

Bits 5,3 = **I1, I0** *Interrupt bits*

The combination of the I1 and I0 bits gives the current interrupt software priority.

These two bits are set/cleared by hardware when entering in interrupt. The loaded value is given by the corresponding bits in the interrupt software priority registers (IxSPR). They can be also set/cleared by software with the RIM, SIM, IRET, HALT, WFI and PUSH/POP instructions. See *Section 10.6: Interrupts* for more details.

Figure 11. Stack manipulation example



Bit 0 = **AVDIE** *Voltage detector interrupt enable bit*

This bit is set and cleared by software. It enables an interrupt to be generated when the AVDF flag is set. The pending interrupt information is automatically cleared when software enters the AVD interrupt routine.

0: AVD interrupt disabled

1: AVD interrupt enabled

7.5.4 AVD threshold selection register (AVDTHCR)

Reset value: 0000 0011 (003h)

7							0
CK2	CK1	CK0	0	0	0	AVD1	AVD0
Read/write							

Bits 7:5 = **CK[2:0]** internal RC prescaler selection

These bits are set by software and cleared by hardware after a reset. These bits select the prescaler of the internal RC oscillator. See *Figure 13: Clock management block diagram on page 41* and *Table 11*.

If the internal RC is used with a supply operating range below 3.3 V, a division ratio of at least 2 must be enabled in the RC prescaler.

Table 11. Internal RC prescaler selection bits

CK2	CK1	CK0	f_{OSC}
0	0	1	$f_{RC/2}$
0	1	0	$f_{RC/4}$
0	1	1	$f_{RC/8}$
1	0	0	$f_{RC/16}$
others			f_{RC}

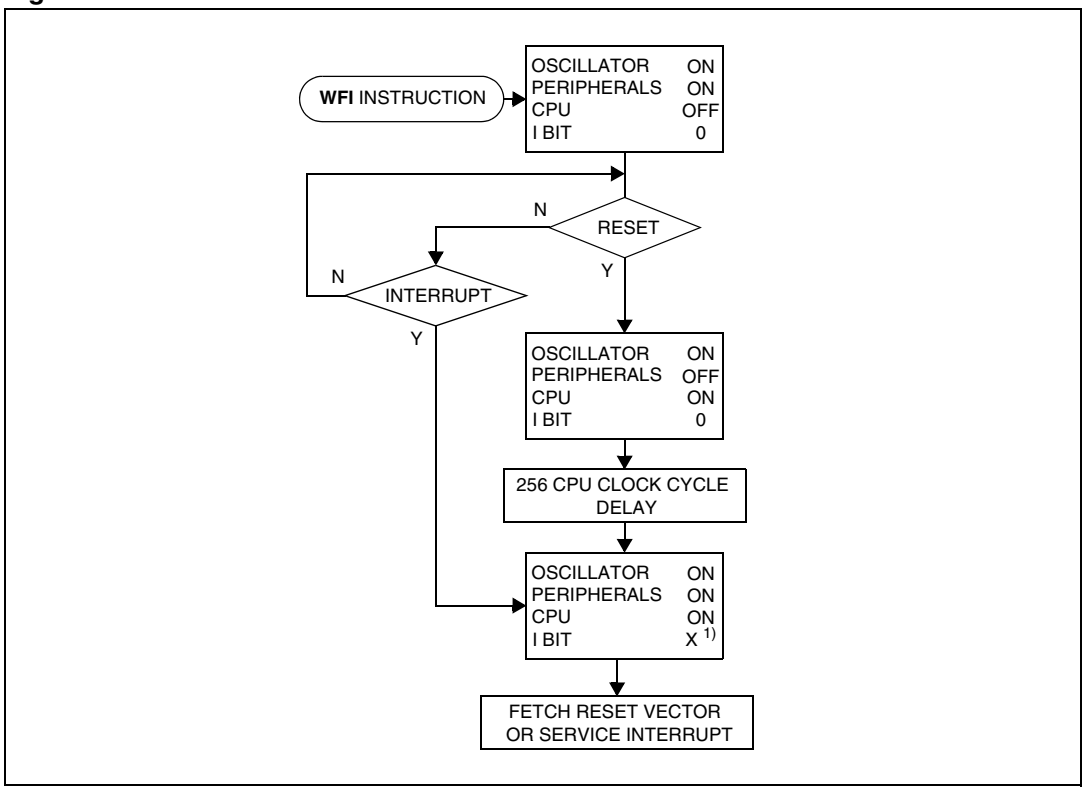
Bits 4:2 = Reserved, must be cleared.

Bits 1:0 = AVD[1:0] AVD Threshold selection. These bits are used to select the AVD threshold. They are set and cleared by software. They are set by hardware after a reset.

Table 12. AVD threshold selection bits

AVD1	AVD0	Functionality
0	0	Low
0	1	Medium
1	0	High
1	1	AVD off

Figure 26. Wait mode flowchart



1. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

9.4 Active-halt and Halt modes

Active-Halt and Halt modes are the two lowest power consumption modes of the MCU. They are both entered by executing the 'HALT' instruction. The decision to enter either in Active-Halt or Halt mode is given by the LTCSR/ATCSR register status as shown in the following table:

Table 20. Enabling/disabling Active-halt and Halt modes

LTCSR TBIE bit	ATCSR OVFIE bit	ATCSRCK1 bit	ATCSRCK0 bit	Meaning
0	x	x	0	Active-halt mode disabled
0	0	x	x	
0	1	1	1	
1	x	x	x	Active-halt mode enabled
x	1	0	1	

One pulse mode

One pulse mode can be used to control PWM2/3 signal with an external LTIC pin. This mode is available only in Dual Timer mode i.e. only for CNTR2, when the OP_EN bit in PWM3CSR register is set.

One Pulse mode is activated by the external LTIC input. The active edge of the LTIC pin is selected by the OPEDGE bit in the PWM3CSR register.

After getting the active edge of the LTIC pin, CNTR2 is reset (000h) and PWM3 is set to high. CNTR2 starts counting from 000h, when it reaches the active DCR3 value then PWM3 goes low. Till this time, any further transitions on the LTIC signal will have no effect. If there are LTIC transitions after CNTR2 reaches DCR3 value, CNTR2 is reset again and PWM3 goes high.

If there is no LTIC active edge, CNTR2 counts until it reaches the ATR2 value, then it is reset again and PWM3 is set to high. The counter again starts counting from 000h, when it reaches the active DCR3 value PWM3 goes low, the counter counts until it reaches ATR2, it resets and PWM3 is set to high and so on.

The same operation applies for PWM2, but in this case the comparison is done on DCR2. OP_EN and OPEDGE bits take effect on the fly and are not synchronized with Counter 2 overflow. The output bit OP2/3 can be used to inverse the polarity of PWM2/3 in one-pulse mode. The update of these bits (OP2/3) is synchronized with the counter 2 overflow, they will be updated if the TRAN2 bit is set.

The time taken from activation of LTIC input and CNTR2 reset is between 2 and 3 t_{CNTR2} cycles, that is, from around 62.5 ns to 94 ns (at 32 MHz input frequency).

Lite timer Input Capture interrupt should be disabled while 12-bit ARtimer is in One Pulse mode. This is to avoid spurious interrupts.

The priority of the various conditions for PWM3 is the following: Break > one-pulse mode with active LTIC edge > Forced overflow by s/w > one-pulse mode without active LTIC edge > normal PWM operation.

It is possible to update DCR2/3 and OP2/3 at the counter 2 reset, the update is synchronized with the counter reset. This is managed by the overflow interrupt which is generated if counter is reset either due to ATR match or active pulse at LTIC pin. DCR2/3 and OP2/3 update in one-pulse mode is performed dynamically using a software force update. DCR3 update in this mode is not synchronized with any event. That may lead to a longer next PWM3 cycle duration than expected just after the change.

In One Pulse mode ATR2 value must be greater than DCR2/3 value for PWM2/3. (opposite to normal PWM mode).

If there is an active edge on the LTIC pin after the counter has reset due to an ATR2 match, then the timer again gets reset and appears as modified Duty cycle depending on whether the new DCR value is less than or more than the previous value.

The TRAN2 bit should be set along with the FORCE2 bit with the same instruction after a write to the DCR register.

ATR2 value should be changed after an overflow in one pulse mode to avoid any irregular PWM cycle.

When exiting from one pulse mode, the OP_EN bit in the PWM3CSR register should be reset first and then the ENCNTR2 bit (if counter 2 must be stopped).

Bits 4:3 = **CK[1:0]** *Counter clock selection bits*

These bits are set and cleared by software and cleared by hardware after a reset. they select the clock frequency of the counter.

Table 37. Counter clock selection

Counter clock selection	CK1	CK0
OFF	0	0
32 MHz	1	1
f_{LTIMER} (1 ms timebase @ 8 MHz)	0	1
f_{CPU}	1	0

Bit 2 = **OVF1** *Overflow flag*

This bit is set by hardware and cleared by software by reading the ATCSR register. It indicates the transition of the Counter1 CNTR1 from FFFh to ATR1 value.

0: No Counter Overflow Occurred

1: Counter Overflow Occurred

Bit 1 = **OVFIE1** *Overflow Interrupt Enable bit*

This bit is read/write by software and cleared by hardware after a reset.

0: Overflow Interrupt Disabled.

1: Overflow Interrupt Enabled.

Bit 0 = **CMPIE** *Compare Interrupt Enable bit*

This bit is read/write by software and cleared by hardware after a reset. it can be used to mask the interrupt generated when any of the cmpfx bit is set.

0: Output Compare Interrupt Disabled.

1: Output Compare Interrupt Enabled.

Counter register 1 high (CNTR1H)

Reset value: 0000 0000 (00h)

15							8
0	0	0	0	CNTR1_11	CNTR1_10	CNTR1_9	CNTR1_8
Read only							

Counter register 1 low (CNTR1L)

Reset value: 0000 0000 (00h)

7							0
CNTR1_7	CNTR1_6	CNTR1_5	CNTR1_4	CNTR1_3	CNTR1_2	CNTR1_1	CNTR1_0
Read only							

Bits 15:12 = Reserved

Bit 6 = **ICF** *Input capture flag*

This bit is set by hardware and cleared by software by reading the LTICR register. Writing to this bit does not change the bit value.

0: No Input Capture

1: An Input Capture has occurred

Note: After an MCU reset, software must initialize the ICF bit by reading the LTICR register

Bit 5 = **TB** *Timebase period selection bit*

This bit is set and cleared by software.

0: Timebase period = t_{OSC} * 8000 (1 ms @ 8 MHz)

1: Timebase period = t_{OSC} * 16000 (2 ms @ 8 MHz)

Bit 4 = **TB1IE** *Timebase Interrupt enable bit*

This bit is set and cleared by software.

0: Timebase (TB1) interrupt disabled

1: Timebase (TB1) interrupt enabled

Bit 3 = **TB1F** *Timebase Interrupt flag*

This bit is set by hardware and cleared by software reading the LTCSR register. Writing to this bit has no effect.

0: No counter overflow

1: A counter overflow has occurred

Bits 2:0 = Reserved, must be kept cleared.

Lite timer input capture register (LTICR)

Reset value: 0000 0000 (00h)

7							0
ICR7	ICR6	ICR5	ICR4	ICR3	ICR2	ICR1	ICR0
Read only							

Bits 7:0 = **ICR[7:0]** *Input Capture value*

These bits are read by software and cleared by hardware after a reset. If the ICF bit in the LTCSR is cleared, the value of the 8-bit up-counter will be captured when a rising or falling edge occurs on the LTIC pin.

Table 41. Lite timer register mapping and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0C	**LTCSR2** Reset Value	0	0	0	0	0	0	TB2IE 0	TB2F 0
0D	**LTARR** Reset Value	AR7 0	AR6 0	AR5 0	AR4 0	AR3 0	AR2 0	AR1 0	AR0 0
0E	**LTCNTR** Reset Value	CNT7 0	CNT6 0	CNT5 0	CNT4 0	CNT3 0	CNT2 0	CNT1 0	CNT0 0

11.5.4 Functional description

Refer to the CR, SR1 and SR2 registers in *Section 11.5.7*. for the bit definitions.

By default the I^2C interface operates in Slave mode (M/SL bit is cleared) except when it initiates a transmit or receive sequence.

First the interface frequency must be configured using the FRi bits in the OAR2 register.

Slave mode

As soon as a start condition is detected, the address is received from the SDA line and sent to the shift register; then it is compared with the address of the interface or the General Call address (if selected by software).

Note: In 10-bit addressing mode, the comparison includes the header sequence (11110xx0) and the two most significant bits of the address.

- **Header matched** (10-bit mode only): the interface generates an acknowledge pulse if the ACK bit is set.
- **Address not matched**: the interface ignores it and waits for another Start condition.
- **Address matched**: the interface generates in sequence:
  - Acknowledge pulse if the ACK bit is set.
  - EVF and ADSL bits are set with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register, **holding the SCL line low** (see *Figure 71* Transfer sequencing EV1).
Next, in 7-bit mode read the DR register to determine from the least significant bit (Data Direction Bit) if the slave must enter Receiver or Transmitter mode.

In 10-bit mode, after receiving the address sequence the slave is always in receive mode. It will enter transmit mode on receiving a repeated Start condition followed by the header sequence with matching address bits and the least significant bit set (11110xx1).

Slave receiver

Following the address reception and after SR1 register has been read, the **slave receives bytes from the SDA line into the** DR register **via** the internal shift register. After each byte the interface generates in sequence:

- Acknowledge pulse if the ACK bit is set
- EVF and BTF bits are set with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register followed by a read of the DR register, **holding the SCL line low** (see *Figure 71* Transfer sequencing EV2).

Slave transmitter

Following the address reception and after SR1 register has been read, **the slave sends bytes from** the DR register to **the SDA line** via the internal shift register.

The slave waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see *Figure 71* Transfer sequencing EV3).

When the acknowledge pulse is received the EVF and BTF bits are set by hardware with an interrupt if the ITE bit is set.

Note: If a Bus Error occurs, a Stop or a repeated Start condition should be generated by the Master to re-synchronize communication, get the transmission acknowledged and the bus released for further communication

Bit 0 = **GCAL** *General Call bit (slave mode).*

This bit is set by hardware when a general call address is detected on the bus while ENGC=1. It is cleared by hardware detecting a Stop condition (STOPF=1) or when the interface is disabled (PE=0).

0: No general call address detected on bus

1: general call address detected on bus

I²C clock control register (I2CCCR)

Reset value: 0000 0000 (00h)

7							0
FM/SM	CC6	CC5	CC4	CC3	CC2	CC1	CC0
Read / Write							

Bit 7 = **FM/SM** *Fast/Standard I²C mode bit*

This bit is set and cleared by software. It is not cleared when the interface is disabled (PE=0).

0: Standard I²C mode

1: Fast I²C mode

Bits 6:0 = **CC[6:0]** *7-bit clock divider bits*

These bits select the speed of the bus (F_{SCL}) depending on the I²C mode. They are not cleared when the interface is disabled (PE=0).

Refer to the Electrical Characteristics section for the table of values.

Note: The programmed F_{SCL} assumes no load on SCL and SDA lines.

I²C data register (I2CDR)

Reset Value: 0000 0000 (00h)

7							0
D7	D6	D5	D4	D3	D2	D1	D0
Read / Write							

Bits 7:0 = **D[7:0]** *8-bit Data register*

These bits contain the byte to be received or transmitted on the bus.

– Transmitter mode: byte transmission start automatically when the software writes in the DR register.

– Receiver mode: the first data byte is received automatically in the DR register using the least significant bit of the address. Then, the following data bytes are received one by one after reading the DR register.

Table 62. ST7 addressing mode overview (continued)

Mode			Syntax	Destination/ source	Pointer address	Pointer size	Length (bytes)
Long	Indirect	Indexed	ld A,([$10.w],X)	0000..FFFF	00..FF	word	+ 2
Relative	Direct		jrne loop	PC-128/PC+127(1)			+ 1
Relative	Indirect		jrne [$10]	PC-128/PC+127(1)	00..FF	byte	+ 2
Bit	Direct		bset $10,#7	00..FF			+ 1
Bit	Indirect		bset [$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt $10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [$10],#7,skip	00..FF	00..FF	byte	+ 3

1. At the time the instruction is executed, the Program Counter (PC) points to the instruction following JRxx.

12.1.1 Inherent mode

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Table 63. Instructions supporting inherent addressing mode

Instruction	Function
NOP	No operation
TRAP	S/W interrupt
WFI	Wait for interrupt (low power mode)
HALT	Halt oscillator (lowest power mode)
RET	Subroutine return
IRET	Interrupt subroutine return
SIM	Set interrupt mask
RIM	Reset interrupt mask
SCF	Set carry flag
RCF	Reset carry flag
RSP	Reset stack pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/decrement
TNZ	Test negative or zero
CPL, NEG	1 or 2 complement

12.2.1 Illegal opcode reset

In order to provide enhanced robustness to the device against unexpected behavior, a system of illegal opcode detection is implemented: a reset is generated if the code to be executed does not correspond to any opcode or prebyte value. This, combined with the Watchdog, allows the detection and recovery from an unexpected fault or interference.

A valid prebyte associated with a valid opcode forming an unauthorized combination does not generate a reset.

Table 68. Illegal opcode detection

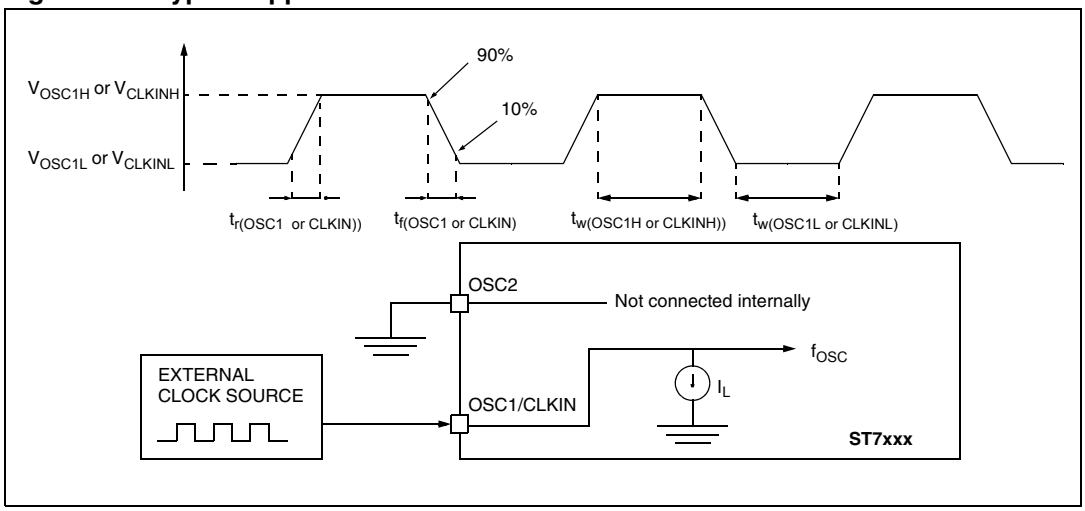
Mnemo	Description	Function/Example	Dst	Src		H	I	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M		H		N	Z	C
ADD	Addition	A = A + M	A	M		H		N	Z	C
AND	Logical And	A = A . M	A	M				N	Z	
BCP	Bit compare A, Memory	tst (A . M)	A	M				N	Z	
BRES	Bit Reset	bres Byte, #3	M							
BSET	Bit Set	bset Byte, #3	M							
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M							C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M							C
CALL	Call subroutine									
CALLR	Call subroutine relative									
CLR	Clear		reg, M					0	1	
CP	Arithmetic Compare	tst(Reg - M)	reg	M				N	Z	C
CPL	One Complement	A = FFH-A	reg, M					N	Z	1
DEC	Decrement	dec Y	reg, M					N	Z	
HALT	Halt						0			
IRET	Interrupt routine return	Pop CC, A, X, PC				H	I	N	Z	C
INC	Increment	inc X	reg, M					N	Z	
JP	Absolute Jump	jp [TBL.w]								
JRA	Jump relative always									
JRT	Jump relative									
JRF	Never jump	jrf *								
JRIH	Jump if ext. interrupt = 1									
JRIL	Jump if ext. interrupt = 0									
JRH	Jump if H = 1	H = 1 ?								
JRNH	Jump if H = 0	H = 0 ?								
JRM	Jump if I = 1	I = 1 ?								
JRNM	Jump if I = 0	I = 0 ?								
JRMI	Jump if N = 1 (minus)	N = 1 ?								

Table 84. External clock source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSC1H} or V_{CLKIN_H}	OSC1/CLKIN input pin high level voltage	see *Figure 98*	$0.7xV_{DD}$		V_{DD}	V
V_{OSC1L} or V_{CLKIN_L}	OSC1/CLKIN input pin low level voltage		V_{SS}		$0.3xV_{DD}$	
$t_{w(OSC1H)}$ or $t_{w(CLKINH)}$ $t_{w(OSC1L)}$ or $t_{w(CLKINL)}$	OSC1/CLKIN high or low time(1)		15			ns
$t_{r(OSC1)}$ or $t_{r(CLKIN)}$ $t_{f(OSC1)}$ or $t_{f(CLKIN)}$	OSC1/CLKIN rise or fall time(1)				15	
I_L	OSCx/CLKIN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 98. Typical application with an external clock source



13.6.1 Auto-wakeup from Halt oscillator (AWU)

Table 85. AWU from Halt characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{AWU}	AWU oscillator frequency		16	32	64	kHz
t_{RCSRT}	AWU oscillator startup time				50	µs

1. Guaranteed by Design. Not tested in production.

Table 95. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C	A

13.9 I/O port pin characteristics

13.9.1 General characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 96. General characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage			V_{SS} - 0.3		$0.3V_{DD}$	V
V_{IH}	Input high level voltage			$0.7V_{DD}$		V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis(1)				400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$				±1	µA
I_S	Static current consumption induced by each floating input pin(2)	Floating input mode			400		
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN}=V_{SS}$	V_{DD}= 5 V	70	100	200	kΩ
			V_{DD}= 3 V		200(1)		
C_{IO}	I/O pin capacitance				5		pF
$t_{f(IO)out}$	Output high to low level fall time(1)	C_L= 50 pF Between 10% and 90%			25		ns
$t_{r(IO)out}$	Output low to high level rise time(1)				25		
$t_{w(IT)in}$	External interrupt pulse time(4)			1			t_{CPU}

1. Data based on validation/design results.
2. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 100*). Static peak current value taken at a fixed V_{IN} value, based on design simulation and technology characteristics, not tested in production. This value depends on V_{DD} and temperature values.
3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.
4. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 100. Two typical applications with unused I/O pin

1. During normal operation the ICCCLK pin must be pulled-up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset.
2. I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

Figure 101. R_{pu} resistance versus voltage at four different temperatures

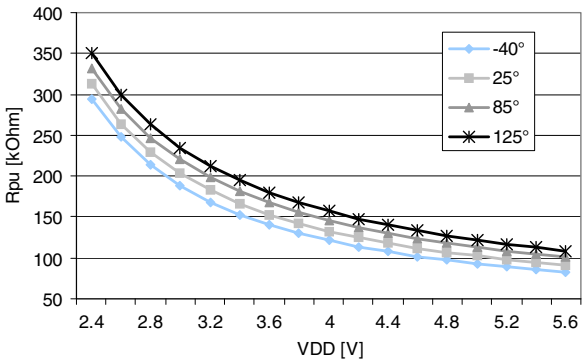


Figure 102. I_{pu} current versus voltage at four different temperatures

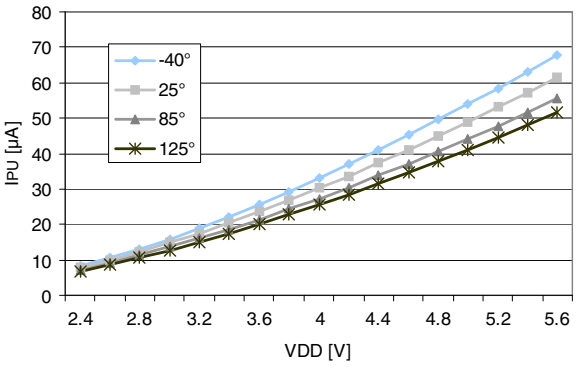
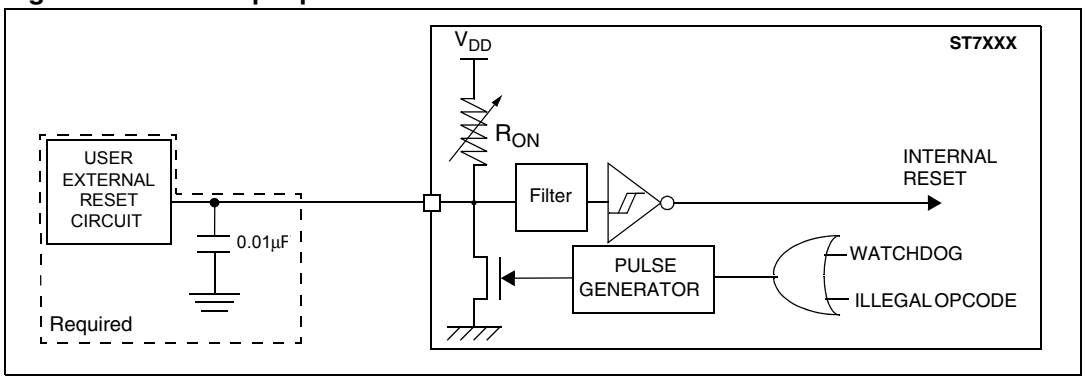


Figure 123. $\overline{\text{RESET}}$ pin protection when LVD is disabled



1. The reset network protects the device against parasitic resets.
The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in *Section 13.10.1 on page 224*. Otherwise the reset will not be taken into account internally.
Because the reset circuit is designed to allow the internal Reset to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in *Section Table 70. on page 194*.
2. Please refer to *Section 12.2.1 on page 189* for more details on illegal opcode reset conditions.

13.11 10-bit ADC characteristics

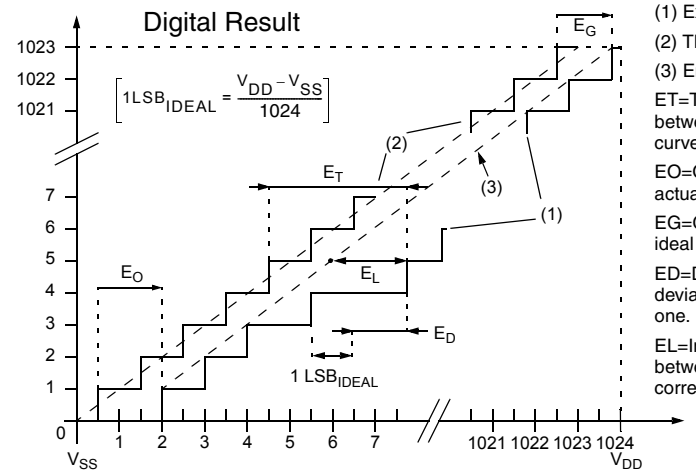
Subject to general operating condition for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 99. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency(2)				4	MHz
V_{AIN}	Conversion voltage range		V_{SSA}		V_{DDA}	V
R_{AIN}	External input resistor	V_{DD} = 5 V, f_{ADC} = 4 MHz			8k(3)	Ω
		V_{DD} = 3.3 V, f_{ADC} = 4 MHz			7k(3)	
		2.7 V ≤V_{DD} ≤5.5 V, f_{ADC} = 2 MHz			10k(3)	
		2.4 V ≤V_{DD} ≤2.7 V, f_{ADC} = 1 MHz			20k(3)	
C_{ADC}	Internal sample and hold capacitor			6		pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU} = 8 MHz, f_{ADC} = 4 MHz		0(4)		µs
t_{ADC}	Conversion time (Sample+Hold)			3.5		
	- Sample capacitor loading time - Hold conversion time			4 10		$1/f_{ADC}$

1. Unless otherwise specified, typical data are based on T_A = 25 °C and V_{DD}-V_{SS} = 5 V. They are given only as design guidelines and are not tested.
2. The maximum ADC clock frequency allowed within V_{DD} = 2.4 V to 2.7 V operating range is 1 MHz.
3. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than the maximum value). Data guaranteed by Design, not tested in production.
4. The stabilization time of the A/D converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.

Figure 125. ADC accuracy characteristics



(1) Example of an actual transfer curve

(2) The ideal transfer curve

(3) End point correlation line

ET=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.

EO=Offset Error: deviation between the first actual transition and the first ideal one.

EG=Gain Error: deviation between the last ideal transition and the last actual one.

ED=Differential Linearity Error: maximum deviation between actual steps and the ideal one.

EL=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Table 103. Amplifier characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(AMP)}$	Amplifier operating voltage		3.6		5.5	V
V_{IN}	Amplifier input voltage(1)	V_{DD} = 3.6 V	0		350	mV
		V_{DD} = 5 V	0		500	
V_{OFFSET} (2)	Amplifier output offset voltage(3)	V_{DD}= 5 V		200		mV
V_{STEP} (2)	Step size for monotonicity(4)	V_{DD} = 3.6 V	3.5			mV
		V_{DD} = 5 V	4.89			
Linearity (2)	Output voltage response		linear			
Gain factor (2)	Amplified analog input gain(5)			8		
Vmax (2)	Output linearity max voltage	V_{INmax} = 430 mV, V_{DD} = 5 V		3.65		V
Vmin (2)	Output linearity min voltage			200		mV

1. Please refer to the Application Note AN1830 for details of TE% vs Vin.
2. Data based on characterization results over the whole temperature range, not tested in production.
3. Refer to the offset variation in temperature below
4. Monotonicity guaranteed if V_{IN} increases or decreases in steps of min. 5mV.
5. For precise conversion results it is recommended to calibrate the amplifier at the following two points: offset at V_{INmin} = 0V ; gain at full scale (for example V_{IN} = 430 mV)

14 Device configuration and ordering information

This device is available for production in user programmable version (Flash).

ST7LITE49K2 XFlash devices are shipped to customers with a default program memory content (FFh).

14.1 Option bytes

The two option bytes allow the hardware configuration of the microcontroller to be selected. The option bytes can be accessed only in programming mode (for example using a standard ST7 programming tool).

14.1.1 Option byte 1

Bits 7:6 = **CKSEL[1:0]** *Start-up clock selection.*

These bits are used to select the startup frequency. By default, the internal RC is selected.

Table 106. Startup clock selection

Configuration	CKSEL1	CKSEL0
Internal RC as startup clock	0	0
AWU RC as a startup clock	0	1
External crystal/ceramic resonator	1	0
External clock	1	1

Bit 5 = Reserved, must always be 1.

Bit 4 = **PLL32OFF** *32 MHz PLL disabled.*

0: PLL32 enabled
1: PLL32 disabled (by-passed). By default the PLL32 is disabled.

Bits 3:2 = **LVD[1:0]** *Low voltage detection selection.*

These option bits enable the low voltage detection block (LVD) with a selected threshold as shown in *Table 107*.

Table 107. LVD threshold configuration

Configuration	VD1	VD0
LVD Off (default value)	1	1
Highest voltage threshold	1	0
Medium voltage threshold	0	1
Lowest voltage threshold	0	0