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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f4550t-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic18f4550t-i-ml</a>

# PIC18F2455/2550/4455/4550

**TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
RA0/AN0	2	I/O I	TTL Analog	PORTA is a bidirectional I/O port.
RA0				Digital I/O.
AN0				Analog input 0.
RA1/AN1	3	I/O I	TTL Analog	Digital I/O.
RA1				Analog input 1.
AN1				
RA2/AN2/VREF-/CVREF	4	I/O I I O	TTL Analog Analog Analog	Digital I/O.
RA2				Analog input 2.
AN2				A/D reference voltage (low) input.
VREF-				Analog comparator reference output.
CVREF				
RA3/AN3/VREF+	5	I/O I I	TTL Analog Analog	Digital I/O.
RA3				Analog input 3.
AN3				A/D reference voltage (high) input.
VREF+				
RA4/T0CKI/C1OUT/RCV	6	I/O I O I	ST ST — TTL	Digital I/O.
RA4				Timer0 external clock input.
T0CKI				Comparator 1 output.
C1OUT				External USB transceiver RCV input.
RCV				
RA5/AN4/SS/ HLVDIN/C2OUT	7	I/O I I I O	TTL Analog TTL Analog —	Digital I/O.
RA5				Analog input 4.
AN4				SPI slave select input.
SS				High/Low-Voltage Detect input.
HLVDIN				Comparator 2 output.
C2OUT				
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power

**Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.  
**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.

## 4.2 Master Clear Reset ( $\overline{\text{MCLR}}$ )

The  $\overline{\text{MCLR}}$  pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the  $\overline{\text{MCLR}}$  Reset path which detects and ignores small pulses.

The  $\overline{\text{MCLR}}$  pin is not driven low by any internal Resets, including the WDT.

In PIC18F2455/2550/4455/4550 devices, the  $\overline{\text{MCLR}}$  input can be disabled with the MCLRE Configuration bit. When  $\overline{\text{MCLR}}$  is disabled, the pin becomes a digital input. See **Section 10.5 “PORTE, TRISE and LATE Registers”** for more information.

## 4.3 Power-on Reset (POR)

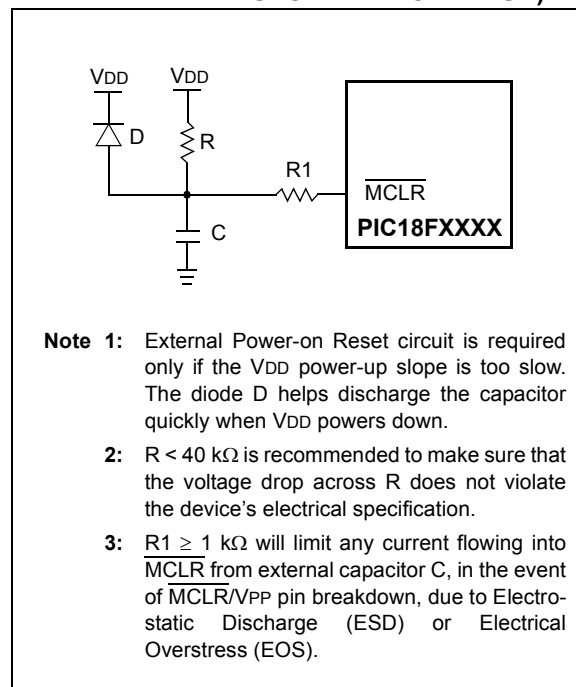
A Power-on Reset pulse is generated on-chip whenever  $V_{DD}$  rises above a certain threshold. This allows the device to start in the initialized state when  $V_{DD}$  is adequate for operation.

To take advantage of the POR circuitry, tie the  $\overline{\text{MCLR}}$  pin through a resistor ( $1\text{ k}\Omega$  to  $10\text{ k}\Omega$ ) to  $V_{DD}$ . This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for  $V_{DD}$  is specified (parameter D004, **Section 28.1 “DC Characteristics”**). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the  $\overline{\text{POR}}$  bit (RCON<1>). The state of the bit is set to ‘0’ whenever a POR occurs; it does not change for any other Reset event.  $\overline{\text{POR}}$  is not reset to ‘1’ by any hardware event. To capture multiple events, the user manually resets the bit to ‘1’ in software following any POR.

**FIGURE 4-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW  $V_{DD}$  POWER-UP)**



# PIC18F2455/2550/4455/4550

**TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)**

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
INDF2	2455	2550	4455	4550	N/A	N/A	N/A
POSTINC2	2455	2550	4455	4550	N/A	N/A	N/A
POSTDEC2	2455	2550	4455	4550	N/A	N/A	N/A
PREINC2	2455	2550	4455	4550	N/A	N/A	N/A
PLUSW2	2455	2550	4455	4550	N/A	N/A	N/A
FSR2H	2455	2550	4455	4550	---- 0000	---- 0000	---- uuuu
FSR2L	2455	2550	4455	4550	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	2455	2550	4455	4550	---x xxxx	---u uuuu	---u uuuu
TMR0H	2455	2550	4455	4550	0000 0000	0000 0000	uuuu uuuu
TMR0L	2455	2550	4455	4550	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	2455	2550	4455	4550	1111 1111	1111 1111	uuuu uuuu
OSCCON	2455	2550	4455	4550	0100 q000	0100 00q0	uuuu uuqu
HLVDCON	2455	2550	4455	4550	0-00 0101	0-00 0101	u-uu uuuu
WDTCON	2455	2550	4455	4550	---- --0	---- --0	---- --u
RCON <sup>(4)</sup>	2455	2550	4455	4550	0q-1 11q0	0q-q qquu	uq-u qquu
TMR1H	2455	2550	4455	4550	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	2455	2550	4455	4550	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	2455	2550	4455	4550	0000 0000	u0uu uuuu	uuuu uuuu
TMR2	2455	2550	4455	4550	0000 0000	0000 0000	uuuu uuuu
PR2	2455	2550	4455	4550	1111 1111	1111 1111	1111 1111
T2CON	2455	2550	4455	4550	-000 0000	-000 0000	-uuu uuuu
SSPBUF	2455	2550	4455	4550	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPADD	2455	2550	4455	4550	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	2455	2550	4455	4550	0000 0000	0000 0000	uuuu uuuu
SSPCON1	2455	2550	4455	4550	0000 0000	0000 0000	uuuu uuuu
SSPCON2	2455	2550	4455	4550	0000 0000	0000 0000	uuuu uuuu
ADRESH	2455	2550	4455	4550	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADRESL	2455	2550	4455	4550	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	2455	2550	4455	4550	--00 0000	--00 0000	--uu uuuu
ADCON1	2455	2550	4455	4550	--00 0qqq	--00 0qqq	--uu uuuu
ADCON2	2455	2550	4455	4550	0-00 0000	0-00 0000	u-uu uuuu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.  
Shaded cells indicate conditions do not apply for the designated device.

**Note 1:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

**2:** One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

**4:** See Table 4-3 for Reset value for specific condition.

**5:** PORTA<6>, LATA<6> and TRISA<6> are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

# PIC18F2455/2550/4455/4550

## 5.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see **Section 5.1.4.1 “Computed GOTO”**).

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of ‘0’. The PC increments by 2 to address sequential instructions in the program memory.

The **CALL**, **RCALL** and **GOTO** program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

## 5.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a **CALL** or **RCALL** instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a **RETURN**, **RETLW** or a **RETFIE** instruction. PCLATU and PCLATH are not affected by any of the **RETURN** or **CALL** instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack Special Function Registers. Data can also be pushed to, or popped from the stack, using these registers.

A **CALL** type instruction causes a push onto the stack. The Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the **CALL**). A **RETURN** type instruction causes a pop from the stack. The contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

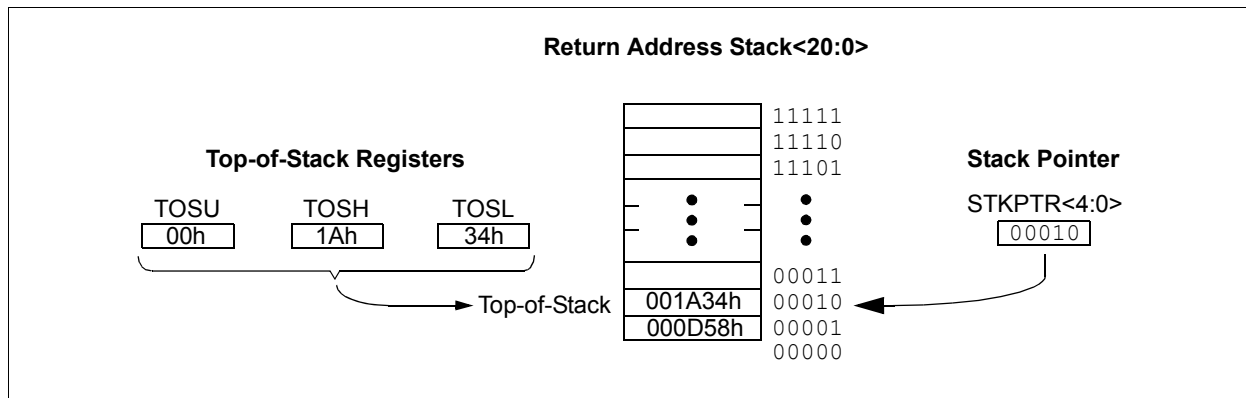
The Stack Pointer is initialized to ‘00000’ after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of ‘00000’; this is only a Reset value. Status bits indicate if the stack is full, has overflowed or has underflowed.

### 5.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 5-2). This allows users to implement a software stack if necessary. After a **CALL**, **RCALL** or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user-defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the global interrupt enable bits while accessing the stack to prevent inadvertent stack corruption.

**FIGURE 5-2: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS**



## 11.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not directly readable or writable; its value is set by the PSA and T0PS2:T0PS0 bits (T0CON<3:0>) which determine the prescaler assignment and prescale ratio.

Clearing the PSA bit assigns the prescaler to the Timer0 module. When it is assigned, prescale values from 1:2 through 1:256, in power-of-2 increments, are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF TMR0`, `MOVWF TMR0`, `BSF TMR0`, etc.) clear the prescaler count.

**Note:** Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count but will not change the prescaler assignment.

### 11.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control and can be changed “on-the-fly” during program execution.

## 11.4 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or from FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF flag bit. The interrupt can be masked by clearing the TMR0IE bit (INTCON<5>). Before re-enabling the interrupt, the TMR0IF bit must be cleared in software by the Interrupt Service Routine.

Since Timer0 is shut down in Sleep mode, the TMR0 interrupt cannot awaken the processor from Sleep.

**TABLE 11-1: REGISTERS ASSOCIATED WITH TIMER0**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
TMR0L	Timer0 Register Low Byte								54
TMR0H	Timer0 Register High Byte								54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	53
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	53
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0	54
TRISA	—	TRISA6 <sup>(1)</sup>	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	56

**Legend:** — = unimplemented locations, read as ‘0’. Shaded cells are not used by Timer0.

**Note 1:** RA6 is configured as a port pin based on various primary oscillator modes. When the port pin is disabled, all of the associated bits read ‘0’.

## 16.4 Enhanced PWM Mode

The Enhanced PWM mode provides additional PWM output options for a broader range of control applications. The module is a backward compatible version of the standard CCP module and offers up to four outputs, designated P1A through P1D. Users are also able to select the polarity of the signal (either active-high or active-low). The module's output mode and polarity are configured by setting the P1M1:P1M0 and CCP1M3:CCP1M0 bits of the CCP1CON register.

Figure 16-1 shows a simplified block diagram of PWM operation. All control registers are double-buffered and are loaded at the beginning of a new PWM cycle (the period boundary when Timer2 resets) in order to prevent glitches on any of the outputs. The exception is the PWM Dead-Band Delay register, ECCP1DEL, which is loaded at either the duty cycle boundary or the boundary period (whichever comes first). Because of the buffering, the module waits until the assigned timer resets instead of starting immediately. This means that Enhanced PWM waveforms do not exactly match the standard PWM waveforms, but are instead offset by one full instruction cycle (4 TOSC).

As before, the user must manually configure the appropriate TRIS bits for output.

### 16.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following equation:

#### EQUATION 16-1:

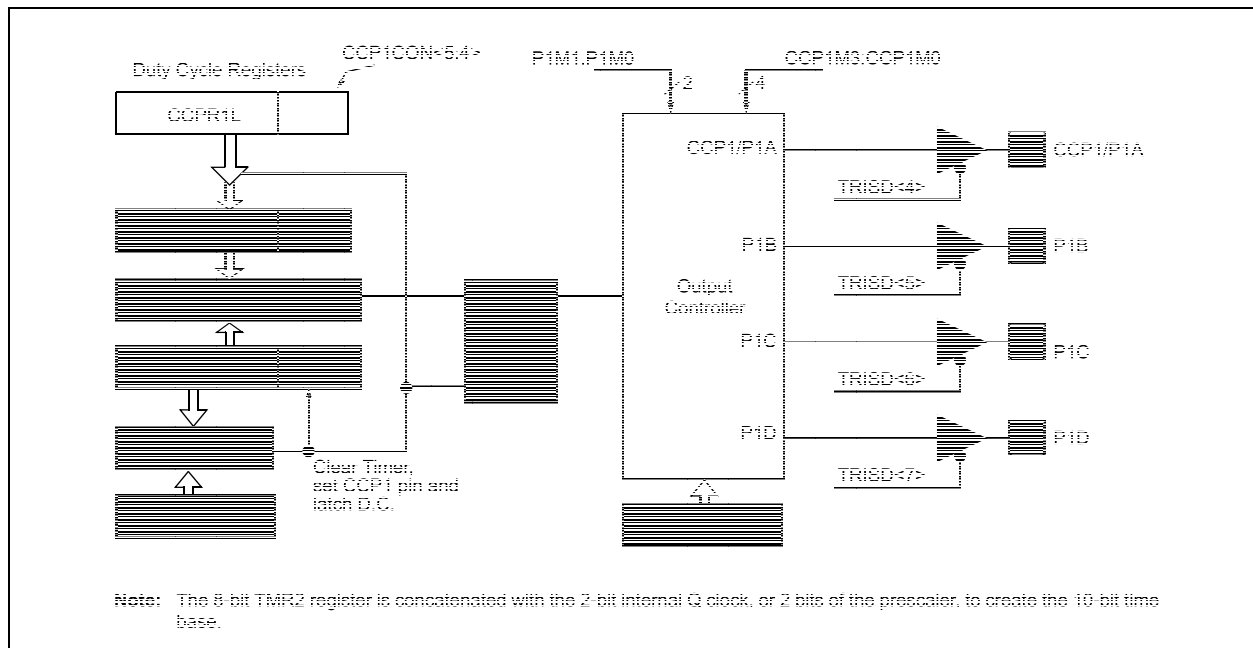
$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

PWM frequency is defined as  $1/[\text{PWM period}]$ . When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is copied from CCPR1L into CCPR1H

**Note:** The Timer2 postscaler (see **Section 13.0 “Timer2 Module”**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

**FIGURE 16-1: SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODULE**



# PIC18F2455/2550/4455/4550

## 17.4.1.3 BDnSTAT Register (SIE Mode)

When the BD and its buffer are owned by the SIE, most of the bits in BDnSTAT take on a different meaning. The configuration is shown in Register 17-6. Once UOWN is set, any data or control settings previously written there by the user will be overwritten with data from the SIE.

The BDnSTAT register is updated by the SIE with the token Packet Identifier (PID) which is stored in BDnSTAT<5:3>. The transfer count in the corresponding BDnCNT register is updated. Values that overflow the 8-bit register carry over to the two most significant digits of the count, stored in BDnSTAT<1:0>.

## 17.4.2 BD BYTE COUNT

The byte count represents the total number of bytes that will be transmitted during an IN transfer. After an IN transfer, the SIE will return the number of bytes sent to the host.

For an OUT transfer, the byte count represents the maximum number of bytes that can be received and stored in USB RAM. After an OUT transfer, the SIE will return the actual number of bytes received. If the number of bytes received exceeds the corresponding byte count, the data packet will be rejected and a NAK handshake will be generated. When this happens, the byte count will not be updated.

The 10-bit byte count is distributed over two registers. The lower 8 bits of the count reside in the BDnCNT register. The upper two bits reside in BDnSTAT<1:0>. This represents a valid byte range of 0 to 1023.

## 17.4.3 BD ADDRESS VALIDATION

The BD Address register pair contains the starting RAM address location for the corresponding endpoint buffer. For an endpoint starting location to be valid, it must fall in the range of the USB RAM, 400h to 7FFh. No mechanism is available in hardware to validate the BD address.

If the value of the BD address does not point to an address in the USB RAM, or if it points to an address within another endpoint's buffer, data is likely to be lost or overwritten. Similarly, overlapping a receive buffer (OUT endpoint) with a BD location in use can yield unexpected results. When developing USB applications, the user may want to consider the inclusion of software-based address validation in their code.

**REGISTER 17-6: BDnSTAT: BUFFER DESCRIPTOR n STATUS REGISTER (BD0STAT THROUGH BD63STAT), SIE MODE (DATA RETURNED BY THE SIE TO THE MICROCONTROLLER)**

R/W-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
UOWN	—	PID3	PID2	PID1	PID0	BC9	BC8	
bit 7								bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **UOWN:** USB Own bit

1 = The SIE owns the BD and its corresponding buffer

bit 6 **Reserved:** Not written by the SIE

bit 5-2 **PID3:PID0:** Packet Identifier bits

The received token PID value of the last transfer (IN, OUT or SETUP transactions only).

bit 1-0 **BC9:BC8:** Byte Count 9 and 8 bits

These bits are updated by the SIE to reflect the actual number of bytes received on an OUT transfer and the actual number of bytes transmitted on an IN transfer.

# PIC18F2455/2550/4455/4550

## 19.3.2 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON1<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

The MSSP module consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready. Once the eight bits of data have been received, that byte is moved to the SSPBUF register. Then, the Buffer Full detect bit, BF (SSPSTAT<0>) and the interrupt flag bit, SSPIF, are set. This double-buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored and the Write Collision detect bit, WCOL (SSPCON1<7>), will be set. User software must clear

the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

**Note:** When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Application software should follow this process even when the current contents of SSPBUF are not important.

The Buffer Full bit, BF (SSPSTAT<0>), indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 19-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPBUF register. Additionally, the MSSP Status register (SSPSTAT) indicates the various status conditions.

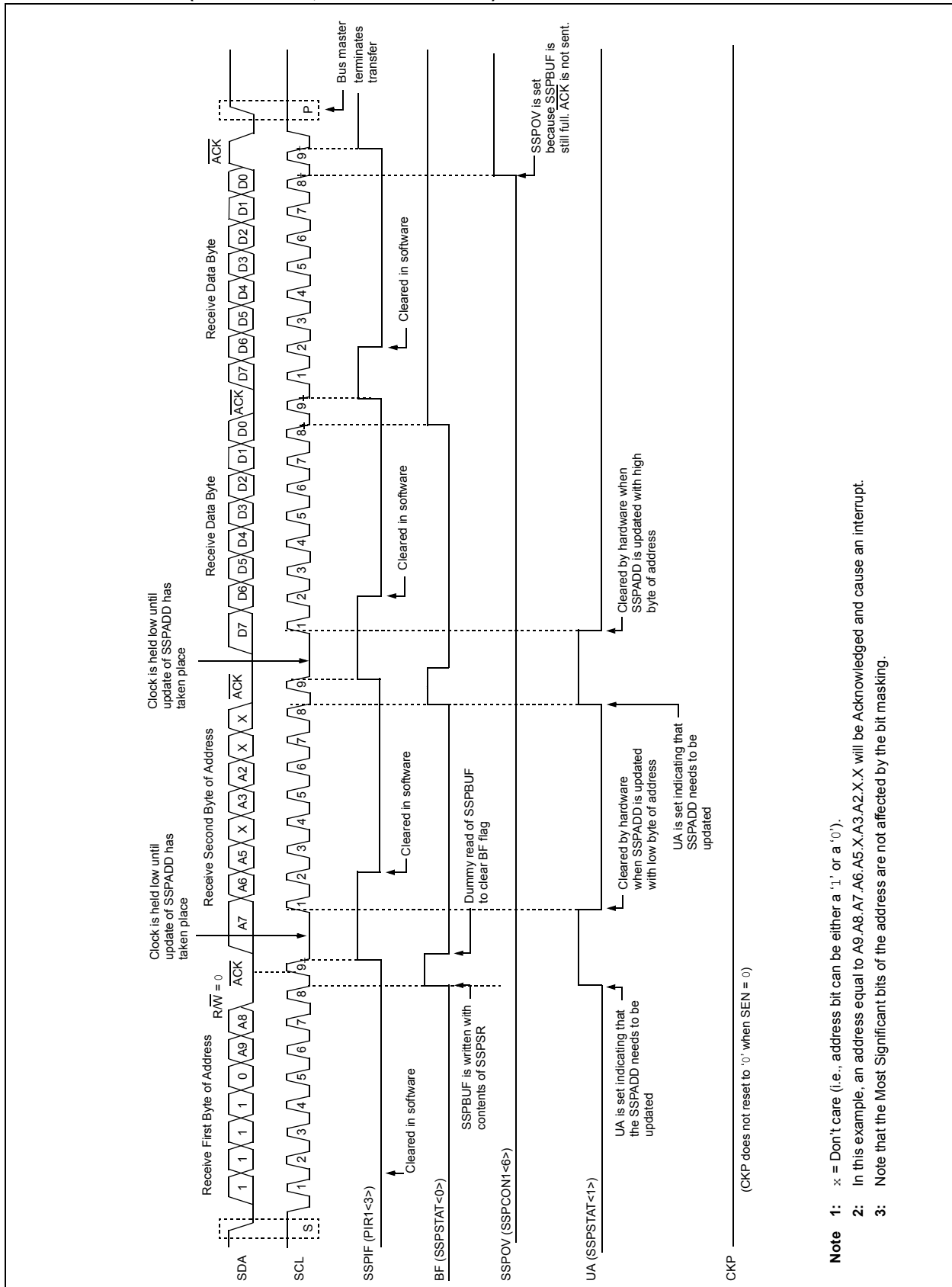
**Note:** The SSPBUF register cannot be used with read-modify-write instructions, such as BCF, BTFSC and COMF.

### EXAMPLE 19-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
TransmitSPI:
BCF      PIR1, SSPIF      ;Make sure interrupt flag is clear (may have been set from previous
                           transmission).
MOVWF    SSPBUF, W        ;Perform read, even if the data in SSPBUF is not important
MOVWF    RXDATA           ;Save previously received byte in user RAM, if the data is meaningful
MOVWF    TXDATA, W        ;WREG = Contents of TXDATA (user data to send)
MOVWF    SSPBUF           ;Load data to send into transmit buffer

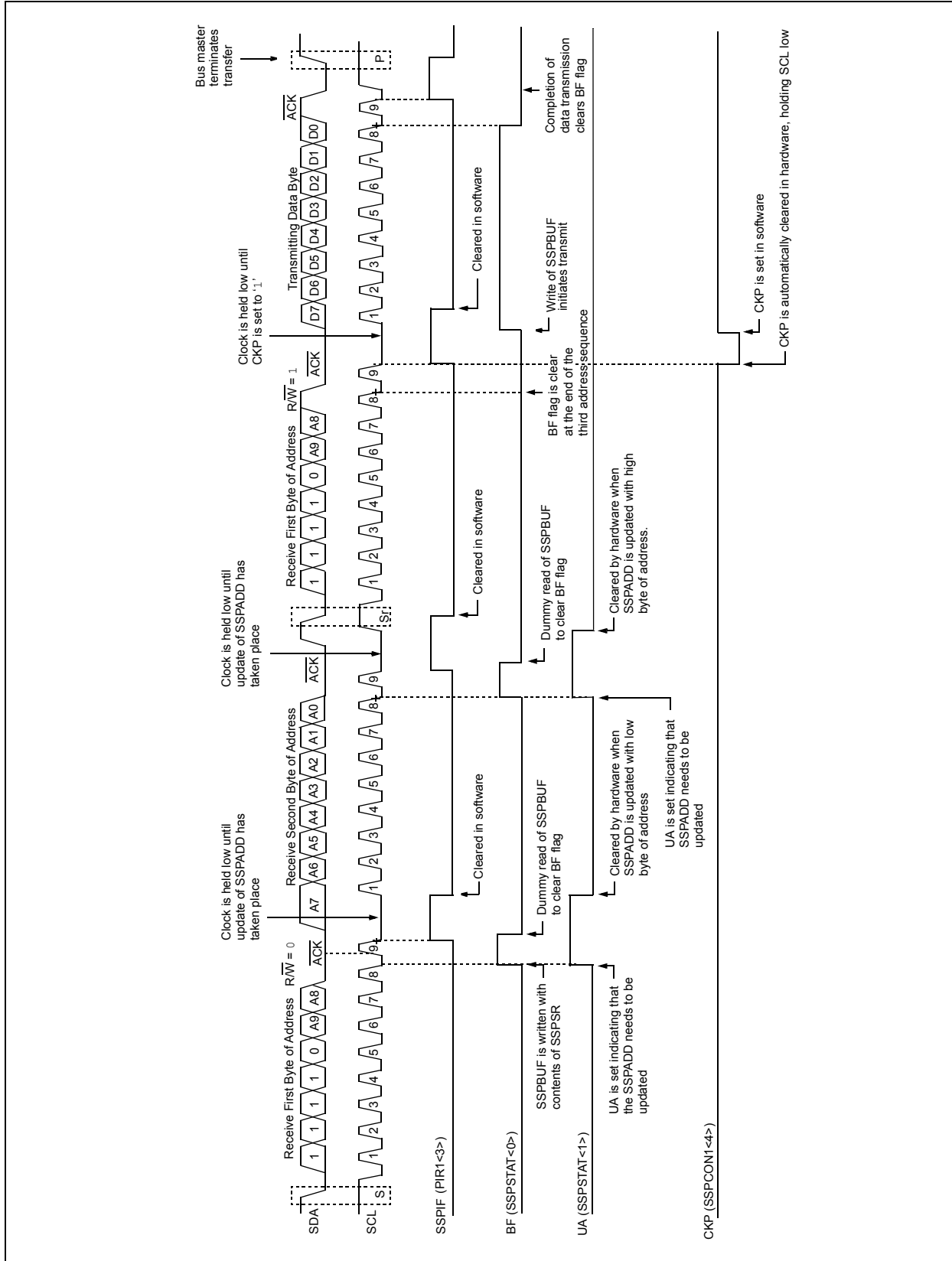
WaitComplete:
BTFSS    PIR1, SSPIF      ;Interrupt flag set when transmit is complete
BRA      WaitComplete
```

**FIGURE 19-12: I<sup>2</sup>C™ SLAVE MODE TIMING WITH SEN = 0 AND ADMSK<5:1> = 01001 (RECEPTION, 10-BIT ADDRESS)**



# PIC18F2455/2550/4455/4550

FIGURE 19-13: I<sup>2</sup>C™ SLAVE MODE TIMING (TRANSMISSION, 10-BIT ADDRESS)



# PIC18F2455/2550/4455/4550

## 19.4.10 I<sup>2</sup>C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address, or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time specification parameter 106). SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high (see data setup time specification parameter 107). When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKDT bit on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 19-23).

After the write to the SSPBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will deassert the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

### 19.4.10.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all eight bits are shifted out.

### 19.4.10.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur) after 2 Tcy after the SSPBUF write. If SSPBUF is rewritten within 2 Tcy, the WCOL bit is set and SSPBUF is updated. This may result in a corrupted transfer.

The user should verify that the WCOL is clear after each write to SSPBUF to ensure the transfer is correct. In all cases, WCOL must be cleared in software.

### 19.4.10.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge (ACK = 0) and is set when the slave does not Acknowledge (ACK = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

## 19.4.11 I<sup>2</sup>C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN (SSPCON2<3>).

**Note:** The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable bit, ACKEN (SSPCON2<4>).

### 19.4.11.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

### 19.4.11.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

### 19.4.11.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).

## 20.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is one of the two serial I/O modules. (Generically, the USART is also known as a Serial Communications Interface or SCI.) The EUSART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers. It can also be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc.

The Enhanced USART module implements additional features, including automatic baud rate detection and calibration, automatic wake-up on Sync Break reception and 12-bit Break character transmit. These make it ideally suited for use in Local Interconnect Network bus (LIN bus) systems.

The EUSART can be configured in the following modes:

- Asynchronous (full-duplex) with:
  - Auto-wake-up on Break signal
  - Auto-baud calibration
  - 12-bit Break character transmission
- Synchronous – Master (half-duplex) with selectable clock polarity
- Synchronous – Slave (half-duplex) with selectable clock polarity

The pins of the Enhanced USART are multiplexed with PORTC. In order to configure RC6/TX/CK and RC7/RX/DT/SDO as an EUSART:

- SPEN bit (RCSTA<7>) must be set (= 1)
- TRISC<7> bit must be set (= 1)
- TRISC<6> bit must be set (= 1)

<b>Note:</b> The EUSART control will automatically reconfigure the pin from input to output as needed.
--

The operation of the Enhanced USART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These are detailed on the following pages in Register 20-1, Register 20-2 and Register 20-3, respectively.

## 20.2.5 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. The Break character transmit consists of a Start bit, followed by twelve '0' bits and a Stop bit. The Frame Break character is sent whenever the SENDB and TXEN bits (TXSTA<3> and TXSTA<5>) are set while the Transmit Shift Register is loaded with data. Note that the value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

Note that the data value written to the TXREG for the Break character is ignored. The write simply serves the purpose of initiating the proper sequence.

The TRMT bit indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 20-10 for the timing of the Break character sequence.

### 20.2.5.1 Break and Sync Transmit Sequence

The following sequence will send a message frame header made up of a Break, followed by an Auto-Baud Sync byte. This sequence is typical of a LIN bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to set up the Break character.
3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
4. Write '55h' to TXREG to load the Sync character into the transmit FIFO buffer.
5. After the Break has been sent, the SENDB bit is reset by hardware. The Sync character now transmits in the preconfigured mode.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

## 20.2.6 RECEIVING A BREAK CHARACTER

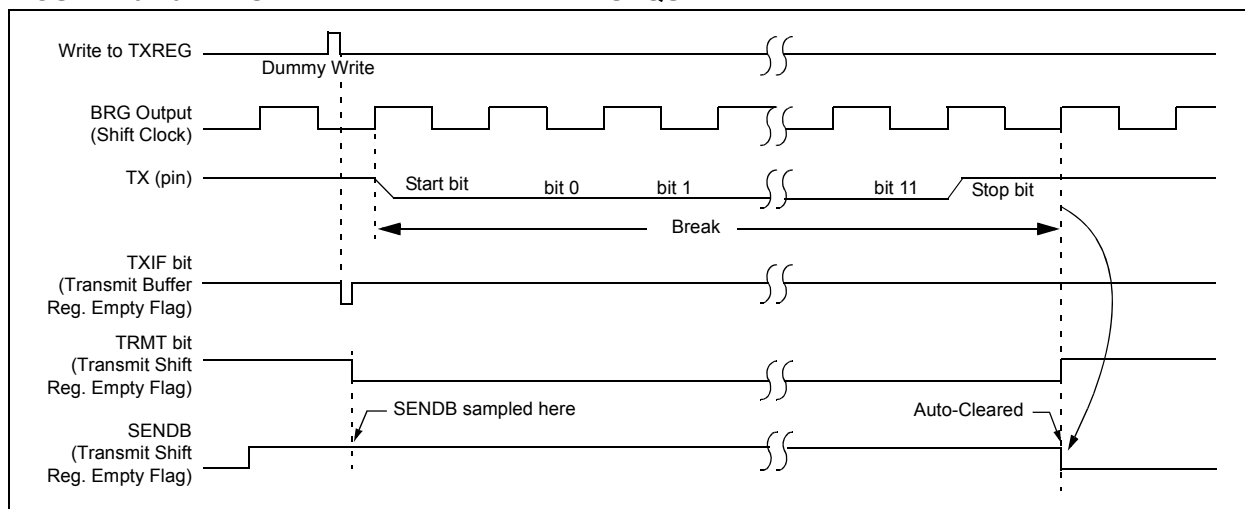
The Enhanced USART module can receive a Break character in two ways.

The first method forces configuration of the baud rate at a frequency of 9/13 the typical speed. This allows for the Stop bit transition to be at the correct sampling location (13 bits for Break versus Start bit and 8 data bits for typical data).

The second method uses the auto-wake-up feature described in **Section 20.2.4 "Auto-Wake-up on Sync Break Character"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Rate Detect feature. For both methods, the user can set the ABD bit once the TXIF interrupt is observed.

**FIGURE 20-10: SEND BREAK CHARACTER SEQUENCE**



# PIC18F2455/2550/4455/4550

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NOTES:

# PIC18F2455/2550/4455/4550

## BZ Branch if Zero

**Syntax:** BZ n

**Operands:**  $-128 \leq n \leq 127$

**Operation:** if Zero bit is '1',  
 $(PC) + 2 + 2n \rightarrow PC$

**Status Affected:** None

**Encoding:**

1110	0000	nnnn	nnnn
------	------	------	------

**Description:** If the Zero bit is '1', then the program will branch.  
 The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be  $PC + 2 + 2n$ . This instruction is then a two-cycle instruction.

**Words:** 1

**Cycles:** 1(2)

**Q Cycle Activity:**

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

**Example:** HERE BZ Jump

Before Instruction

PC = address (HERE)

After Instruction

If Zero PC = 1;  
 = address (Jump)

If Zero PC = 0;  
 = address (HERE + 2)

## CALL Subroutine Call

**Syntax:** CALL k {,s}

**Operands:**  $0 \leq k \leq 1048575$   
 $s \in [0,1]$

**Operation:**  $(PC) + 4 \rightarrow TOS$ ,  
 $k \rightarrow PC<20:1>$ ;  
 if  $s = 1$ ,  
 $(W) \rightarrow WS$ ,  
 $(STATUS) \rightarrow STATUSS$ ,  
 $(BSR) \rightarrow BSRS$

**Status Affected:** None

**Encoding:**  
 1st word ( $k<7:0>$ )  
 2nd word ( $k<19:8>$ )

1110	110s	$k_7kkk$	$kkkk_0$
1111	$k_{19}kkk$	$kkkk$	$kkkk_8$

**Description:** Subroutine call of entire 2-Mbyte memory range. First, return address ( $PC + 4$ ) is pushed onto the return stack. If 's' = 1, the W, STATUS and BSR registers are also pushed into their respective shadow registers, WS, STATUSS and BSRS. If 's' = 0, no update occurs (default). Then, the 20-bit value 'k' is loaded into  $PC<20:1>$ . CALL is a two-cycle instruction.

**Words:** 2

**Cycles:** 2

**Q Cycle Activity:**

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>, Push PC to stack	Push PC to stack	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

**Example:** HERE CALL THERE,1

Before Instruction

PC = address (HERE)

After Instruction

PC = address (THERE)  
 TOS = address (HERE + 4)  
 WS = W  
 BSRS = BSR  
 STATUSS = STATUS

# PIC18F2455/2550/4455/4550

## LFSR Load FSR

Syntax: LFSR f, k

Operands:  $0 \leq f \leq 2$   
 $0 \leq k \leq 4095$

Operation:  $k \rightarrow \text{FSRf}$

Status Affected: None

Encoding:

1110	1110	00ff	$k_{11}kkk$
1111	0000	$k_7kkk$	$kkkk$

Description: The 12-bit literal 'k' is loaded into the File Select Register pointed to by 'f'.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k' MSB	Process Data	Write literal 'k' MSB to FSRfH
Decode	Read literal 'k' LSB	Process Data	Write literal 'k' to FSRfL

**Example:** LFSR 2, 3ABh

After Instruction

FSR2H = 03h  
 FSR2L = ABh

## MOVF Move f

Syntax: MOVF f {,d {,a}}

Operands:  $0 \leq f \leq 255$   
 $d \in [0,1]$   
 $a \in [0,1]$

Operation:  $f \rightarrow \text{dest}$

Status Affected: N, Z

Encoding:

0101	00da	ffff	ffff
------	------	------	------

Description: The contents of register 'f' are moved to a destination dependent upon the status of 'd'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). Location 'f' can be anywhere in the 256-byte bank.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever  $f \leq 95$  (5Fh). See **Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write W

**Example:** MOVF REG, 0, 0

Before Instruction

REG = 22h  
 W = FFh

After Instruction

REG = 22h  
 W = 22h

# PIC18F2455/2550/4455/4550

## SLEEP Enter Sleep mode

Syntax: SLEEP

Operands: None

Operation: 00h → WDT,  
0 → WDT postscaler,  
1 →  $\overline{TO}$ ,  
0 →  $\overline{PD}$

Status Affected:  $\overline{TO}$ ,  $\overline{PD}$

Encoding: 

0000	0000	0000	0011
------	------	------	------

Description: The Power-Down status bit ( $\overline{PD}$ ) is cleared. The Time-out status bit ( $\overline{TO}$ ) is set. Watchdog Timer and its postscaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	Go to Sleep

**Example:** SLEEP

Before Instruction

$\overline{TO}$  = ?

$\overline{PD}$  = ?

After Instruction

$\overline{TO}$  = 1 †

$\overline{PD}$  = 0

† If WDT causes wake-up, this bit is cleared.

## SUBFWB Subtract f from W with Borrow

Syntax: SUBFWB f {,d {,a}}

Operands:  $0 \leq f \leq 255$   
 $d \in [0,1]$   
 $a \in [0,1]$

Operation:  $(W) - (f) - (\overline{C}) \rightarrow \text{dest}$

Status Affected: N, OV, C, DC, Z

Encoding: 

0101	01da	ffff	ffff
------	------	------	------

Description: Subtract register 'f' and Carry flag (borrow) from W (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever  $f \leq 95$  (5Fh). See **Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

**Example 1:** SUBFWB REG, 1, 0

Before Instruction

REG = 3

W = 2

C = 1

After Instruction

REG = FF

W = 2

C = 0

Z = 0

N = 1 ; result is negative

**Example 2:** SUBFWB REG, 0, 0

Before Instruction

REG = 2

W = 5

C = 1

After Instruction

REG = 2

W = 3

C = 1

Z = 0

N = 0 ; result is positive

**Example 3:** SUBFWB REG, 1, 0

Before Instruction

REG = 1

W = 2

C = 0

After Instruction

REG = 0

W = 2

C = 1

Z = 1 ; result is zero

N = 0

# PIC18F2455/2550/4455/4550

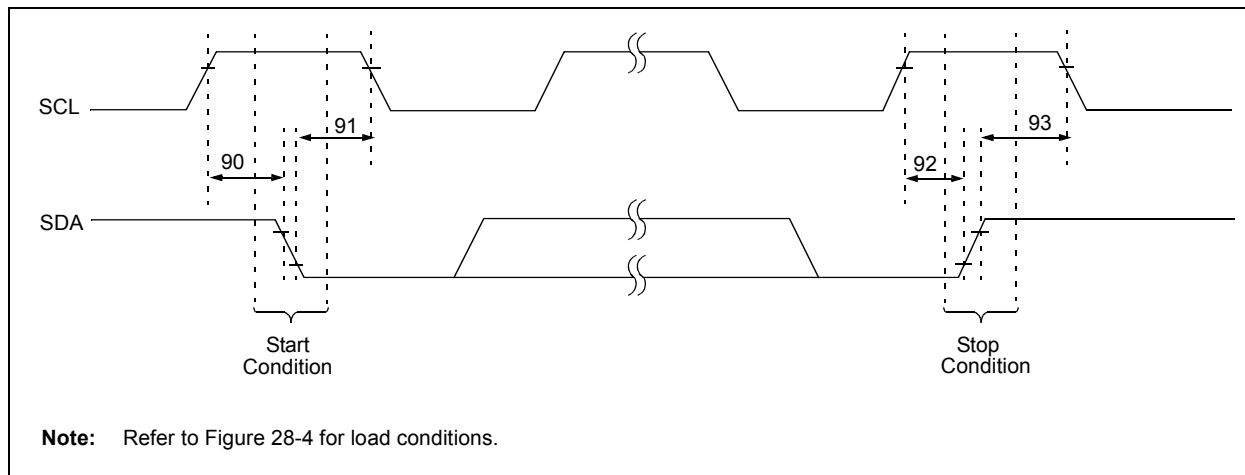
## 28.2 DC Characteristics: Power-Down and Supply Current PIC18F2455/2550/4455/4550 (Industrial) PIC18LF2455/2550/4455/4550 (Industrial) (Continued)

PIC18LF2455/2550/4455/4550 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature      -40°C ≤ TA ≤ +85°C for industrial						
PIC18F2455/2550/4455/4550 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature      -40°C ≤ TA ≤ +85°C for industrial						
Param No.	Symbol	Device	Typ	Max	Units	Conditions			
		Supply Current (IDD) <sup>(2)</sup>							
		PIC18LFX455/X550	65	130	μA	-40°C	VDD = 2.0V	FOSC = 1 MHz ( <b>PRI_IDLE</b> mode, EC oscillator)	
			65	120	μA	+25°C			
			70	115	μA	+85°C			
		PIC18LFX455/X550	120	270	μA	-40°C	VDD = 3.0V		
			120	250	μA	+25°C			
			130	240	μA	+85°C			
		All devices	230	480	μA	-40°C	VDD = 5.0V		
			240	450	μA	+25°C			
			250	430	μA	+85°C			
		PIC18LFX455/X550	255	475	μA	-40°C	VDD = 2.0V	FOSC = 4 MHz ( <b>PRI_IDLE</b> mode, EC oscillator)	
			260	450	μA	+25°C			
			270	430	μA	+85°C			
		PIC18LFX455/X550	420	900	μA	-40°C	VDD = 3.0V		
			430	850	μA	+25°C			
			450	810	μA	+85°C			
		All devices	0.9	1.5	mA	-40°C	VDD = 5.0V		
			0.9	1.4	mA	+25°C			
			0.9	1.3	mA	+85°C			
		All devices	6.0	16	mA	-40°C	VDD = 4.2V	FOSC = 40 MHz ( <b>PRI_IDLE</b> mode, EC oscillator)	
			6.2	16	mA	+25°C			
			6.6	16	mA	+85°C			
		All devices	8.1	18	mA	-40°C	VDD = 5.0V		
			8.3	18	mA	+25°C			
			9.0	18	mA	+85°C			
		All devices	8.0	18	mA	-40°C	VDD = 4.2V		FOSC = 48 MHz ( <b>PRI_IDLE</b> mode, EC oscillator)
			8.1	18	mA	+25°C			
			8.2	18	mA	+85°C			
		All devices	9.8	21	mA	-40°C	VDD = 5.0V		
			10.0	21	mA	+25°C			
			10.5	21	mA	+85°C			

**Legend:** Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to  $V_{DD}$  or  $V_{SS}$  and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.  
The test conditions for all  $I_{DD}$  measurements in active operation mode are:  
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to  $V_{DD}$  or  $V_{SS}$ ;  
MCLR =  $V_{DD}$ ; WDT enabled/disabled as specified.
- 3:** Standard low-cost 32 kHz crystals have an operating temperature range of  $-10^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ . Extended temperature crystals are available at a much higher cost.
- 4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

**FIGURE 28-17: MASTER SSP I<sup>2</sup>C™ BUS START/STOP BITS TIMING WAVEFORMS**

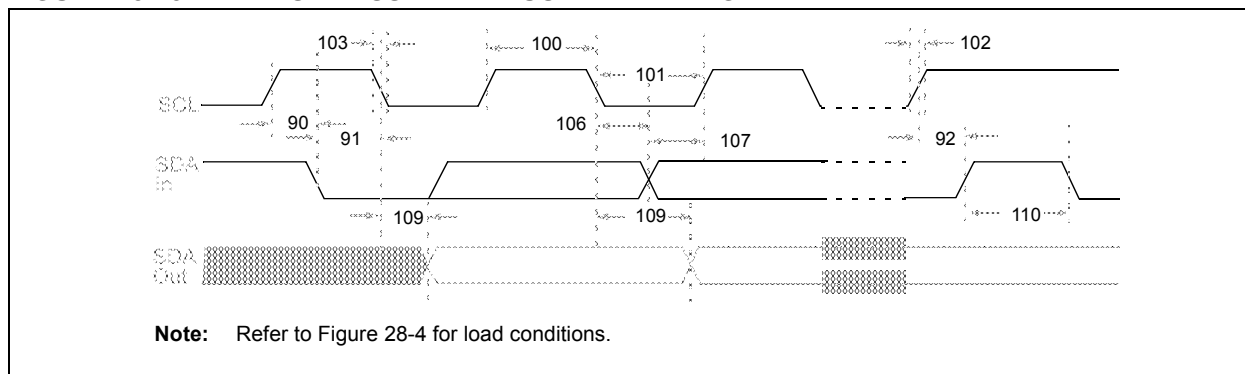


**TABLE 28-21: MASTER SSP I<sup>2</sup>C™ BUS START/STOP BITS REQUIREMENTS**

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	$2(T_{OSC})(BRG + 1)$	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	$2(T_{OSC})(BRG + 1)$	—		
			1 MHz mode <sup>(1)</sup>	$2(T_{OSC})(BRG + 1)$	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	$2(T_{OSC})(BRG + 1)$	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	$2(T_{OSC})(BRG + 1)$	—		
			1 MHz mode <sup>(1)</sup>	$2(T_{OSC})(BRG + 1)$	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	$2(T_{OSC})(BRG + 1)$	—	ns	
			400 kHz mode	$2(T_{OSC})(BRG + 1)$	—		
			1 MHz mode <sup>(1)</sup>	$2(T_{OSC})(BRG + 1)$	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	$2(T_{OSC})(BRG + 1)$	—	ns	
			400 kHz mode	$2(T_{OSC})(BRG + 1)$	—		
			1 MHz mode <sup>(1)</sup>	$2(T_{OSC})(BRG + 1)$	—		

**Note 1:** Maximum pin capacitance = 10 pF for all I<sup>2</sup>C™ pins.

**FIGURE 28-18: MASTER SSP I<sup>2</sup>C™ BUS DATA TIMING**



# PIC18F2455/2550/4455/4550

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## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**