



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	24KB (12K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4455-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Din Nama	Pin Number	Pin	Buffer	Description					
Pin Name	PDIP, SOIC	Туре	Туре	2000.19.1011					
MCLR/VPP/RE3 MCLR	1	I	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.					
VPP		Р		Programming voltage input.					
RE3		I	ST	Digital input.					
OSC1/CLKI OSC1 CLKI	9	 	Analog Analog	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)					
OSC2/CLKO/RA6 OSC2	10	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.					
CLKO		0	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.					
RA6		I/O	TTL	General purpose I/O pin.					
Legend: TTL = TTL cor ST = Schmitt	npatible in Trigger inp	put out with	CMOS le	CMOS = CMOS compatible input or output evels I = Input					

S levels I = Input P = Power

O = Output

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

2.0 OSCILLATOR CONFIGURATIONS

2.1 Overview

Devices in the PIC18F2455/2550/4455/4550 family incorporate a different oscillator and microcontroller clock system than previous PIC18F devices. The addition of the USB module, with its unique requirements for a stable clock source, make it necessary to provide a separate clock source that is compliant with both USB low-speed and full-speed specifications.

To accommodate these requirements, PIC18F2455/ 2550/4455/4550 devices include a new clock branch to provide a 48 MHz clock for full-speed USB operation. Since it is driven from the primary clock source, an additional system of prescalers and postscalers has been added to accommodate a wide range of oscillator frequencies. An overview of the oscillator structure is shown in Figure 2-1.

Other oscillator features used in PIC18 enhanced microcontrollers, such as the internal oscillator block and clock switching, remain the same. They are discussed later in this chapter.

2.1.1 OSCILLATOR CONTROL

The operation of the oscillator in PIC18F2455/2550/ 4455/4550 devices is controlled through two Configuration registers and two control registers. Configuration registers, CONFIG1L and CONFIG1H, select the oscillator mode and USB prescaler/postscaler options. As Configuration bits, these are set when the device is programmed and left in that configuration until the device is reprogrammed.

The OSCCON register (Register 2-2) selects the Active Clock mode; it is primarily used in controlling clock switching in power-managed modes. Its use is discussed in **Section 2.4.1** "Oscillator Control **Register**".

The OSCTUNE register (Register 2-1) is used to trim the INTRC frequency source, as well as select the low-frequency clock source that drives several special features. Its use is described in **Section 2.2.5.2 "OSCTUNE Register"**.

2.2 Oscillator Types

PIC18F2455/2550/4455/4550 devices can be operated in twelve distinct oscillator modes. In contrast with previous PIC18 enhanced microcontrollers, four of these modes involve the use of two oscillator types at once. Users can program the FOSC3:FOSC0 Configuration bits to select one of these modes:

- 1. XT Crystal/Resonator
- 2. HS High-Speed Crystal/Resonator
- 3. HSPLL High-Speed Crystal/Resonator with PLL Enabled
- 4. EC External Clock with Fosc/4 Output
- 5. ECIO External Clock with I/O on RA6
- 6. ECPLL External Clock with PLL Enabled and Fosc/4 Output on RA6
- 7. ECPIO External Clock with PLL Enabled, I/O on RA6
- 8. INTHS Internal Oscillator used as Microcontroller Clock Source, HS Oscillator used as USB Clock Source
- 9. INTIO Internal Oscillator used as Microcontroller Clock Source, EC Oscillator used as USB Clock Source, Digital I/O on RA6
- 10. INTCKO Internal Oscillator used as Microcontroller Clock Source, EC Oscillator used as USB Clock Source, Fosc/4 Output on RA6

2.2.1 OSCILLATOR MODES AND USB OPERATION

Because of the unique requirements of the USB module, a different approach to clock operation is necessary. In previous PIC[®] devices, all core and peripheral clocks were driven by a single oscillator source; the usual sources were primary, secondary or the internal oscillator. With PIC18F2455/2550/4455/4550 devices, the primary oscillator becomes part of the USB module and cannot be associated to any other clock source. Thus, the USB module must be clocked from the primary clock source; however, the microcontroller core and other peripherals can be separately clocked from the secondary or internal oscillators as before.

Because of the timing requirements imposed by USB, an internal clock of either 6 MHz or 48 MHz is required while the USB module is enabled. Fortunately, the microcontroller and other peripherals are not required to run at this clock speed when using the primary oscillator. There are numerous options to achieve the USB module clock requirement and still provide flexibility for clocking the rest of the device from the primary oscillator source. These are detailed in **Section 2.3 "Oscillator Settings for USB"**.

3.1.3 CLOCK TRANSITIONS AND STATUS INDICATORS

The length of the transition between clock sources is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Three bits indicate the current clock source and its status. They are:

- OSTS (OSCCON<3>)
- IOFS (OSCCON<2>)
- T1RUN (T1CON<6>)

In general, only one of these bits will be set while in a given power-managed mode. When the OSTS bit is set, the primary clock is providing the device clock. When the IOFS bit is set, the INTOSC output is providing a stable, 8 MHz clock source to a divider that actually drives the device clock. When the T1RUN bit is set, the Timer1 oscillator is providing the clock. If none of these bits are set, then either the INTRC clock source is clocking the device, or the INTOSC source is not yet stable.

If the internal oscillator block is configured as the primary clock source by the FOSC3:FOSC0 Configuration bits, then both the OSTS and IOFS bits may be set when in PRI_RUN or PRI_IDLE modes. This indicates that the primary clock (INTOSC output) is

generating a stable 8 MHz output. Entering another power-managed RC mode at the same frequency would clear the OSTS bit.

- Note 1: Caution should be used when modifying a single IRCF bit. If VDD is less than 3V, it is possible to select a higher clock speed than is supported by the low VDD. Improper device operation may result if the VDD/Fosc specifications are violated.
 - 2: Executing a SLEEP instruction does not necessarily place the device into Sleep mode. It acts as the trigger to place the controller into either the Sleep mode, or one of the Idle modes, depending on the setting of the IDLEN bit.

3.1.4 MULTIPLE SLEEP COMMANDS

The power-managed mode that is invoked with the SLEEP instruction is determined by the setting of the IDLEN bit at the time the instruction is executed. If another SLEEP instruction is executed, the device will enter the power-managed mode specified by IDLEN at that time. If IDLEN has changed, the device will enter the new power-managed mode specified by the new setting.

Upon resuming normal operation after waking from Sleep or Idle, the internal state machines require at least one TcY delay before another SLEEP instruction can be executed. If two back to back SLEEP instructions will be executed, the process shown in Example 3-1 should be used.

EXAMPLE 3-1: EXECUTING BACK TO BACK SLEEP INSTRUCTIONS

SLEEP NOP ;Wait at least 1 Tcy before executing another sleep instruction SLEEP

3.2 Run Modes

In the Run modes, clocks to both the core and peripherals are active. The difference between these modes is the clock source.

3.2.1 PRI_RUN MODE

The PRI_RUN mode is the normal, full-power execution mode of the microcontroller. This is also the default mode upon a device Reset unless Two-Speed Start-up is enabled (see **Section 25.3 "Two-Speed Start-up"** for details). In this mode, the OSTS bit is set. The IOFS bit may be set if the internal oscillator block is the primary clock source (see **Section 2.4.1 "Oscillator Control Register"**).

3.2.2 SEC_RUN MODE

The SEC_RUN mode is the compatible mode to the "clock switching" feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high-accuracy clock source.

3.2.3 RC_RUN MODE

In RC_RUN mode, the CPU and peripherals are clocked from the internal oscillator block using the INTOSC multiplexer; the primary clock is shut down. When using the INTRC source, this mode provides the best power conservation of all the Run modes while still executing code. It works well for user applications which are not highly timing sensitive or do not require high-speed clocks at all times.

If the primary clock source is the internal oscillator block (either INTRC or INTOSC), there are no distinguishable differences between the PRI_RUN and RC_RUN modes during execution. However, a clock switch delay will occur during entry to and exit from RC_RUN mode. Therefore, if the primary clock source is the internal oscillator block, the use of RC_RUN mode is not recommended.

This mode is entered by setting SCS1 to '1'. Although it is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. When the clock source is switched to the INTOSC multiplexer (see Figure 3-3), the primary oscillator is shut down and the OSTS bit is cleared. The IRCF bits may be modified at any time to immediately change the clock speed.

Note: Caution should be used when modifying a single IRCF bit. If VDD is less than 3V, it is possible to select a higher clock speed than is supported by the low VDD. Improper device operation may result if the VDD/Fosc specifications are violated.

If the IRCF bits and the INTSRC bit are all clear, the INTOSC output is not enabled and the IOFS bit will remain clear; there will be no indication of the current clock source. The INTRC source is providing the device clocks.

If the IRCF bits are changed from all clear (thus, enabling the INTOSC output), or if INTSRC is set, the IOFS bit becomes set after the INTOSC output becomes stable. Clocks to the device continue while the INTOSC source stabilizes after an interval of TIOBST.

If the IRCF bits were previously at a non-zero value or if INTSRC was set before setting SCS1 and the INTOSC source was already stable, the IOFS bit will remain set.

On transitions from RC_RUN mode to PRI_RUN mode, the device continues to be clocked from the INTOSC multiplexer while the primary clock is started. When the primary clock becomes ready, a clock switch to the primary clock occurs (see Figure 3-4). When the clock switch is complete, the IOFS bit is cleared, the OSTS bit is set and the primary clock is providing the device clock. The IDLEN and SCS bits are not affected by the switch. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

PIC18F2455/2550/4455/4550

						<u>'</u>				
File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page
OSCCON	IDLEN	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0	0100 q000	54, 33
HLVDCON	VDIRMAG	_	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0-00 0101	54, 285
WDTCON	—	—	-	—	—	—	—	SWDTEN	0	54, 304
RCON	IPEN	SBOREN ⁽²⁾	_	RI	TO	PD	POR	BOR	0q-1 11q0	54, 46
TMR1H	Timer1 Regis	XXXX XXXX	54, 136							
TMR1L	Timer1 Regis	XXXX XXXX	54, 136							
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	0000 0000	54, 131
TMR2	Timer2 Regis	ter							0000 0000	54, 138
PR2	Timer2 Period	d Register							1111 1111	54, 138
T2CON	_	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	54, 137
SSPBUF	MSSP Receiv	/e Buffer/Trans	smit Register						XXXX XXXX	54, 198, 207
SSPADD	MSSP Addres	ss Register in	I ² C™ Slave m	ode. MSSP Ba	aud Rate Relo	ad Register in	I ² C [™] Master	mode.	0000 0000	54, 207
SSPSTAT	SMP	CKE	D/Ā	Р	S	R/W	UA	BF	0000 0000	54, 198, 208
SSPCON1	WCOL	SSPOV	SSPEN	СКР	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	54, 199, 209
SSPCON2	GCEN	ACKSTAT	ACKDT/ ADMSK5 ⁽⁷⁾	ACKEN/ ADMSK4 ⁽⁷⁾	RCEN/ ADMSK3 ⁽⁷⁾	PEN/ ADMSK2 ⁽⁷⁾	RSEN/ ADMSK1 ⁽⁷⁾	SEN	0000 0000	54, 210
ADRESH	A/D Result R	egister High B	yte	•			•		XXXX XXXX	54, 274
ADRESL	A/D Result Re	egister Low By	/te						XXXX XXXX	54, 274
ADCON0	_	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	00 0000	54, 265
ADCON1	—	_	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	00 0qqq	54, 266
ADCON2	ADFM	_	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	0-00 0000	54, 267
CCPR1H	Capture/Com	pare/PWM Re	gister 1 High I	Byte					XXXX XXXX	55, 144
CCPR1L	Capture/Com	pare/PWM Re	gister 1 Low E	Byte					XXXX XXXX	55, 144
CCP1CON	P1M1 ⁽³⁾	P1M0 ⁽³⁾	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	55, 143, 151
CCPR2H	Capture/Com	pare/PWM Re	gister 2 High I	Byte					XXXX XXXX	55, 144
CCPR2L	Capture/Com	pare/PWM Re	gister 2 Low E	Byte					XXXX XXXX	55, 144
CCP2CON	_	_	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	55, 143
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	_	WUE	ABDEN	0100 0-00	55, 246
ECCP1DEL	PRSEN	PDC6 ⁽³⁾	PDC5 ⁽³⁾	PDC4 ⁽³⁾	PDC3 ⁽³⁾	PDC2 ⁽³⁾	PDC1 ⁽³⁾	PDC0 ⁽³⁾	0000 0000	55, 160
ECCP1AS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1 ⁽³⁾	PSSBD0 ⁽³⁾	0000 0000	55, 161
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000 0000	55, 281
CMCON	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	55, 275
TMR3H	Timer3 Regis	ter High Byte							XXXX XXXX	55, 141
TMR3L	Timer3 Regis	ter Low Byte		1	1	1	1		XXXX XXXX	55, 141
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	0000 0000	55, 139
SPBRGH	EUSART Bau	id Rate Gener	ator Register I	High Byte					0000 0000	55, 247
SPBRG	EUSART Bau	ud Rate Gener	ator Register I	Low Byte					0000 0000	55, 247
RCREG	EUSART Red	eive Register							0000 0000	55, 256
TXREG	EUSART Tra	nsmit Register		r	1	1	r		0000 0000	55, 253
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	55, 244
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	55, 245

TABLE 5-2: REGISTER FILE SUMMARY (CONTINUED)

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

Note 1: Bit 21 of the TBLPTRU allows access to the device Configuration bits.

2: The SBOREN bit is only available when BOREN<1:0> = 01; otherwise, the bit reads as '0'.

3: These registers and/or bits are not implemented on 28-pin devices and are read as '0'. Reset values are shown for 40/44-pin devices; individual unimplemented bits should be interpreted as '-'.

4: RA6 is configured as a port pin based on various primary oscillator modes. When the port pin is disabled, all of the associated bits read '0'.

5: RE3 is only available as a port pin when the MCLRE Configuration bit is clear; otherwise, the bit reads as '0'.

6: RC5 and RC4 are only available as port pins when the USB module is disabled (UCON<3> = 0).

7: I^2C^{TM} Slave mode only.

NOTES:

6.5 Writing to Flash Program Memory

The minimum programming block is 16 words or 32 bytes. Word or byte programming is not supported.

Table writes are used internally to load the holding registers needed to program the Flash memory. There are 32 holding registers used by the table writes for programming.

Since the Table Latch (TABLAT) is only a single byte, the TBLWT instruction may need to be executed 32 times for each programming operation. All of the table write operations will essentially be short writes because only the holding registers are written. At the end of updating the 32 holding registers, the EECON1 register must be written to in order to start the programming operation with a long write.

The long write is necessary for programming the internal Flash. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

The EEPROM on-chip timer controls the write time. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device.

Note: The default value of the holding registers on device Resets and after write operations is FFh. A write of FFh to a holding register does not modify that byte. This means that individual bytes of program memory may be modified, provided that the change does not attempt to change any bit from a '0' to a '1'. When modifying individual bytes, it is not necessary to load all 32 holding registers before executing a write operation.





6.5.1 FLASH PROGRAM MEMORY WRITE SEQUENCE

The sequence of events for programming an internal program memory location should be:

- 1. Read 64 bytes into RAM.
- 2. Update data values in RAM as necessary.
- 3. Load Table Pointer register with address being erased.
- 4. Execute the Row Erase procedure.
- 5. Load Table Pointer register with address of first byte being written.
- 6. Write 32 bytes into the holding registers with auto-increment.
- Set the EECON1 register for the write operation:
 set EEPGD bit to point to program memory;
 - clear the CFGS bit to access program memory;
 - set WREN to enable byte writes.

- 8. Disable interrupts.
- 9. Write 55h to EECON2.
- 10. Write 0AAh to EECON2.
- 11. Set the WR bit. This will begin the write cycle.
- 12. The CPU will stall for duration of the write (about 2 ms using internal timer).
- 13. Re-enable interrupts.
- 14. Repeat steps 6 through 14 once more to write 64 bytes.
- 15. Verify the memory (table read).

This procedure will require about 8 ms to update one row of 64 bytes of memory. An example of the required code is given in Example 6-3.

Note: Before setting the WR bit, the Table Pointer address needs to be within the intended address range of the 32 bytes in the holding register.

EXAMPLE 6-3:	WRITIN	G TO FLASH PROGRA	M MEMORY (CONTINUED)
PROGRAM_MEMORY			
	BSF	EECON1, EEPGD	; point to Flash program memory
	BCF	EECON1, CFGS	; access Flash program memory
	BSF	EECON1, WREN	; enable write to memory
	BCF	INTCON, GIE	; disable interrupts
	MOVLW	55h	
Required	MOVWF	EECON2	; write 55h
Sequence	MOVLW	0AAh	
	MOVWF	EECON2	; write OAAh
	BSF	EECON1, WR	; start program (CPU stall)
	DECFSZ	COUNTER1	
	BRA	WRITE BUFFER BACK	
	BSF	INTCON, GIE	; re-enable interrupts
	BCF	EECON1, WREN	; disable write to memory

6.5.2 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

6.5.3 UNEXPECTED TERMINATION OF WRITE OPERATION

If a write is terminated by an unplanned event, such as loss of power or an unexpected Reset, the memory location just programmed should be verified and reprogrammed if needed. If the write operation is interrupted by a MCLR Reset or a WDT Time-out Reset during normal operation, the user can check the WRERR bit and rewrite the location(s) as needed.

6.5.4 PROTECTION AGAINST SPURIOUS WRITES

To protect against spurious writes to Flash program memory, the write initiate sequence must also be followed. See **Section 25.0** "**Special Features of the CPU**" for more detail.

6.6 Flash Program Operation During Code Protection

See Section 25.5 "Program Verification and Code Protection" for details on code protection of Flash program memory.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
TBLPTRU			bit 21 ⁽¹⁾	Program Me	emory Table I	Pointer Uppe	r Byte (TBLP	TR<20:16>)	53
TBLPTRH	Program M	emory Table	e Pointer H	igh Byte (TB	LPTR<15:8	>)			53
TBLPTRL	Program M	emory Table	e Pointer Lo	ow Byte (TB	LPTR<7:0>)				53
TABLAT	Program M	emory Table	e Latch						53
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	53
EECON2	EEPROM C	Control Regi	ster 2 (not	a physical re	egister)				55
EECON1	EEPGD	CFGS	_	FREE	WRERR	WREN	WR	RD	55
IPR2	OSCFIP	CMIP	USBIP	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	56
PIR2	OSCFIF	CMIF	USBIF	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	56
PIE2	OSCFIE	CMIE	USBIE	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	56

TABLE 6-2: REGISTERS ASSOCIATED WITH PROGRAM FLASH MEMORY

Legend: — = unimplemented, read as '0'. Shaded cells are not used during Flash/EEPROM access.

Note 1: Bit 21 of the TBLPTRU allows access to the device Configuration bits.

Pin	Function	TRIS Setting	I/O	I/O Type	Description				
RA0/AN0	RA0	0	OUT	DIG	LATA<0> data output; not affected by analog input.				
		1	IN	TTL	PORTA<0> data input; disabled when analog input enabled.				
	AN0	1	IN	ANA	A/D Input Channel 0 and Comparator C1- input. Default configuration on POR; does not affect digital output.				
RA1/AN1	RA1	LATA<1> data output; not affected by analog input.							
		1	IN	TTL	PORTA<1> data input; reads '0' on POR.				
	AN1	1	IN	ANA	A/D Input Channel 1 and Comparator C2- input. Default configuration on POR; does not affect digital output.				
RA2/AN2/ Vref-/CVref	RA2	0	OUT	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output enabled.				
		1	IN	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CVREF output enabled.				
	AN2	1	IN	ANA	A/D Input Channel 2 and Comparator C2+ input. Default configuration on POR; not affected by analog output.				
	VREF-	1	IN	ANA	A/D and comparator voltage reference low input.				
	CVREF	х	OUT	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.				
RA3/AN3/	RA3	0	OUT	DIG	LATA<3> data output; not affected by analog input.				
VREF+		1	IN	TTL	PORTA<3> data input; disabled when analog input enabled.				
	AN3	1	IN	ANA	A/D Input Channel 3 and Comparator C1+ input. Default configurati on POR.				
	VREF+	1	IN	ANA	A/D and comparator voltage reference high input.				
RA4/T0CKI/	RA4	0	OUT	DIG	LATA<4> data output; not affected by analog input.				
C10UT/RCV		1	IN	ST	PORTA<4> data input; disabled when analog input enabled.				
	T0CKI	1	IN	ST	Timer0 clock input.				
	C10UT	0	OUT	DIG	Comparator 1 output; takes priority over port data.				
	RCV	x	IN	TTL	External USB transceiver RCV input.				
RA5/AN4/SS/	RA5	0	OUT	DIG	LATA<5> data output; not affected by analog input.				
HLVDIN/C2OUT		1	IN	TTL	PORTA<5> data input; disabled when analog input enabled.				
	AN4	1	IN	ANA	A/D Input Channel 4. Default configuration on POR.				
	SS	1	IN	TTL	Slave select input for MSSP module.				
	HLVDIN	1	IN	ANA	High/Low-Voltage Detect external trip point input.				
	C2OUT	0	OUT	DIG	Comparator 2 output; takes priority over port data.				
OSC2/CLKO/	OSC2	х	OUT	ANA	Main oscillator feedback output connection (all XT and HS modes).				
RA6	CLKO	х	OUT	DIG	System cycle clock output (Fosc/4); available in EC, ECPLL and INTCKO modes.				
	RA6	0	OUT	DIG	LATA<6> data output. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.				
		1	IN	TTL	PORTA<6> data input. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.				

TABLE 10-1: PORTA I/O SUMMARY

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input,

TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

		TRIS			- • · ·
Pin	Function	Setting	I/O	І/О Туре	Description
RD0/SPP0	RD0	0	OUT	DIG	LATD<0> data output.
		1	IN	ST	PORTD<0> data input.
	SPP0	1	OUT	DIG	SPP<0> output data; takes priority over port data.
		1	IN	TTL	SPP<0> input data.
RD1/SPP1	RD1	0	OUT	DIG	LATD<1> data output.
		1	IN	ST	PORTD<1> data input.
	SPP1	1	OUT	DIG	SPP<1> output data; takes priority over port data.
		1	IN	TTL	SPP<1> input data.
RD2/SPP2	RD2	0	OUT	DIG	LATD<2> data output.
		1	IN	ST	PORTD<2> data input.
	SPP2	1	OUT	DIG	SPP<2> output data; takes priority over port data.
		1	IN	TTL	SPP<2> input data.
RD3/SPP3	RD3	0	OUT	DIG	LATD<3> data output.
		1	IN	ST	PORTD<3> data input.
	SPP3	1	OUT	DIG	SPP<3> output data; takes priority over port data.
		1	IN	TTL	SPP<3> input data.
RD4/SPP4	RD4	0	OUT	DIG	LATD<4> data output.
		1	IN	ST	PORTD<4> data input.
	SPP4	1	OUT	DIG	SPP<4> output data; takes priority over port data.
		1	IN	TTL	SPP<4> input data.
RD5/SPP5/P1B	RD5	0	OUT	DIG	LATD<5> data output
		1	IN	ST	PORTD<5> data input
	SPP5	1	OUT	DIG	SPP<5> output data; takes priority over port data.
		1	IN	TTL	SPP<5> input data.
	P1B	0	OUT	DIG	ECCP1 Enhanced PWM output, Channel B; takes priority over port and SPP data. ⁽¹⁾
RD6/SPP6/P1C	RD6	0	OUT	DIG	LATD<6> data output.
		1	IN	ST	PORTD<6> data input.
	SPP6	1	OUT	DIG	SPP<6> output data; takes priority over port data.
		1	IN	TTL	SPP<6> input data.
	P1C	0	OUT	DIG	ECCP1 Enhanced PWM output, Channel C; takes priority over port and SPP data. ⁽¹⁾
RD7/SPP7/P1D	RD7	0	OUT	DIG	LATD<7> data output.
		1	IN	ST	PORTD<7> data input.
	SPP7	1	OUT	DIG	SPP<7> output data; takes priority over port data.
		1	IN	TTL	SPP<7> input data.
	P1D	0	OUT	DIG	ECCP1 Enhanced PWM output, Channel D; takes priority over port and SPP data. ⁽¹⁾

TABLE 10-7: PORTD I/O SUMMARY

Legend: OUT = Output, IN = Input, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input

Note 1: May be configured for tri-state during Enhanced PWM shutdown events.

17.0 UNIVERSAL SERIAL BUS (USB)

This section describes the details of the USB peripheral. Because of the very specific nature of the module, knowledge of USB is expected. Some high-level USB information is provided in **Section 17.10 "Overview of USB"** only for application design reference. Designers are encouraged to refer to the official specification published by the USB Implementers Forum (USB-IF) for the latest information. USB specification Revision 2.0 is the most current specification at the time of publication of this document.

17.1 Overview of the USB Peripheral

The PIC18FX455/X550 device family contains a full-speed and low-speed compatible USB Serial Interface Engine (SIE) that allows fast communication between any USB host and the PIC[®] microcontroller. The SIE can be interfaced directly to the USB, utilizing the internal transceiver, or it can be connected through an external transceiver. An internal 3.3V regulator is also available to power the internal transceiver in 5V applications.

Some special hardware features have been included to improve performance. Dual port memory in the device's data memory space (USB RAM) has been supplied to share direct memory access between the microcontroller core and the SIE. Buffer descriptors are also provided, allowing users to freely program endpoint memory usage within the USB RAM space. A Streaming Parallel Port has been provided to support the uninterrupted transfer of large volumes of data, such as isochronous data, to external memory buffers.

Figure 17-1 presents a general overview of the USB peripheral and its features.



FIGURE 17-1: USB PERIPHERAL AND OPTIONS









19.4.4.5 Clock Synchronization and the CKP bit

When the CKP bit is cleared, the SCL output is forced to '0'. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has

already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2 C bus have deasserted SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 19-14).



FIGURE 19-14: CLOCK SYNCHRONIZATION TIMING

PIC18F2455/2550/4455/4550



© 2009 Microchip Technology Inc.

U-0	U-0		R/W-	0	R/W	-0	R/W	′-0 ⁽¹⁾	R	2/W(1)		R/W	(1)	R	/W ⁽¹⁾
_	_		VCFG	G1	VCF	G0	PCF	=G3	P	CFG2		PCFC	G1	PC	CFG0
bit 7											•				bit 0
Legend:															
R = Readat	ole bit	N	/ = Writ	table bi	t		U = U	nimple	mente	d bit, re	ead as	ʻ0'			
-n = Value a	at POR	'1	' = Bit i	is set			'0' = B	it is cle	eared		X	= Bit is	s unkn	lown	
bit 7-6	Unimpler	nenteo	d: Read	d as '0'											
bit 5	VCFG1: \	/oltage	Refere	ence C	onfigur	ation b	oit (Vre	EF- SOU	rce)						
	1 = VREF- 0 = VSS	(AN2)			5				,						
bit 4	VCFG0 : \	/oltage	Refere	ence C	onfigur	ation b	oit (Vre	EF+ SO	urce)						
	1 = VREF+	- (AN3)		•		•		,						
	0 = V DD														
bit 3-0	PCFG3:P	CFG0:	: A/D P	ort Co	nfigurat	tion Co	ontrol b	oits:							
	PCEG2:	3	~	0			(2)	(2)	(2)	_			_]
	PCFG0	AN1	AN1	AN1	ANS	ANS	AN7	ANG	ANE	AN4	AN3	AN2	AN1	ANG	
	₀₀₀₀ (1)	А	Α	Α	Α	Α	А	Α	Α	Α	Α	Α	Α	Α	
	0001	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	
	0010	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	
	0011	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	
	0100	D	D	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	
	0101	D	D	D	А	Α	Α	А	Α	Α	Α	А	Α	Α	
	0110	D	D	D	D	Α	Α	Α	Α	Α	Α	А	Α	Α	
	0111 (1)	D	D	D	D	D	Α	А	Α	Α	А	А	А	А	
	1000	D	D	D	D	D	D	Α	Α	Α	Α	Α	Α	Α	
	1001	D	D	D	D	D	D	D	Α	Α	Α	Α	Α	Α	
	1010	D	D	D	D	D	D	D	D	Α	Α	Α	А	Α	1
	1011	D	D	D	D	D	D	D	D	D	Α	Α	А	А	
	1100	D	D	D	D	D	D	D	D	D	D	А	А	А	
	1101	D	D	D	D	D	D	D	D	D	D	D	Α	Α	

REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1



D

D

D

D

D

D

D = Digital I/O

D

D

D

D

D

D

D

D

D

D

D

D

А

D

2: AN5 through AN7 are available only on 40/44-pin devices.

D

D

D

D

1110

1111

D

D

A = Analog input

25.2 Watchdog Timer (WDT)

For PIC18F2455/2550/4455/4550 devices, the WDT is driven by the INTRC source. When the WDT is enabled, the clock source is also enabled. The nominal WDT period is 4 ms and has the same stability as the INTRC oscillator.

The 4 ms period of the WDT is multiplied by a 16-bit postscaler. Any output of the WDT postscaler is selected by a multiplexer, controlled by bits in Configuration Register 2H. Available periods range from 4 ms to 131.072 seconds (2.18 minutes). The WDT and postscaler are cleared when any of the following events occur: a SLEEP or CLRWDT instruction is executed, the IRCF bits (OSCCON<6:4>) are changed or a clock failure has occurred.

- Note 1: The CLRWDT and SLEEP instructions clear the WDT and postscaler counts when executed.
 - 2: Changing the setting of the IRCF bits (OSCCON<6:4>) clears the WDT and postscaler counts.
 - **3:** When a CLRWDT instruction is executed, the postscaler count will be cleared.

25.2.1 CONTROL REGISTER

Register 25-15 shows the WDTCON register. This is a readable and writable register which contains a control bit that allows software to override the WDT enable Configuration bit, but only if the Configuration bit has disabled the WDT.



FIGURE 25-1: WDT BLOCK DIAGRAM

25.5.1 PROGRAM MEMORY CODE PROTECTION

The program memory may be read to or written from any location using the table read and table write instructions. The device ID may be read with table reads. The Configuration registers may be read and written with the table read and table write instructions.

In normal execution mode, the CPx bits have no direct effect. CPx bits inhibit external reads and writes. A block of user memory may be protected from table writes if the WRTx Configuration bit is '0'. The EBTRx bits control table reads. For a block of user memory with the EBTRx bit set to '0', a table read instruction that executes from within that block is allowed to read. A table read instruction that executes from a location outside of that block is not allowed to read and will result in reading '0's. Figures 25-6 through 25-8 illustrate table write and table read protection.

Note: Code protection bits may only be written to a '0' from a '1' state. It is not possible to write a '1' to a bit in the '0' state. Code protection bits are only set to '1' by a full Chip Erase or Block Erase function. The full Chip Erase and Block Erase functions can only be initiated via ICSP operation or an external programmer.

FIGURE 25-6: TABLE WRITE (WRTx) DISALLOWED



PIC18F2455/2550/4455/4550



FIGURE 28-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 28-8: BROWN-OUT RESET TIMING



TABLE 28-12:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER
AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Тур	Мах	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	—		μS	
31	Twdt	Watchdog Timer Time-out Period (no postscaler)	3.5	4.1	4.8	ms	
32	Tost	Oscillator Start-up Timer Period	1024 Tosc	_	1024 Tosc	_	Tosc = OSC1 period
33	TPWRT	Power-up Timer Period	57.0	65.5	77.1	ms	
34	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μS	
35	TBOR	Brown-out Reset Pulse Width	200	_	—	μS	$VDD \le BVDD$ (see D005)
36	TIRVST	Time for Internal Reference Voltage to become Stable	—	20	50	μS	
37	Tlvd	Low-Voltage Detect Pulse Width	200	_	—	μS	$V\text{DD} \leq V\text{LVD}$
38	TCSD	CPU Start-up Time	5	_	10	μS	
39	TIOBST	Time for INTOSC to Stabilize	_	1		ms	



FIGURE 28-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)

TABLE 28-18: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
70	TssL2scH, TssL2scL	$\overline{\text{SS}} \downarrow \text{to SCK} \downarrow \text{or SCK} \uparrow \text{Input}$	3 Тсү	_	ns		
71	TscH	SCK Input High Time	Continuous	1.25 Tcy + 30		ns	
71A		(Slave mode)	Single Byte	40	—	ns	(Note 1)
72	TscL	SCK Input Low Time	Continuous	1.25 Tcy + 30		ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73A	Tb2b	Last Clock Edge of Byte 1 to the First	Clock Edge of Byte 2	1.5 Tcy + 40	_	ns	(Note 2)
74	TscH2diL, TscL2diL	Hold Time of SDI Data Input to SCK	35	—	ns		
75	TdoR	SDO Data Output Rise Time	PIC18FXXXX	—	25	ns	
			PIC18LFXXXX	—	45	ns	VDD = 2.0V
76	TdoF	SDO Data Output Fall Time		—	25	ns	
77	TssH2doZ	SS ↑ to SDO Output High-Impedance	ce	10	50	ns	
78	TscR	SCK Output Rise Time	PIC18FXXXX	—	25	ns	
		(Master mode)	PIC18LFXXXX	—	45	ns	VDD = 2.0V
79	TscF	SCK Output Fall Time (Master mode	e)	—	25	ns	
80	TscH2doV,	SDO Data Output Valid after SCK	PIC18FXXXX	—	50	ns	
	TscL2doV	Edge	PIC18LFXXXX	—	100	ns	VDD = 2.0V
82	TssL2doV	SDO Data Output Valid after $\overline{ ext{SS}}\downarrow$	PIC18FXXXX		50	ns	
		Edge	PIC18LFXXXX		100	ns	VDD = 2.0V
83	TscH2ssH, TscL2ssH	SS ↑ after SCK Edge		1.5 Tcy + 40	_	ns	

Note 1: Requires the use of Parameter 73A.

2: Only if Parameter 71A and 72A are used.

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available