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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

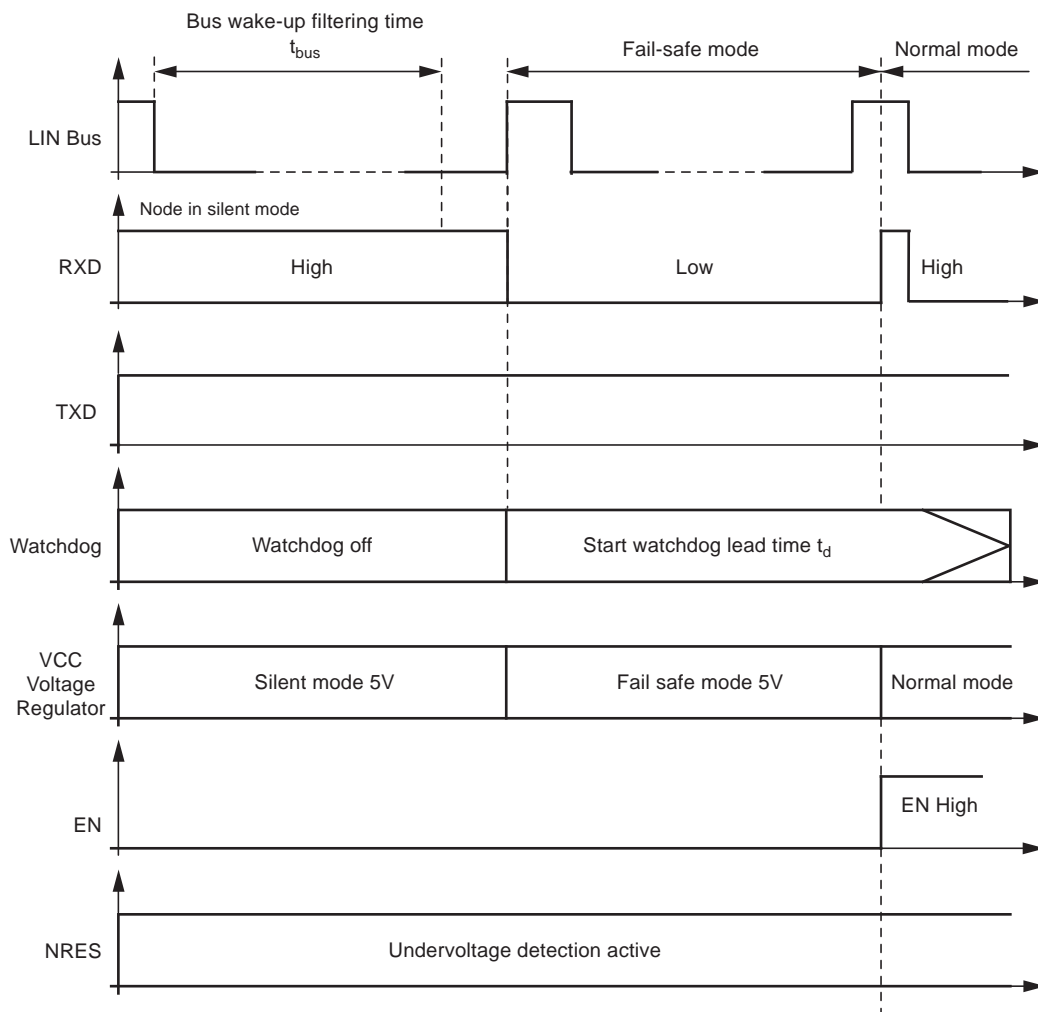
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TC)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ata6612c-plqw-1

A falling edge at the LIN pin followed by a dominant bus level maintained for a certain time period ($> t_{bus}$) and followed by a rising edge at the LIN pin (see Figure 3-4) result in a remote wake-up request. The device switches from silent mode to fail-safe mode. The remote wake-up request is indicated by a low level at the RXD pin to interrupt the microcontroller (see Figure 3-4). EN high can be used to switch directly to normal mode.

Figure 3-4. LIN Wake-up from Silent Mode



3.3.24.2 Worst Case Calculation with $R_{WD_OSC} = 51k$

The internal oscillator has a tolerance of 20%. This means that t_1 and t_2 can also vary by 20%. The worst case calculation for the watchdog period t_{wd} is calculated as follows.

The ideal watchdog time t_{wd} is between the maximum t_1 and the minimum t_1 plus the minimum t_2 .

$$t_{1,min} = 0.8 \times t_1 = 16.5ms, t_{1,max} = 1.2 \times t_1 = 24.8ms$$

$$t_{2,min} = 0.8 \times t_2 = 17.3ms, t_{2,max} = 1.2 \times t_2 = 26ms$$

$$t_{wdmax} = t_{1min} + t_{2min} = 16.5ms + 17.3ms = 33.8ms$$

$$t_{wdmin} = t_{1max} = 24.8ms$$

$$t_{wd} = 29.3ms \pm 4.5ms (\pm 15\%)$$

A microcontroller with an oscillator tolerance of $\pm 15\%$ is sufficient to supply the trigger inputs correctly.

Table 3-2. Typical Watchdog Timings

R_{WD_OSC} k	Oscillator Period $t_{osc}/\mu s$	Lead Time t_d/ms	Closed Window t_1/ms	Open Window t_2/ms	Trigger Period from Microcontroller t_{wd}/ms	Reset Time t_{nres}/ms
34	13.3	105	14.0	14.7	19.9	4
51	19.61	154.8	20.64	21.67	29.32	4
91	33.54	264.80	35.32	37.06	50.14	4
120	42.84	338.22	45.11	47.34	64.05	4

When the BOOTRST Fuse is unprogrammed, the boot section size set to 2K bytes and the IVSEL bit in the MCUCR register is set before any interrupts are enabled, the most typical and general program setup for the reset and interrupt vector addresses in ATA6613C is:

Address	Labels	Code	Comments
0x0000	RESET:	ldi r16,high(RAMEND);	Main program start
0x0001		out SPH,r16	; Set Stack Pointer to top of RAM
0x0002		ldi r16,low(RAMEND)	
0x0003		out SPL,r16	
0x0004		sei	; Enable interrupts
0x0005		<instr> xxx	
;			
.org 0xC02			
0x1C02		rjmp EXT_INT0	; IRQ0 Handler
0x1C04		rjmp EXT_INT1	; IRQ1 Handler
...	;
0x1C32		rjmp SPM_RDY	; Store Program Memory Ready Handler

When the BOOTRST fuse is programmed and the boot section size set to 2Kbytes, the most typical and general program setup for the reset and interrupt vector addresses in ATA6613C is:

Address	Labels	Code	Comments
.org 0x0002			
0x0002		rjmp EXT_INT0	; IRQ0 Handler
0x0004		rjmp EXT_INT1	; IRQ1 Handler
...	;
0x0032		rjmp SPM_RDY	; Store Program Memory Ready Handler
;			
.org 0x1C00			
0x1C00	RESET:	ldi r16,high(RAMEND);	Main program start
0x1C01		out SPH,r16	; Set Stack Pointer to top of RAM
0x1C02		ldi r16,low(RAMEND)	
0x1C03		out SPL,r16	
0x1C04		sei	; Enable interrupts
0x1C05		<instr> xxx	

When the BOOTRST fuse is programmed, the boot section size set to 2Kbytes and the IVSEL bit in the MCUCR register is set before any interrupts are enabled, the most typical and general program setup for the reset and interrupt vector addresses in ATA6613C is:

Address	Labels	Code	Comments
;			
.org 0x1C00			
0x1C00		rjmp RESET	; Reset handler
0x1C02		rjmp EXT_INT0	; IRQ0 Handler
0x1C04		rjmp EXT_INT1	; IRQ1 Handler
...	;
0x1C32		rjmp SPM_RDY	; Store Program Memory Ready Handler
;			
0x1C33	RESET:	ldi r16,high(RAMEND);	Main program start
0x1C34		out SPH,r16	; Set Stack Pointer to top of RAM
0x1C35		ldi r16,low(RAMEND)	
0x1C36		out SPL,r16	
0x1C37		sei	; Enable interrupts
0x1C38		<instr> xxx	

Table 5-50. Waveform Generation Mode Bit Description

Mode	WGM02	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on ⁽¹⁾⁽²⁾
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, phase correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	TOP	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, phase correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	TOP	TOP

Notes: 1. MAX = 0xFF

2. BOTTOM = 0x00

5.12.8.2 Timer/Counter Control Register B – TCCR0B

Bit	7	6	5	4	3	2	1	0	
	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	TCCR0B
Read/Write	W	W	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- Bit 7 – FOC0A: Force Output Compare A

The FOC0A bit is only active when the WGM bits specify a non-PWM mode.

However, for ensuring compatibility with future devices, this bit must be set to zero when TCCR0B is written when operating in PWM mode. When writing a logical one to the FOC0A bit, an immediate compare match is forced on the waveform generation unit. The OC0A output is changed according to its COM0A1:0 bits setting. Note that the FOC0A bit is implemented as a strobe. Therefore it is the value present in the COM0A1:0 bits that determines the effect of the forced compare.

A FOC0A strobe will not generate any interrupt, nor will it clear the timer in CTC mode using OCR0A as TOP.

The FOC0A bit is always read as zero.

- Bit 6 – FOC0B: Force Output Compare B

The FOC0B bit is only active when the WGM bits specify a non-PWM mode.

However, for ensuring compatibility with future devices, this bit must be set to zero when TCCR0B is written when operating in PWM mode. When writing a logical one to the FOC0B bit, an immediate compare match is forced on the waveform generation unit. The OC0B output is changed according to its COM0B1:0 bits setting. Note that the FOC0B bit is implemented as a strobe. Therefore it is the value present in the COM0B1:0 bits that determines the effect of the forced compare.

A FOC0B strobe will not generate any interrupt, nor will it clear the timer in CTC mode using OCR0B as TOP.

The FOC0B bit is always read as zero.

- Bits 5:4 – Res: Reserved Bits

These bits are reserved bits in the Atmel® ATA6612C/ATA6613C and will always read as zero.

- Bit 3 – WGM02: Waveform Generation Mode

See the description in the [Section 5.12.8.1 “Timer/Counter Control Register A – TCCR0A”](#) on page 107.

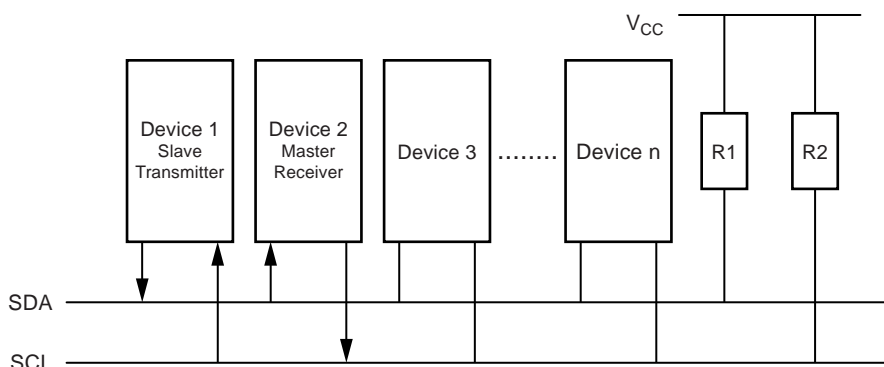
- Bits 2:0 – CS02:0: Clock Select

The three clock select bits select the clock source to be used by the Timer/Counter.

5.19.8.4 Slave Transmitter Mode

In the slave transmitter mode, a number of data bytes are transmitted to a master receiver (see Figure 5-94). All the status codes mentioned in this section assume that the prescaler bits are zero or are masked to zero.

Figure 5-94. Data Transfer in Slave Transmitter Mode



To initiate the slave transmitter mode, TWAR and TWCR must be initialized as follows:

TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE
value	Device's Own Slave Address							

The upper seven bits are the address to which the 2-wire serial interface will respond when addressed by a master. If the LSB is set, the TWI will respond to the general call address (0x00), otherwise it will ignore the general call address.

TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE
value	0	1	0	0	0	1	0	X

TWEN must be written to one to enable the TWI. The TWEA bit must be written to one to enable the acknowledgement of the device's own slave address or the general call address. TWSTA and TWSTO must be written to zero.

When TWAR and TWCR have been initialized, the TWI waits until it is addressed by its own slave address (or the general call address if enabled) followed by the data direction bit. If the direction bit is “1” (read), the TWI will operate in ST mode, otherwise SR mode is entered. After its own slave address and the write bit have been received, the TWINT flag is set and a valid status code can be read from TWSR. The status code is used to determine the appropriate software action. The appropriate action to be taken for each status code is detailed in Table 5-94 on page 217. The slave transmitter mode may also be entered if arbitration is lost while the TWI is in the master mode (see state 0xB0).

If the TWEA bit is written to zero during a transfer, the TWI will transmit the last byte of the transfer. State 0xC0 or state 0xC8 will be entered, depending on whether the master receiver transmits a NACK or ACK after the final byte. The TWI is switched to the not addressed Slave mode, and will ignore the master if it continues the transfer. Thus the master receiver receives all “1” as serial data. state 0xC8 is entered if the master demands additional data bytes (by transmitting ACK), even though the Slave has transmitted the last byte (TWEA zero and expecting NACK from the master).

While TWEA is zero, the TWI does not respond to its own slave address. However, the 2-wire serial bus is still monitored and address recognition may resume at any time by setting TWEA. This implies that the TWEA bit may be used to temporarily isolate the TWI from the 2-wire serial bus.

In all sleep modes other than Idle mode, the clock system to the TWI is turned off. If the TWEA bit is set, the interface can still acknowledge its own slave address or the general call address by using the 2-wire serial bus clock as a clock source. The part will then wake up from sleep and the TWI will hold the SCL clock low during the wake up and until the TWINT flag is cleared (by writing it to one). Further data transmission will be carried out as normal, with the AVR® clocks running as normal. Observe that if the AVR is set up with a long start-up time, the SCL line may be held low for a long time, blocking other data transmissions.

Note that the 2-wire serial Interface data register – TWDR does not reflect the last byte present on the bus when waking up from these sleep modes.

5.21 Analog-to-Digital Converter

5.21.1 Features

- " 10-bit resolution
- " 0.5LSB integral non-linearity
- " ± 2 LSB absolute accuracy
- " 13 - 260 μ s conversion time
- " Up to 15kSPS at maximum resolution
- " 6 multiplexed single ended input channels
- " 2 additional multiplexed single ended input channels (TQFP and QFN package only)
- " Optional left adjustment for ADC result readout
- " 0 to V_{CC} ADC input voltage range
- " Selectable 1.1V ADC reference voltage
- " Free running or single conversion mode
- " Interrupt on ADC conversion complete
- " Sleep mode noise canceler

The Atmel® ATA6612C/ATA6613C features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel analog multiplexer which allows eight single-ended voltage inputs constructed from the pins of Port A. The single-ended voltage inputs refer to 0V (GND).

The ADC contains a sample and hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in [Figure 5-100 on page 225](#).

The ADC has a separate analog supply voltage pin, AV_{CC} . AV_{CC} must not differ more than $\pm 0.3V$ from V_{CC} . See the paragraph [Section 5.21.5 "ADC Noise Canceler" on page 231](#) on how to connect this pin.

Internal reference voltages of nominally 1.1V or AV_{CC} are provided On-chip. The voltage reference may be externally decoupled at the AREF pin by a capacitor for better noise performance.

The power reduction ADC bit, PRADC, in [Section 5.7.7.1 "Power Reduction Register - PRR" on page 58](#) must be disabled by writing a logical zero to enable the ADC.

Figure 6-32. Analog to Digital Converter DNL versus V_{CC}

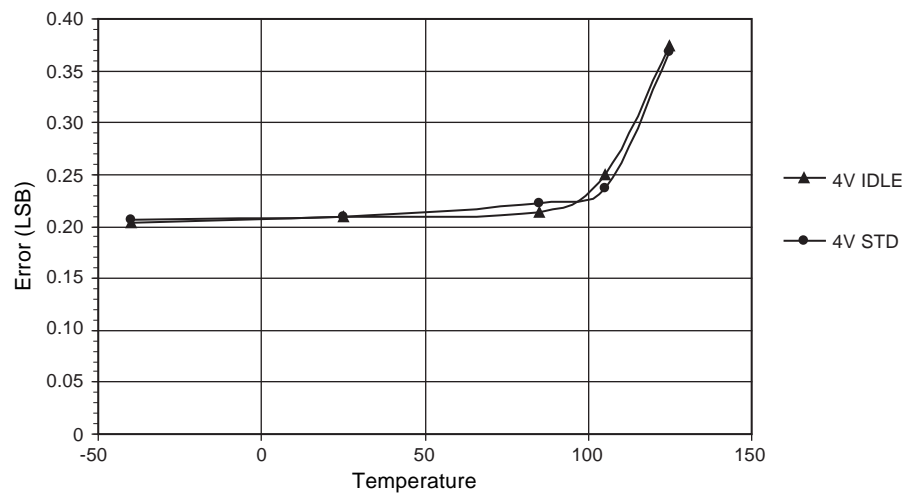
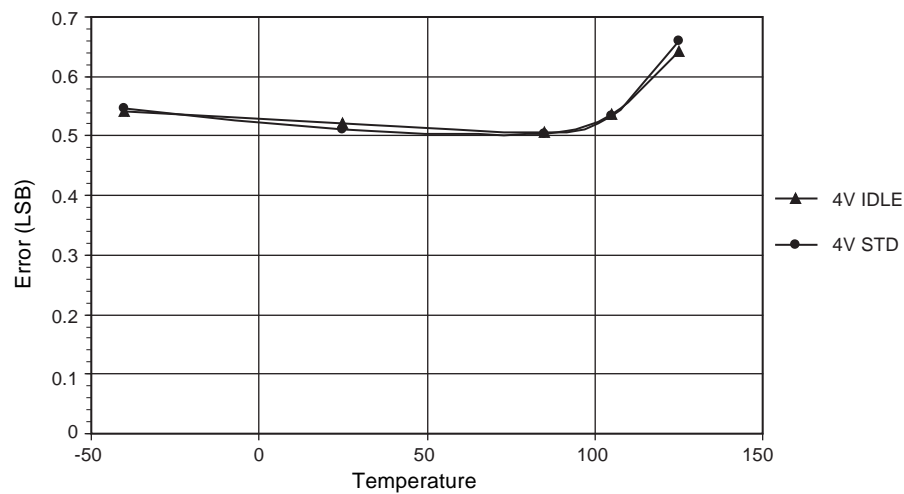


Figure 6-33. Analog to Digital Converter INL versus V_{CC}



6.4 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	–	–	–	–	–	–	–	–	
(0xFE)	Reserved	–	–	–	–	–	–	–	–	
(0xFD)	Reserved	–	–	–	–	–	–	–	–	
(0xFC)	Reserved	–	–	–	–	–	–	–	–	
(0xFB)	Reserved	–	–	–	–	–	–	–	–	
(0xFA)	Reserved	–	–	–	–	–	–	–	–	
(0xF9)	Reserved	–	–	–	–	–	–	–	–	
(0xF8)	Reserved	–	–	–	–	–	–	–	–	
(0xF7)	Reserved	–	–	–	–	–	–	–	–	
(0xF6)	Reserved	–	–	–	–	–	–	–	–	
(0xF5)	Reserved	–	–	–	–	–	–	–	–	
(0xF4)	Reserved	–	–	–	–	–	–	–	–	
(0xF3)	Reserved	–	–	–	–	–	–	–	–	
(0xF2)	Reserved	–	–	–	–	–	–	–	–	
(0xF1)	Reserved	–	–	–	–	–	–	–	–	
(0xF0)	Reserved	–	–	–	–	–	–	–	–	
(0xEF)	Reserved	–	–	–	–	–	–	–	–	
(0xEE)	Reserved	–	–	–	–	–	–	–	–	
(0xED)	Reserved	–	–	–	–	–	–	–	–	
(0xEC)	Reserved	–	–	–	–	–	–	–	–	
(0xEB)	Reserved	–	–	–	–	–	–	–	–	
(0xEA)	Reserved	–	–	–	–	–	–	–	–	
(0xE9)	Reserved	–	–	–	–	–	–	–	–	
(0xE8)	Reserved	–	–	–	–	–	–	–	–	
(0xE7)	Reserved	–	–	–	–	–	–	–	–	
(0xE6)	Reserved	–	–	–	–	–	–	–	–	
(0xE5)	Reserved	–	–	–	–	–	–	–	–	
(0xE4)	Reserved	–	–	–	–	–	–	–	–	
(0xE3)	Reserved	–	–	–	–	–	–	–	–	
(0xE2)	Reserved	–	–	–	–	–	–	–	–	
(0xE1)	Reserved	–	–	–	–	–	–	–	–	
(0xE0)	Reserved	–	–	–	–	–	–	–	–	
(0xDF)	Reserved	–	–	–	–	–	–	–	–	

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVR's, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The Atmel ATA6612C/ATA6613C is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.
 5. Only valid for Atmel ATA6612C/ATA6613C

6.4 Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBD)	TWAMR	TWAM6	TWAM5	TWAM4	TWAM3	TWAM2	TWAM1	TWAM0	–	202
(0xBC)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	200
(0xBB)	TWDR	2-wire serial interface data register								201
(0xBA)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	202
(0xB9)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	201
(0xB8)	TWBR	2-wire serial interface bit rate register								199
(0xB7)	Reserved	–	–	–	–	–	–	–	–	
(0xB6)	ASSR	–	EXCLK	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	154
(0xB5)	Reserved	–	–	–	–	–	–	–	–	
(0xB4)	OCR2B	Timer/counter2 output compare register B								151
(0xB3)	OCR2A	Timer/counter2 output compare register A								151
(0xB2)	TCNT2	Timer/counter2 (8-bit)								151
(0xB1)	TCCR2B	FOC2A	FOC2B	–	–	WGM22	CS22	CS21	CS20	150
(0xB0)	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	–	–	WGM21	WGM20	148
(0xAF)	Reserved	–	–	–	–	–	–	–	–	
(0xAE)	Reserved	–	–	–	–	–	–	–	–	
(0xAD)	Reserved	–	–	–	–	–	–	–	–	
(0xAC)	Reserved	–	–	–	–	–	–	–	–	
(0xAB)	Reserved	–	–	–	–	–	–	–	–	
(0xAA)	Reserved	–	–	–	–	–	–	–	–	
(0xA9)	Reserved	–	–	–	–	–	–	–	–	
(0xA8)	Reserved	–	–	–	–	–	–	–	–	
(0xA7)	Reserved	–	–	–	–	–	–	–	–	
(0xA6)	Reserved	–	–	–	–	–	–	–	–	
(0xA5)	Reserved	–	–	–	–	–	–	–	–	
(0xA4)	Reserved	–	–	–	–	–	–	–	–	
(0xA3)	Reserved	–	–	–	–	–	–	–	–	
(0xA2)	Reserved	–	–	–	–	–	–	–	–	
(0xA1)	Reserved	–	–	–	–	–	–	–	–	
(0xA0)	Reserved	–	–	–	–	–	–	–	–	
(0x9F)	Reserved	–	–	–	–	–	–	–	–	
(0x9E)	Reserved	–	–	–	–	–	–	–	–	
(0x9D)	Reserved	–	–	–	–	–	–	–	–	
(0x9C)	Reserved	–	–	–	–	–	–	–	–	

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
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