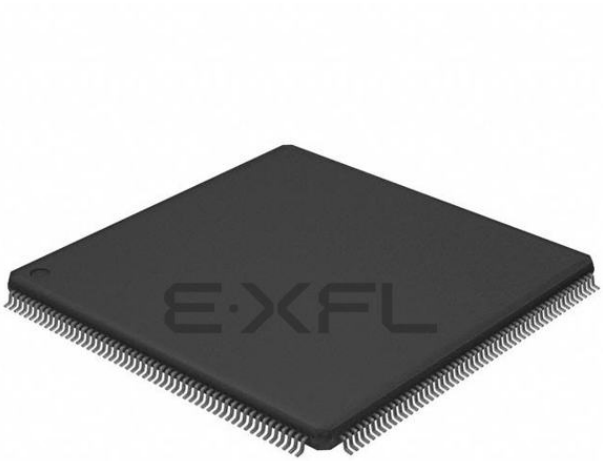


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	EBI/EMI, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	160
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	82K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2420fbd208-551

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[28]/SCL0	48[4]	R3[4]	I/O	**P0[28] —** General purpose digital input/output pin.
			I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
P0[29]/USB_D+1	61[5]	U4[5]	I/O	**P0[29] —** General purpose digital input/output pin.
			I/O	**USB_D+1 —** USB port 1 bidirectional D+ line.
P0[30]/USB_D−1	62[5]	R6[5]	I/O	**P0[30] —** General purpose digital input/output pin.
			I/O	**USB_D−1 —** USB port 1 bidirectional D− line.
P0[31]/USB_D+2	51[5]	T2[5]	I/O	**P0[31] —** General purpose digital input/output pin.
			I/O	**USB_D+2 —** USB port 2 bidirectional D+ line.
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect block.
P1[0]/ ENET_TXD0	196[1]	A3[1]	I/O	**P1[0] —** General purpose digital input/output pin.
			O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface) (LPC2460 only).
P1[1]/ ENET_TXD1	194[1]	B5[1]	I/O	**P1[1] —** General purpose digital input/output pin.
			O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface) (LPC2460 only).
P1[2]/ ENET_TXD2/ MCICLK/ PWM0[1]	185[1]	D9[1]	I/O	**P1[2] —** General purpose digital input/output pin.
			O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface) (LPC2460 only).
			O	**MCICLK —** Clock output line for SD/MMC interface.
			O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
P1[3]/ ENET_TXD3/ MCICMD/ PWM0[2]	177[1]	A10[1]	I/O	**P1[3] —** General purpose digital input/output pin.
			O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface) (LPC2460 only).
			I/O	**MCICMD —** Command line for SD/MMC interface.
			O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
P1[4]/ ENET_TX_EN	192[1]	A5[1]	I/O	**P1[4] —** General purpose digital input/output pin.
			O	**ENET_TX_EN —** Ethernet transmit data enable (RMII/MII interface) (LPC2460 only).
P1[5]/ ENET_TX_ER/ MCIPWR/ PWM0[3]	156[1]	A17[1]	I/O	**P1[5] —** General purpose digital input/output pin.
			O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface) (LPC2460 only).
			O	**MCIPWR —** Power Supply Enable for external SD/MMC power supply.
			O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
P1[6]/ ENET_TX_CLK/ MCIDAT0/ PWM0[4]	171[1]	B11[1]	I/O	**P1[6] —** General purpose digital input/output pin.
			I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface) (LPC2460 only).
			I/O	**MCIDAT0 —** Data line 0 for SD/MMC interface.
			O	**PWM0[4] —** Pulse Width Modulator 0, output 4.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[7]/ ENET_COL/ MCIDAT1/ PWM0[5]	153[1]	D14[1]	I/O	**P1[7] —** General purpose digital input/output pin.
			I	**ENET_COL —** Ethernet Collision detect (MII interface) (LPC2460 only).
			I/O	**MCIDAT1 —** Data line 1 for SD/MMC interface.
			O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
P1[8]/ ENET_CRS_DV/ ENET_CRS	190[1]	C7[1]	I/O	**P1[8] —** General purpose digital input/output pin.
			I	**ENET_CRS_DV/ENET_CRS —** Ethernet Carrier Sense/Data Valid (RMII interface)/ Ethernet Carrier Sense (MII interface) (LPC2460 only).
P1[9]/ ENET_RXD0	188[1]	A6[1]	I/O	**P1[9] —** General purpose digital input/output pin.
			I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface) (LPC2460 only).
P1[10]/ ENET_RXD1	186[1]	C8[1]	I/O	**P1[10] —** General purpose digital input/output pin.
			I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface) (LPC2460 only).
P1[11]/ ENET_RXD2/ MCIDAT2/ PWM0[6]	163[1]	A14[1]	I/O	**P1[11] —** General purpose digital input/output pin.
			I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface) (LPC2460 only).
			I/O	**MCIDAT2 —** Data line 2 for SD/MMC interface.
			O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]/ ENET_RXD3/ MCIDAT3/ PCAP0[0]	157[1]	A16[1]	I/O	**P1[12] —** General purpose digital input/output pin.
			I	**ENET_RXD3 —** Ethernet Receive Data (MII interface) (LPC2460 only).
			I/O	**MCIDAT3 —** Data line 3 for SD/MMC interface.
			I	**PCAP0[0] —** Capture input for PWM0, channel 0.
P1[13]/ ENET_RX_DV	147[1]	D16[1]	I/O	**P1[13] —** General purpose digital input/output pin.
			I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface) (LPC2460 only).
P1[14]/ ENET_RX_ER	184[1]	A7[1]	I/O	**P1[14] —** General purpose digital input/output pin.
			I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface) (LPC2460 only).
P1[15]/ ENET_REF_CLK/ ENET_RX_CLK	182[1]	A8[1]	I/O	**P1[15] —** General purpose digital input/output pin.
			I	**ENET_REF_CLK/ENET_RX_CLK —** Ethernet Reference Clock (RMII interface)/ Ethernet Receive Clock (MII interface) (LPC2460 only).
P1[16]/ ENET_MDC	180[1]	D10[1]	I/O	**P1[16] —** General purpose digital input/output pin.
			O	**ENET_MDC —** Ethernet MIIM clock (LPC2460 only).
P1[17]/ ENET_MDIO	178[1]	A9[1]	I/O	**P1[17] —** General purpose digital input/output pin.
			I/O	**ENET_MDIO —** Ethernet MIIM data input and output (LPC2460 only).

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P3[31]/D31/ MAT1[2]	25[1]	J3[1]	I/O	**P3[31] —** General purpose digital input/output pin.
			I/O	**D31 —** External memory data line 31.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P4[0] to P4[31]			I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the Pin Connect block.
P4[0]/A0	75[1]	U9[1]	I/O	**P4[0] —**]General purpose digital input/output pin.
			I/O	**A0 —** External memory address line 0.
P4[1]/A1	79[1]	U10[1]	I/O	**P4[1] —** General purpose digital input/output pin.
			I/O	**A1 —** External memory address line 1.
P4[2]/A2	83[1]	T11[1]	I/O	**P4[2] —** General purpose digital input/output pin.
			I/O	**A2 —** External memory address line 2.
P4[3]/A3	97[1]	U16[1]	I/O	**P4[3] —** General purpose digital input/output pin.
			I/O	**A3 —** External memory address line 3.
P4[4]/A4	103[1]	R15[1]	I/O	**P4[4] —** General purpose digital input/output pin.
			I/O	**A4 —** External memory address line 4.
P4[5]/A5	107[1]	R16[1]	I/O	**P4[5] —** General purpose digital input/output pin.
			I/O	**A5 —** External memory address line 5.
P4[6]/A6	113[1]	M14[1]	I/O	**P4[6] —** General purpose digital input/output pin.
			I/O	**A6 —** External memory address line 6.
P4[7]/A7	121[1]	L16[1]	I/O	**P4[7] —** General purpose digital input/output pin.
			I/O	**A7 —** External memory address line 7.
P4[8]/A8	127[1]	J17[1]	I/O	**P4[8] —** General purpose digital input/output pin.
			I/O	**A8 —** External memory address line 8.
P4[9]/A9	131[1]	H17[1]	I/O	**P4[9] —** General purpose digital input/output pin.
			I/O	**A9 —** External memory address line 9.
P4[10]/A10	135[1]	G17[1]	I/O	**P4[10] —** General purpose digital input/output pin.
			I/O	**A10 —** External memory address line 10.
P4[11]/A11	145[1]	F14[1]	I/O	**P4[11] —** General purpose digital input/output pin.
			I/O	**A11 —** External memory address line 11.
P4[12]/A12	149[1]	C16[1]	I/O	**P4[12] —** General purpose digital input/output pin.
			I/O	**A12 —** External memory address line 12.
P4[13]/A13	155[1]	B16[1]	I/O	**P4[13] —** General purpose digital input/output pin.
			I/O	**A13 —** External memory address line 13.
P4[14]/A14	159[1]	B15[1]	I/O	**P4[14] —** General purpose digital input/output pin.
			I/O	**A14 —** External memory address line 14.
P4[15]/A15	173[1]	A11[1]	I/O	**P4[15] —** General purpose digital input/output pin.
			I/O	**A15 —** External memory address line 15.
P4[16]/A16	101[1]	U17[1]	I/O	**P4[16] —** General purpose digital input/output pin.
			I/O	**A16 —** External memory address line 16.

7. Functional description

7.1 Architectural overview

The LPC2420/2460 microcontroller consists of an ARM7TDMI-S CPU with emulation support, the ARM7 local bus for closely coupled, high-speed access to the majority of on-chip memory, the AMBA AHB interfacing to high-speed on-chip peripherals and external memory, and the AMBA APB for connection to other on-chip peripheral functions. The microcontroller permanently configures the ARM7TDMI-S processor for little-endian byte order.

The LPC2460 only implements two AHB in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the VIC, GPDMA controller, and EMC.

The second AHB (LPC2460 only), referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

AHB peripherals are allocated a 2 MB range of addresses at the very top of the 4 GB ARM memory space. Each AHB peripheral is allocated a 16 kB address space within the AHB address space. Lower speed peripheral functions are connected to the APB. The AHB to APB bridge interfaces the APB to the AHB. APB peripherals are also allocated a 2 MB range of addresses, beginning at the 3.5 GB address point. Each APB peripheral is allocated a 16 kB address space within the APB address space.

The ARM7TDMI-S processor is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed complex instruction set computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- the standard 32-bit ARM set
- a 16-bit Thumb set

- One AHB master for transferring data. This interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data. Usually the burst size is set to half the size of the FIFO in the peripheral.
- Internal four-word FIFO per channel.
- Supports 8-bit, 16-bit, and 32-bit wide transactions.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Interrupt masking. The DMA error and DMA terminal count interrupt requests can be masked.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC2420/2460 use accelerated GPIO functions:

- GPIO registers are relocated to the ARM local bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.

Additionally, any pin on port 0 and port 2 (total of 64 pins) that is not configured as an analog input/output can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake the chip up from Power-down mode.

7.8.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Backward compatibility with other earlier devices is maintained with legacy port 0 and port 1 registers appearing at the original addresses on the APB.

7.9 Ethernet (LPC2460 only)

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share a dedicated AHB subsystem that is used to access the Ethernet SRAM for Ethernet data, control, and status information. All other AHB traffic in the LPC2420/2460 takes place on a different AHB subsystem, effectively separating Ethernet activity from the rest of the system. The Ethernet DMA can also access off-chip memory via the EMC, as well as the SRAM located on another AHB. However, using memory other than the Ethernet SRAM, especially off-chip memory, will slow Ethernet access to memory and increase the loading of its AHB.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.9.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.

7.10.2.1 Features

- OHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

7.10.3 USB OTG controller

USB OTG is a supplement to the *USB 2.0 specification* that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG controller integrates the host controller, device controller, and a master-only I^2C-bus interface to implement OTG dual-role device functionality. The dedicated I^2C-bus interface controls an external OTG transceiver.

7.10.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

7.11 CAN controller and acceptance filters (LPC2460 only)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.11.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.

- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

7.12 10-bit ADC

The LPC2420/2460 contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.12.1 Features

- 10-bit successive approximation ADC
- Input multiplexing among 8 pins
- Power-down mode
- Measurement range 0 V to $V_{i(VREF)}$
- 10-bit conversion time $\geq$ 2.44 μs
- Burst conversion mode for single or multiple inputs
- Optional conversion on transition of input pin or Timer Match signal
- Individual result registers for each ADC channel to reduce interrupt overhead

7.13 10-bit DAC

The DAC allows the LPC2420/2460 to generate a variable analog output. The maximum output value of the DAC is $V_{i(VREF)}$.

7.13.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive

7.14 UARTs

The LPC2420/2460 contains four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.14.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.

The VBAT pin supplies power only to the RTC and the Battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that can be used by external hardware to restore chip power and resume operation.

7.23.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- An alarm output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC and Battery RAM.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values. This enhancement enables the RTC to be used as a System Timer.
- 2 kB data SRAM powered by VBAT.
- RTC and Battery RAM power supply is isolated from the rest of the chip.

7.24 Clocking and power control

7.24.1 Crystal oscillators

The LPC2420/2460 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2420/2460 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.24.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy.

Upon power-up or any chip reset, the LPC2420/2460 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.24.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The

7.24.4.4 Deep power-down mode

Deep power-down mode is similar to the Power-down mode, but now the on-chip regulator that supplies power to the internal logic is also shut off. This produces the lowest possible power consumption without removing power from the entire chip. Since the Deep power-down mode shuts down the on-chip logic power supply, there is no register or memory retention, and resumption of operation involves the same activities as a full chip reset.

If power is supplied to the LPC2420/2460 during Deep power-down mode, wake-up can be caused by the RTC Alarm interrupt or by external Reset.

While in Deep power-down mode, external device power may be removed. In this case, the LPC2420/2460 will start up when external power is restored.

Essential data may be retained through Deep power-down mode (or through complete powering off of the chip) by storing data in the Battery RAM, as long as the external power to the VBAT pin is maintained.

7.24.4.5 Power domains

The LPC2420/2460 provides two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the Battery RAM.

On the LPC2420/2460, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(DCDC)(3V3)}$ pins power the on-chip DC-to-DC converter which in turn provides power to the CPU and most of the peripherals.

Although both the I/O pad ring and the core require a 3.3 V supply, different powering schemes can be used depending on the actual application requirements.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(DCDC)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(DCDC)(3V3)}$). Having the on-chip DC-DC converter powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC and the Battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that may be used by external hardware to restore chip power and resume operation.

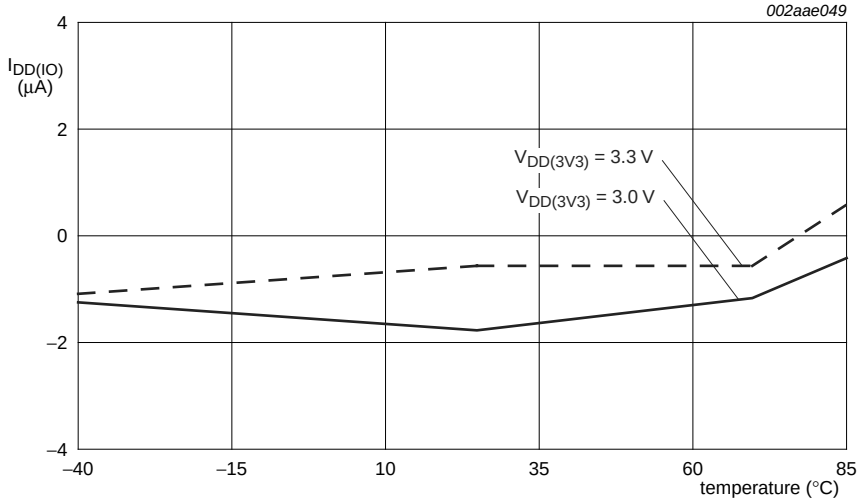
10. Static characteristics

Table 9. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

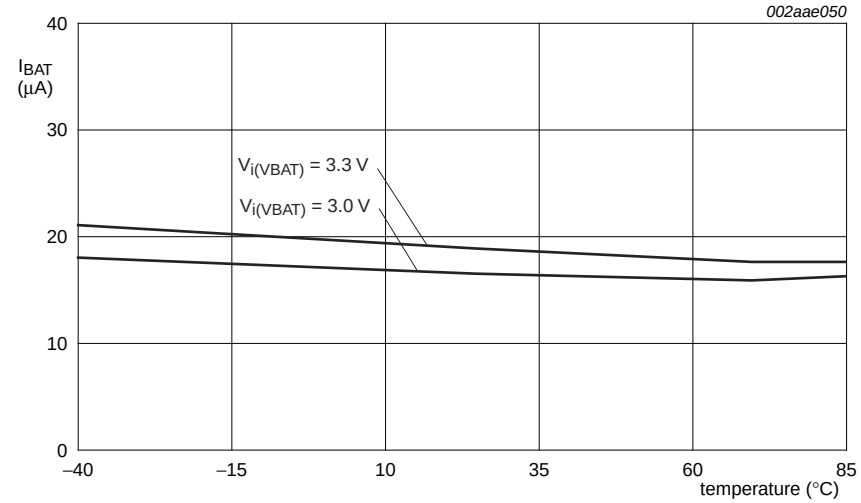
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	core and external rail		3.0	3.3	3.6	V
$V_{DD(DCDC)(3V3)}$	DC-to-DC converter supply voltage (3.3 V)			3.0	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			3.0	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[2]	2.0	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF			2.5	3.3	V_{DDA}	V
$I_{DD(DCDC)act(3V3)}$	active mode DC-to-DC converter supply current (3.3 V)	$V_{DD(DCDC)(3V3)}$ = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from the on-chip SRAM; no peripherals enabled; PCLK = CCLK / 8					
		CCLK = 12 MHz		-	17.4	-	mA
		CCLK = 72 MHz		-	66.1	-	mA
$I_{DD(DCDC)pd(3V3)}$	Power-down mode DC-to-DC converter supply current (3.3 V)		[3]	-	113	-	µA
$I_{DD(DCDC)dpd(3V3)}$	Deep power-down mode DC-to-DC converter supply current (3.3 V)		[3]	-	20	-	µA
I_{BATact}	active mode battery supply current		[4]	-	20	-	µA
I_{BAT}	battery supply current	Deep power-down mode	[3]	-	20	-	µA
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[5][6][7][8]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V

10.1 Power-down mode



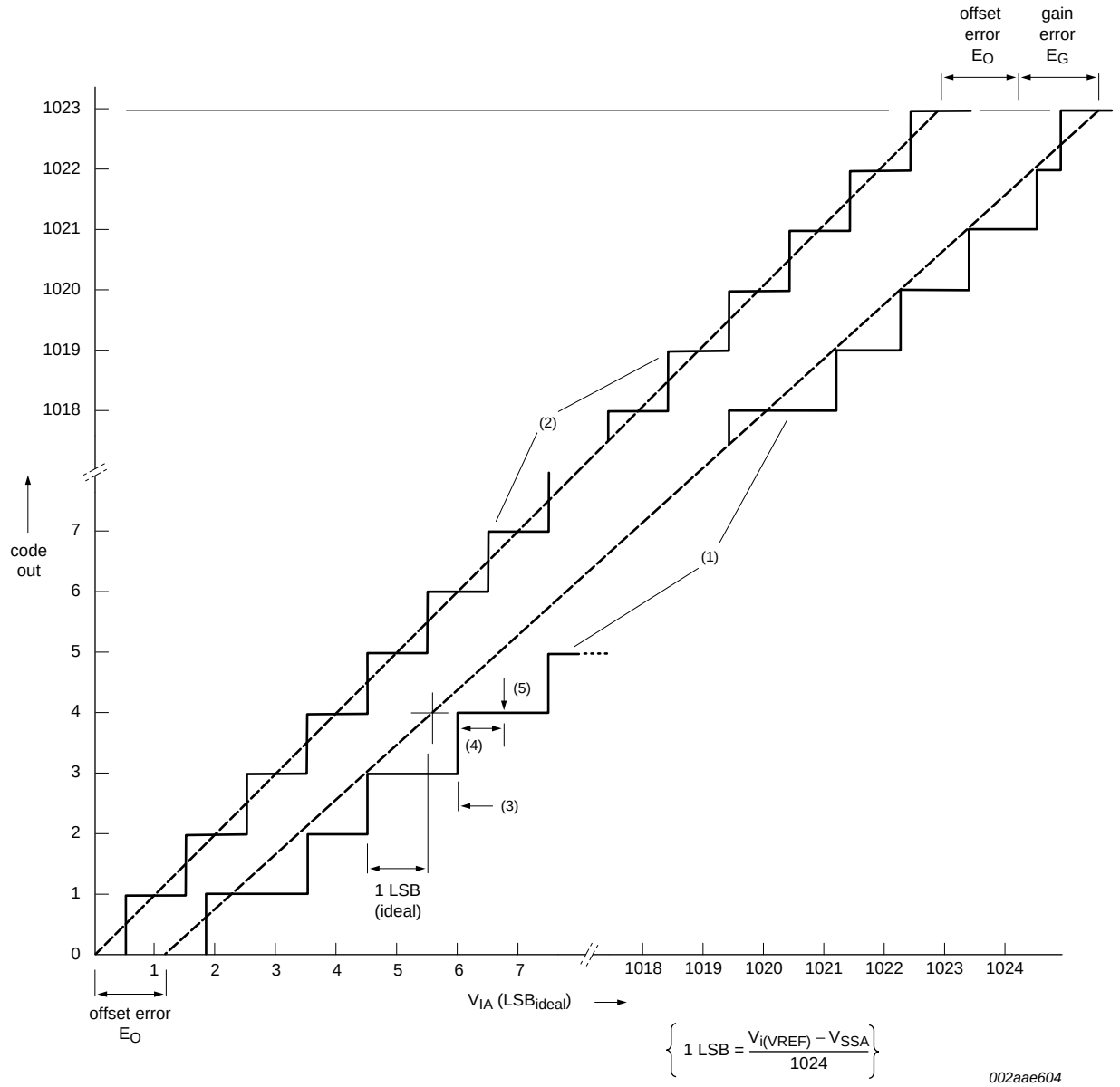
$V_{i(VBAT)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 5. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 6. RTC battery maximum supply current I_{BAT} versus temperature in Power-down mode



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 19. ADC characteristics

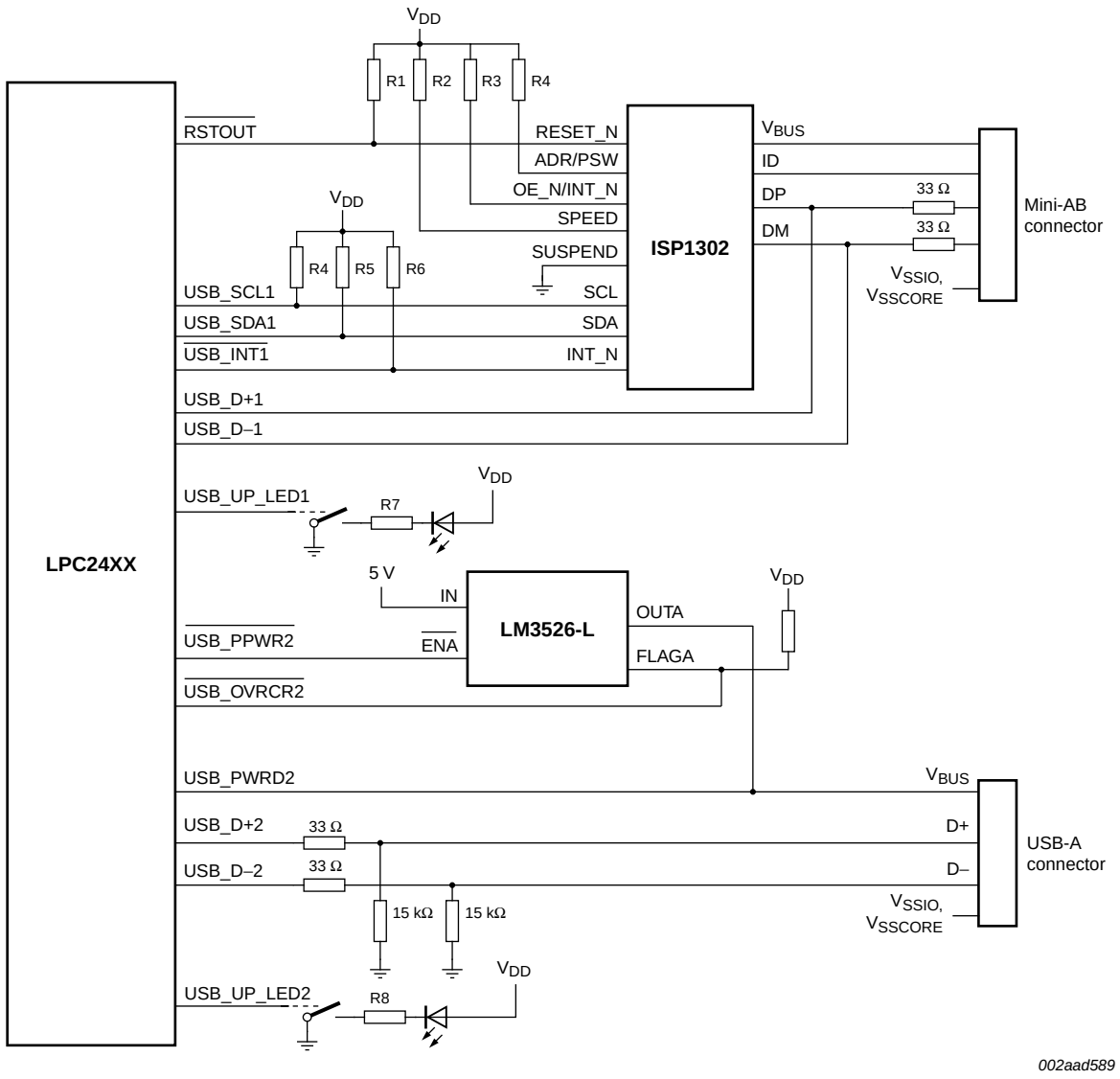


Fig 25. LPC2420/2460 USB OTG port configuration: USB port 1 OTG dual-role device, USB port 2 host

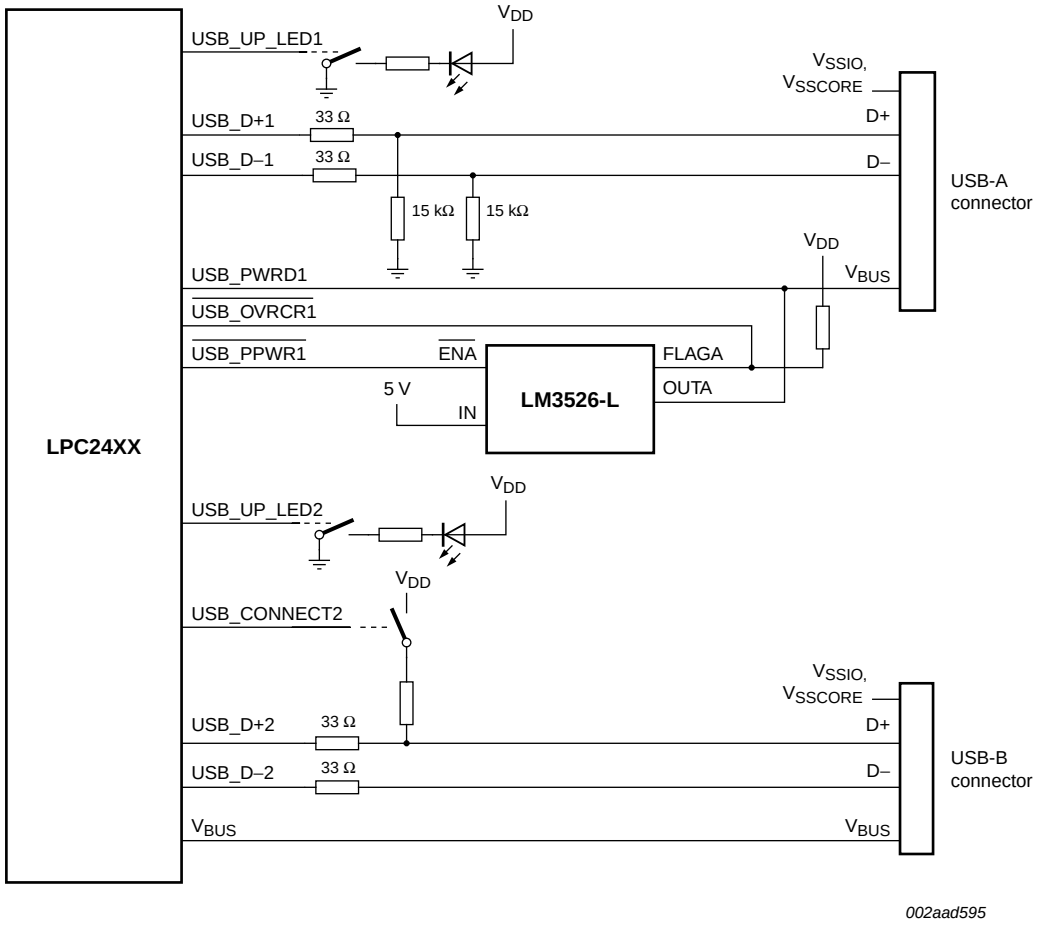


Fig 27. LPC2420/2460 USB OTG port configuration: USB port 2 device, USB port 1 host

Table 20. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.4 RTC 32 kHz oscillator component selection

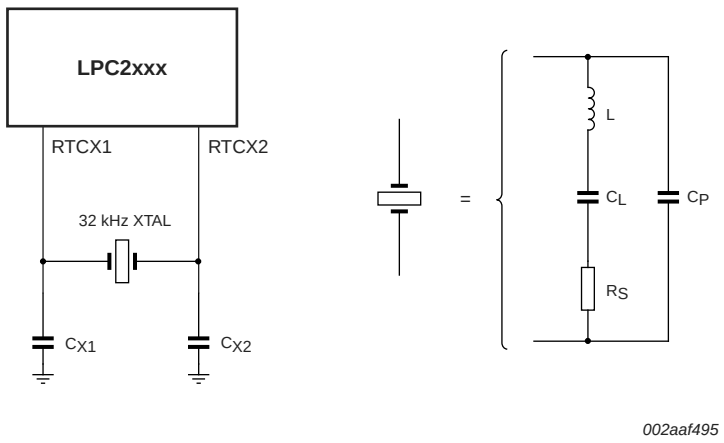


Fig 31. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 31. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 21 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 21 that belong to a specific C_L. The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L. Parasitics from PCB and package are not taken into account.

Table 21. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 kΩ	18 pF, 18 pF
13 pF	< 100 kΩ	22 pF, 22 pF
15 pF	< 100 kΩ	27 pF, 27 pF

17. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2420_60 v.6.2	20131016	Product data sheet	-	LPC2420_60 v.6.1
Modifications:	• Table 2 “Ordering options”: Corrected options for LPC2420FET208. • Table 4 “Pin description”, Table note 6: Changed glitch filter spec from 5 ns to 10 ns. • Table 10 “Dynamic characteristics”: Changed min clock cycle time from 42 to 40. • Table 16 “Dynamic characteristics: Dynamic external memory interface”: Updated $t_{d(QV)}$ typ and max.			
LPC2420_60 v.6.1	20110922	Product data sheet	-	LPC2420_60 v.6
Modifications:	• Table 14 “Dynamic characteristics: Static external memory interface”: Removed text "EMC Dynamic Read Config Register = 0x0 (RD = 00)".			

Table 23. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2420_60 v.6	20110823	Product data sheet	-	LPC2420_60 v.5
Modifications:	• Table 4 “Pin description”: Updated description for USB_UP_LED1 and USB_UP_LED2. • Table 4 “Pin description”: Added Table note 8 for DBGEN, TMS, TDI, $\overline{\text{TRST}}$, and RTCK pins. • Table 4 “Pin description”: Added Table note 9 for TCK and TDO pins. • Table 4 “Pin description”: Added Table note 11 for XTAL1 and XTAL2 pins. • Table 4 “Pin description”: Added Table note 12 for RTCX1 and RTCX2 pins. • Table 6 “Limiting values”: Added “non-operating” to conditions of storage spec. • Table 6 “Limiting values”: Updated Table note [5]. • Added Table 8 “Thermal resistance value (C/W): ±15 %”. • Table 9 “Static characteristics”: Removed R_{pu}. • Table 9 “Static characteristics”: Changed V_{hys} Typ value of I^2C-bus pins to $0.05V_{DD(3V3)}$. • Added Table 11 “Dynamic characteristic: internal oscillators”. • Added Table 12 “Dynamic characteristic: I/O pins[1]”. • Table 14 “Dynamic characteristics: Static external memory interface”: Updated min, typical and max values for $t_{h(D)}$. • Table 14 “Dynamic characteristics: Static external memory interface”: Updated min, typical and max values for t_{WEHDNV}. • Table 14 “Dynamic characteristics: Static external memory interface”: Removed “AHB clock = 1 MHz”. • Table 14 “Dynamic characteristics: Static external memory interface”: Swapped current min and max values for t_{am}. • Table 15 “Dynamic characteristics: Dynamic external memory interface”: Added Table note 1. • Table 15 “Dynamic characteristics: Dynamic external memory interface”: Removed “AHB clock = 1 MHz”. • Added Table 16 “Dynamic characteristics: Dynamic external memory interface”. • Added Section 10.3 “Electrical pin characteristics”. • Added Section 14.3 “Crystal oscillator XTAL input and component selection”. • Added Section 14.4 “RTC 32 kHz oscillator component selection”. • Updated Section 14.5 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Added Section 14.6 “Standard I/O pin configuration” • Added Section 14.7 “Reset pin configuration” • Moved Figure 13 “External clock timing (with an amplitude of at least Vi(RMS) = 200 mV)” to below Table 10 “Dynamic characteristics”. • Updated Figure 19 “ADC characteristics”.			
LPC2420_60 v.5	20100224	Preliminary data sheet	-	LPC2420_60 v.4
Modifications:	• Table 9: Merged power-down mode information into one table. • Table 9: Changed typical values from 19 to 20 for $I_{DD(DCDC)dpd(3V3)}$, I_{BATact}, and I_{BAT}. • Added Table 16 “Dynamic characteristics: Dynamic external memory interface”. • Added Table 18 “DAC electrical characteristics”.			
LPC2420_60 v.4	20091015	Preliminary data sheet	-	LPC2420_60 v.3

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**