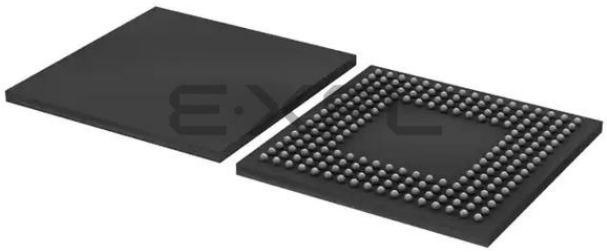

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Program Memory Type	ROMless
EEPROM Size	-
RAM Size	82K x 8
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Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	P2[17]/$\overline{\text{RAS}}$	14	P0[11]/RXD2/SCL2/ MAT3[1]	15	P4[4]/A4	16	P4[5]/A5
17	P4[20]/A20/ SDA2/SCK1		-		-		-
Row T							
1	P0[27]/SDA0	2	P0[31]/USB_D+2	3	P3[26]/D26/ MAT0[1]/PWM1[3]	4	P2[26]/CKEOUT2/ MAT3[0]/MISO0
5	V_{SSIO}	6	P3[23]/D23/ CAP0[0]/PCAP1[0]	7	P0[14]/$\overline{\text{USB\_HSTEN2}}$/ USB_CONNECT2/ SSEL1	8	P2[20]/$\overline{\text{DYCS0}}$
9	P1[24]/USB_RX_DM1/ PWM1[5]/MOSI0	10	P1[25]/$\overline{\text{USB\_LS1}}$/ USB_HSTEN1/MAT1[1]	11	P4[2]/A2	12	P1[27]/$\overline{\text{USB\_INT1}}$/ USB_OVRCR1/CAP0[1]
13	P1[28]/USB_SCL1/ PCAP1[0]/MAT0[0]	14	P0[1]/TD1/RXD3/SCL1	15	P0[10]/TXD2/SDA2/ MAT3[0]	16	P2[13]/$\overline{\text{EINT3}}$/ MCIDAT3/I2STX_SDA
17	P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/I2STX_CLK		-		-		-
Row U							
1	USB_D−2	2	P3[25]/D25/ MAT0[0]/PWM1[2]	3	P2[18]/CLKOUT0	4	P0[29]/USB_D+1
5	P2[23]/$\overline{\text{DYCS3}}$/ CAP3[1]/SSEL0	6	P1[19]/$\overline{\text{USB\_TX\_E1}}$/ USB_PPWR1/CAP1[1]	7	P1[20]/USB_TX_DP1/ PWM1[2]/SCK0	8	P1[22]/USB_RCV1/ USB_PWRD1/MAT1[0]
9	P4[0]/A0	10	P4[1]/A1	11	P2[21]/$\overline{\text{DYCS1}}$	12	P2[22]/$\overline{\text{DYCS2}}$/ CAP3[0]/SCK0
13	$V_{DD(3V3)}$	14	P1[29]/USB_SDA1/ PCAP1[1]/MAT0[1]	15	P0[0]/RD1/TXD3/SDA1	16	P4[3]/A3
17	P4[16]/A16		-		-		-

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Ball	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect block.
P0[0]/RD1/ TXD3/SDA1	94[1]	U15[1]	I/O	**P0[0] —** General purpose digital input/output pin.
			I	**RD1 —** CAN1 receiver input (LPC2460 only).
			O	**TXD3 —** Transmitter output for UART3.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[1]/TD1/RXD3/ SCL1	96[1]	T14[1]	I/O	**P0[1] —** General purpose digital input/output pin.
			O	**TD1 —** CAN1 transmitter output (LPC2460 only).
			I	**RXD3 —** Receiver input for UART3.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[2]/TXD0	202[1]	C4[1]	I/O	**P0[2] —** General purpose digital input/output pin.
			O	**TXD0 —** Transmitter output for UART0.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[26]/ USB_SSPND1/ PWM1[6]/ CAP0[0]	82[1]	R10[1]	I/O	**P1[26] —** General purpose digital input/output pin.
			O	**USB_SSPND1 —** USB port 1 Bus Suspend status (OTG transceiver).
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/ USB_INT1/ USB_OVRCR1/ CAP0[1]	88[1]	T12[1]	I/O	**P1[27] —** General purpose digital input/output pin.
			I	**USB_INT1 —** USB port 1 OTG transceiver interrupt (OTG transceiver).
			I	**USB_OVRCR1 —** USB port 1 Over-Current status.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/ USB_SCL1/ PCAP1[0]/ MAT0[0]	90[1]	T13[1]	I/O	**P1[28] —** General purpose digital input/output pin.
			I/O	**USB_SCL1 —** USB port 1 I^2C-bus serial clock (OTG transceiver).
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/ USB_SDA1/ PCAP1[1]/ MAT0[1]	92[1]	U14[1]	I/O	**P1[29] —** General purpose digital input/output pin.
			I/O	**USB_SDA1 —** USB port 1 I^2C-bus serial data (OTG transceiver).
			I	**PCAP1[1] —** Capture input for PWM1, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 0.
P1[30]/ USB_PWRD2/ V_{BUS}/AD0[4]	42[2]	P2[2]	I/O	**P1[30] —** General purpose digital input/output pin.
			I	**USB_PWRD2 —** Power Status for USB port 2.
			I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/ USB_OVRCR2/ SCK1/AD0[5]	40[2]	P1[2]	I/O	**P1[31] —** General purpose digital input/output pin.
			I	**USB_OVRCR2 —** Over-Current status for USB port 2.
			I/O	**SCK1 —** Serial Clock for SSP1.
			I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]			I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect block.
P2[0]/PWM1[1]/ TXD1/ TRACECLK	154[1]	B17[1]	I/O	**P2[0] —** General purpose digital input/output pin.
			O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
			O	**TXD1 —** Transmitter output for UART1.
			O	**TRACECLK —** Trace Clock.
P2[1]/PWM1[2]/ RXD1/ PIPESTAT0	152[1]	E14[1]	I/O	**P2[1] —** General purpose digital input/output pin.
			O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
			I	**RXD1 —** Receiver input for UART1.
			O	**PIPESTAT0 —** Pipeline Status, bit 0.
P2[2]/PWM1[3]/ CTS1/ PIPESTAT1	150[1]	D15[1]	I/O	**P2[2] —** General purpose digital input/output pin.
			O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
			I	**CTS1 —** Clear to Send input for UART1.
			O	**PIPESTAT1 —** Pipeline Status, bit 1.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P3[21]/D21/ PWM0[6]/DTR1	175[1]	C10[1]	I/O	**P3[21] —** General purpose digital input/output pin.
			I/O	**D21 —** External memory data line 21.
			O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
			O	**DTR1 —** Data Terminal Ready output for UART1.
P3[22]/D22/ PCAP0[0]/RI1	195[1]	C6[1]	I/O	**P3[22] —** General purpose digital input/output pin.
			I/O	**D22 —** External memory data line 22.
			I	**PCAP0[0] —** Capture input for PWM0, channel 0.
			I	**RI1 —** Ring Indicator input for UART1.
P3[23]/D23/ CAP0[0]/ PCAP1[0]	65[1]	T6[1]	I/O	**P3[23] —** General purpose digital input/output pin.
			I/O	**D23 —** External memory data line 23.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
P3[24]/D24/ CAP0[1]/ PWM1[1]	58[1]	R5[1]	I/O	**P3[24] —** General purpose digital input/output pin.
			I/O	**D24 —** External memory data line 24.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
			O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
P3[25]/D25/ MAT0[0]/ PWM1[2]	56[1]	U2[1]	I/O	**P3[25] —** General purpose digital input/output pin.
			I/O	**D25 —** External memory data line 25.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
			O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
P3[26]/D26/ MAT0[1]/ PWM1[3]	55[1]	T3[1]	I/O	**P3[26] —** General purpose digital input/output pin.
			I/O	**D26 —** External memory data line 26.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
			O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
P3[27]/D27/ CAP1[0]/ PWM1[4]	203[1]	A1[1]	I/O	**P3[27] —** General purpose digital input/output pin.
			I/O	**D27 —** External memory data line 27.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
			O	**PWM1[4] —** Pulse Width Modulator 1, output 4.
P3[28]/D28/ CAP1[1]/ PWM1[5]	5[1]	D2[1]	I/O	**P3[28] —** General purpose digital input/output pin.
			I/O	**D28 —** External memory data line 28.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.
			O	**PWM1[5] —** Pulse Width Modulator 1, output 5.
P3[29]/D29/ MAT1[0]/ PWM1[6]	11[1]	F3[1]	I/O	**P3[29] —** General purpose digital input/output pin.
			I/O	**D29 —** External memory data line 29.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
			O	**PWM1[6] —** Pulse Width Modulator 1, output 6.
P3[30]/D30/ MAT1[1]/ RTS1	19[1]	H3[1]	I/O	**P3[30] —** General purpose digital input/output pin.
			I/O	**D30 —** External memory data line 30.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
			O	**RTS1 —** Request to Send output for UART1.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P3[31]/D31/ MAT1[2]	25[1]	J3[1]	I/O	**P3[31] —** General purpose digital input/output pin.
			I/O	**D31 —** External memory data line 31.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P4[0] to P4[31]			I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the Pin Connect block.
P4[0]/A0	75[1]	U9[1]	I/O	**P4[0] —**]General purpose digital input/output pin.
			I/O	**A0 —** External memory address line 0.
P4[1]/A1	79[1]	U10[1]	I/O	**P4[1] —** General purpose digital input/output pin.
			I/O	**A1 —** External memory address line 1.
P4[2]/A2	83[1]	T11[1]	I/O	**P4[2] —** General purpose digital input/output pin.
			I/O	**A2 —** External memory address line 2.
P4[3]/A3	97[1]	U16[1]	I/O	**P4[3] —** General purpose digital input/output pin.
			I/O	**A3 —** External memory address line 3.
P4[4]/A4	103[1]	R15[1]	I/O	**P4[4] —** General purpose digital input/output pin.
			I/O	**A4 —** External memory address line 4.
P4[5]/A5	107[1]	R16[1]	I/O	**P4[5] —** General purpose digital input/output pin.
			I/O	**A5 —** External memory address line 5.
P4[6]/A6	113[1]	M14[1]	I/O	**P4[6] —** General purpose digital input/output pin.
			I/O	**A6 —** External memory address line 6.
P4[7]/A7	121[1]	L16[1]	I/O	**P4[7] —** General purpose digital input/output pin.
			I/O	**A7 —** External memory address line 7.
P4[8]/A8	127[1]	J17[1]	I/O	**P4[8] —** General purpose digital input/output pin.
			I/O	**A8 —** External memory address line 8.
P4[9]/A9	131[1]	H17[1]	I/O	**P4[9] —** General purpose digital input/output pin.
			I/O	**A9 —** External memory address line 9.
P4[10]/A10	135[1]	G17[1]	I/O	**P4[10] —** General purpose digital input/output pin.
			I/O	**A10 —** External memory address line 10.
P4[11]/A11	145[1]	F14[1]	I/O	**P4[11] —** General purpose digital input/output pin.
			I/O	**A11 —** External memory address line 11.
P4[12]/A12	149[1]	C16[1]	I/O	**P4[12] —** General purpose digital input/output pin.
			I/O	**A12 —** External memory address line 12.
P4[13]/A13	155[1]	B16[1]	I/O	**P4[13] —** General purpose digital input/output pin.
			I/O	**A13 —** External memory address line 13.
P4[14]/A14	159[1]	B15[1]	I/O	**P4[14] —** General purpose digital input/output pin.
			I/O	**A14 —** External memory address line 14.
P4[15]/A15	173[1]	A11[1]	I/O	**P4[15] —** General purpose digital input/output pin.
			I/O	**A15 —** External memory address line 15.
P4[16]/A16	101[1]	U17[1]	I/O	**P4[16] —** General purpose digital input/output pin.
			I/O	**A16 —** External memory address line 16.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P4[31]/$\overline{CS1}$	193[1]	A4[1]	I/O	**P4[31] —** General purpose digital input/output pin.
			O	**$\overline{CS1}$ —** LOW active Chip Select 1 signal.
ALARM	37[7]	N1[7]	O	**ALARM —** RTC controlled output. This is a 1.8 V pin. It goes HIGH when a RTC alarm is generated.
USB_D−2	52	U1	I/O	**USB_D−2 —** USB port 2 bidirectional D− line.
DBGEN	9[1][8]	F4[1][8]	I	**DBGEN —** JTAG interface control signal. Also used for boundary scanning.
TDO	2[1][9]	D3[1][9]	O	**TDO —** Test data out for JTAG interface.
TDI	4[1][8]	C2[1][8]	I	**TDI —** Test data in for JTAG interface.
TMS	6[1][8]	E3[1][8]	I	**TMS —** Test Mode Select for JTAG interface.
$\overline{TRST}$	8[1][8]	D1[1][8]	I	**$\overline{TRST}$ —** Test Reset for JTAG interface.
TCK	10[1][9]	E2[1][9]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
RTCK	206[1][8]	C3[1][8]	I/O	**RTCK —** JTAG interface control signal. **Note:** LOW on this pin while $\overline{RESET}$ is LOW enables ETM pins (P2[9:0]) to operate as Trace port after reset.
$\overline{RSTOUT}$	29	K3	O	**$\overline{RSTOUT}$ —** This is a 3.3 V pin. LOW on this pin indicates LPC2420/2460 being in Reset state.
$\overline{RESET}$	35[10]	M2[10]	I	**external reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	44[7][11]	M4[7][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	46[7][11]	N4[7][11]	O	Output from the oscillator amplifier.
RTCX1	34[7][12]	K2[7][12]	I	Input to the RTC oscillator circuit.
RTCX2	36[7][12]	L2[7][12]	O	Output from the RTC oscillator circuit.
V_{SSIO}	33, 63, 77, 93, 114, 133, 148, 169, 189, 200[7]	L3, T5, R9, P12, N16, H14, E15, A12, B6, A2[7]	I	**ground:** 0 V reference for the digital I/O pins.
V_{SSCORE}	32, 84, 172[7]	K4, P10, D12[7]	I	**ground:** 0 V reference for the core.
V_{SSA}	22[7]	J2[7]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SSIO}/V_{SSCORE}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	15, 60, 71, 89, 112, 125, 146, 165, 181, 198[7]	G3, P6, P8, U13, P17, K16, C17, B13, C9, D7[7]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
n.c.	30, 117, 141[7]	J4, L14, G14[7]	I	**not connected pins:** These pins must be left unconnected (floating).

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
$V_{DD(DCDC)(3V3)}$	26, 86, 174[7]	H4, P11, D11[7]	I	**3.3 V DC-to-DC converter supply voltage:** This is the power supply for the on-chip DC-to-DC converter.
V_{DDA}	20[7]	G4[7]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC.
VREF	24[7]	K1[7]	I	**ADC reference:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. The level on this pin is used as a reference for ADC and DAC.
VBAT	38[7]	M3[7]	I	**RTC power supply:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a ADC input, digital section of the pad is disabled.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C-bus lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[7] Pad provides special analog functionality.

[8] This pin has a built-in pull-up resistor.

[9] This pin has no built-in pull-up and no built-in pull-down resistor.

[10] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[11] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[12] If the RTC is not used, these pins can be left floating.

The Thumb set's 16-bit instruction length allows it to approach higher density compared to standard ARM code while retaining most of the ARM's performance.

7.2 On-chip SRAM

The LPC2420/2460 includes a SRAM memory of 64 kB reserved for the ARM processor exclusive use. This RAM may be used for code and/or data storage and may be accessed as 8 bits, 16 bits, and 32 bits.

A 16 kB SRAM block serving as a buffer for the Ethernet controller (LPC2460 only) and a 16 kB SRAM associated with the second AHB can be used both for data and code storage, too. The 2 kB RTC SRAM can be used for data storage only. The RTC SRAM is battery powered and retains the content in the absence of the main power supply.

7.3 Memory map

The LPC2420/2460 memory map incorporates several distinct regions as shown in Table 5 and Figure 4.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either boot ROM or SRAM (see Section 7.25.6).

Table 5. LPC2420/2460 memory usage and details

Address range	General use	Address range details and description	
0x0000 0000 to 0x3FFF FFFF	fast I/O	0x3FFF C000 to 0x3FFF FFFF	fast GPIO registers
0x4000 0000 to 0x7FFF FFFF	on-chip RAM	0x4000 0000 to 0x4000 FFFF	RAM (64 kB)
		0x7FE0 0000 to 0x7FE0 3FFF	Ethernet RAM (16 kB) (LPC2460 only)
		0x7FD0 0000 to 0x7FD0 3FFF	USB RAM (16 kB)
0x8000 0000 to 0xDFFF FFFF	off-chip memory	Four static memory banks, 16 MB each	
		0x8000 0000 to 0x80FF FFFF	static memory bank 0
		0x8100 0000 to 0x81FF FFFF	static memory bank 1
		0x8200 0000 to 0x82FF FFFF	static memory bank 2
		0x8300 0000 to 0x83FF FFFF	static memory bank 3
		Four dynamic memory banks, 256 MB each	
		0xA000 0000 to 0xAFFF FFFF	dynamic memory bank 0
		0xB000 0000 to 0xBFFF FFFF	dynamic memory bank 1
		0xC000 0000 to 0xCFFF FFFF	dynamic memory bank 2
		0xD000 0000 to 0xDFFF FFFF	dynamic memory bank 3
0xE000 0000 to 0xEFFF FFFF	APB peripherals	36 peripheral blocks, 16 kB each	
0xF000 0000 to 0xFFFF FFFF	AHB peripherals		

- One AHB master for transferring data. This interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data. Usually the burst size is set to half the size of the FIFO in the peripheral.
- Internal four-word FIFO per channel.
- Supports 8-bit, 16-bit, and 32-bit wide transactions.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Interrupt masking. The DMA error and DMA terminal count interrupt requests can be masked.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC2420/2460 use accelerated GPIO functions:

- GPIO registers are relocated to the ARM local bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.

Additionally, any pin on port 0 and port 2 (total of 64 pins) that is not configured as an analog input/output can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake the chip up from Power-down mode.

7.8.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Backward compatibility with other earlier devices is maintained with legacy port 0 and port 1 registers appearing at the original addresses on the APB.

7.10.2.1 Features

- OHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

7.10.3 USB OTG controller

USB OTG is a supplement to the *USB 2.0 specification* that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG controller integrates the host controller, device controller, and a master-only I^2C-bus interface to implement OTG dual-role device functionality. The dedicated I^2C-bus interface controls an external OTG transceiver.

7.10.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

7.11 CAN controller and acceptance filters (LPC2460 only)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.11.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.

- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- UART3 includes an IrDA mode to support infrared communication.

7.15 SPI serial I/O controller

The LPC2420/2460 contains one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

7.15.1 Features

- Compliant with SPI specification
- Synchronous, Serial, Full Duplex Communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.16 SSP serial I/O controller

The LPC2420/2460 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.16.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of one half (Master mode) and one twelfth (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.17 SD/MMC card interface

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

7.22 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

7.22.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

7.23 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in Power-down and Deep power-down modes. On the LPC2420/2460, the RTC can be clocked by a separate 32.768 kHz oscillator or by a programmable prescale divider based on the APB clock. Also, the RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

The VBAT pin supplies power only to the RTC and the Battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that can be used by external hardware to restore chip power and resume operation.

7.23.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- An alarm output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC and Battery RAM.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values. This enhancement enables the RTC to be used as a System Timer.
- 2 kB data SRAM powered by VBAT.
- RTC and Battery RAM power supply is isolated from the rest of the chip.

7.24 Clocking and power control

7.24.1 Crystal oscillators

The LPC2420/2460 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2420/2460 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.24.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy.

Upon power-up or any chip reset, the LPC2420/2460 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.24.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The

7.25.4 AHB

The LPC2460 implements two AHB in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, is implemented on LPC2420 as well and includes the Vectored Interrupt Controller, GPDMA controller, USB interface, and 16 kB SRAM.

The second AHB, referred to as AHB2, is implemented on LPC2460 only and includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the USB block, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

7.25.5 External interrupt inputs

The LPC2420/2460 includes up to 68 edge sensitive interrupt inputs combined with up to four level sensitive external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

7.25.6 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear at the beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the Boot ROM, the SRAM, or external memory. This allows code running in different memory spaces to have control of the interrupts.

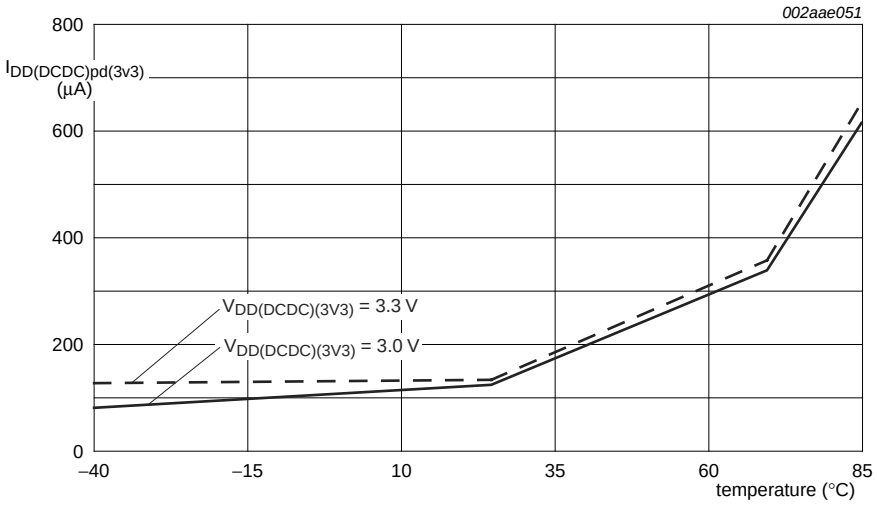
7.26 Emulation and debugging

The LPC2420/2460 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on P2[0] to P2[9]. This means that all communication, timer, and interface peripherals residing on other pins are available during the development and debugging phase as they are when the application is run in the embedded system itself.

7.26.1 EmbeddedICE

The EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. The EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM7TDMI-S core present on the target system.

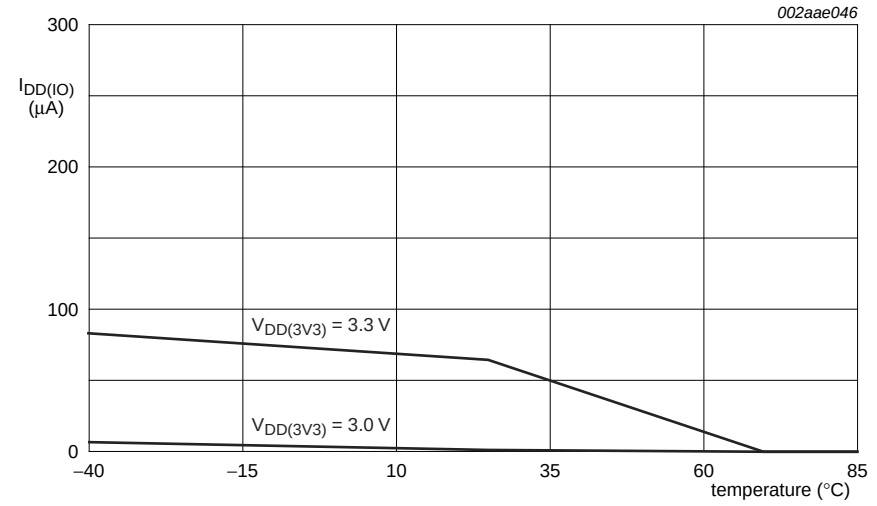
The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a coprocessor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 7. Total DC-to-DC converter supply current $I_{DD(DCDC)pd(3V3)}$ at different temperatures in Power-down mode

10.2 Deep power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 8. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Deep power-down mode

11.5 Dynamic external memory interface

Table 15. Dynamic characteristics: Dynamic external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V, EMC Dynamic Read Config Register = 0x0 (RD = 00)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Common							
$t_{d(SV)}$	chip select valid delay time		[1]	-	1.05	1.76	ns
$t_{h(S)}$	chip select hold time		[1]	0.1	1.02	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		[1]	-	1.51	1.95	ns
$t_{h(RAS)}$	row address strobe hold time		[1]	0.5	1.51	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		[1]	-	0.98	1.27	ns
$t_{h(CAS)}$	column address strobe hold time		[1]	0.1	0.97	-	ns
$t_{d(WV)}$	write valid delay time		[1]	-	0.84	1.95	ns
$t_{h(W)}$	write hold time		[1]	0.1	0.84	-	ns
$t_{d(GV)}$	output enable valid delay time		[1]	-	0.95	1.86	ns
$t_{h(G)}$	output enable hold time		[1]	0.1	1	-	ns
$t_{d(AV)}$	address valid delay time		[1]	-	0.87	1.95	ns
$t_{h(A)}$	address hold time		[1]	0.1	0.81	-	ns
Read cycle parameters							
$t_{su(D)}$	data input set-up time		[1]	0.51	2.24	-	ns
$t_{h(D)}$	data input hold time		[1]	0.57	2.41	-	ns
Write cycle parameters							
$t_{d(QV)}$	data output valid delay time		[1]	-	2.65	4.36	ns
$t_{h(Q)}$	data output hold time		[1]	0.49	2.61	-	ns

[1] See Figure 18.

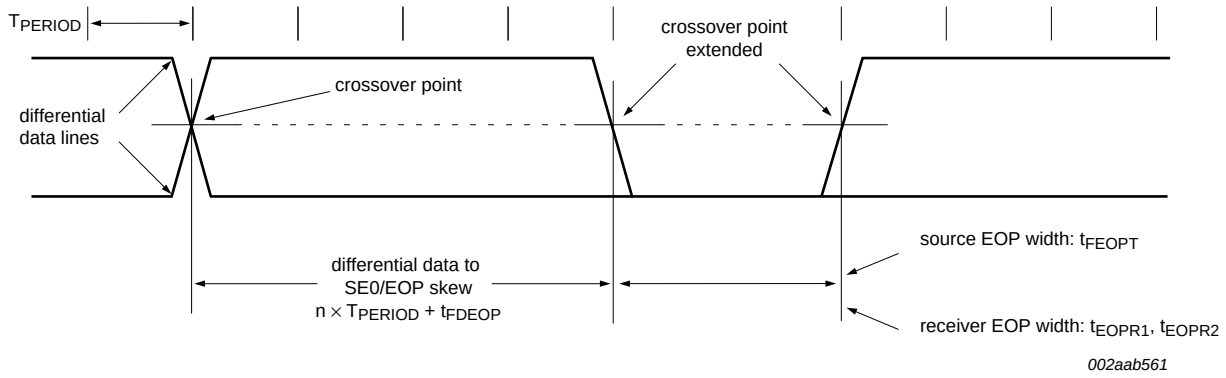


Fig 16. Differential data-to-EOP transition skew and EOP width

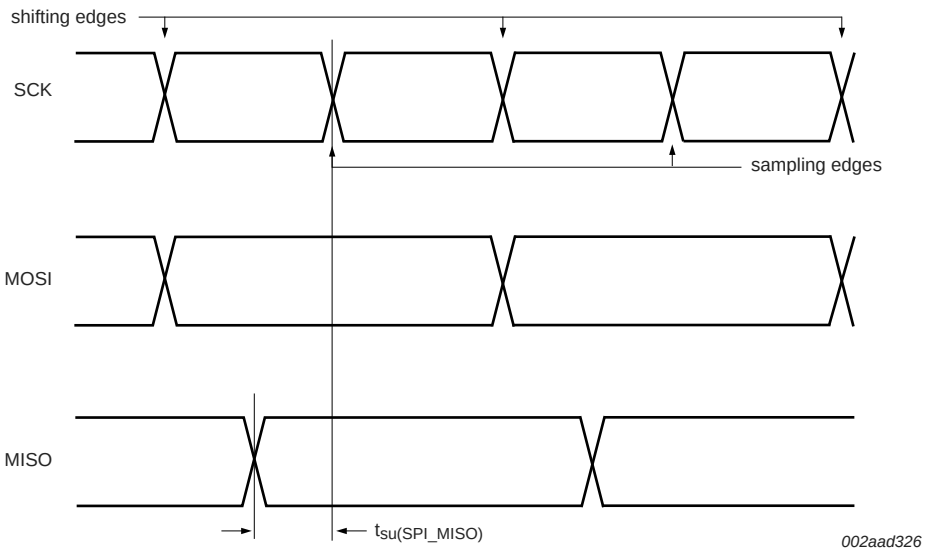


Fig 17. MISO line set-up time in SSP Master mode

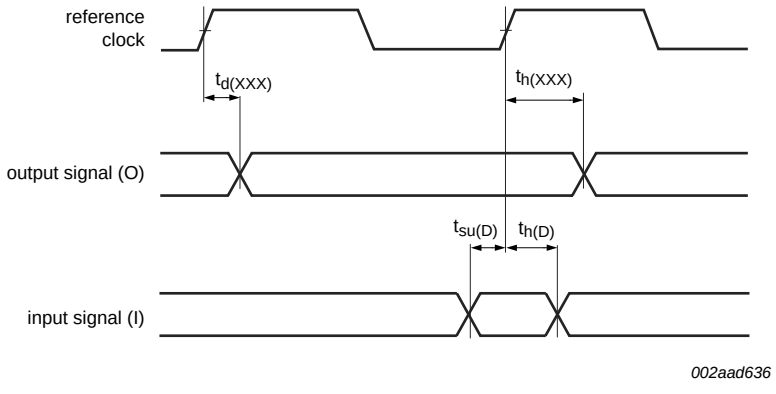


Fig 18. Signal timing

12. ADC electrical characteristics

Table 17. ADC characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB
E_G	gain error		[1][6]	-	-	±0.5	%
E_T	absolute error		[1][7]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[8]	-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 19.

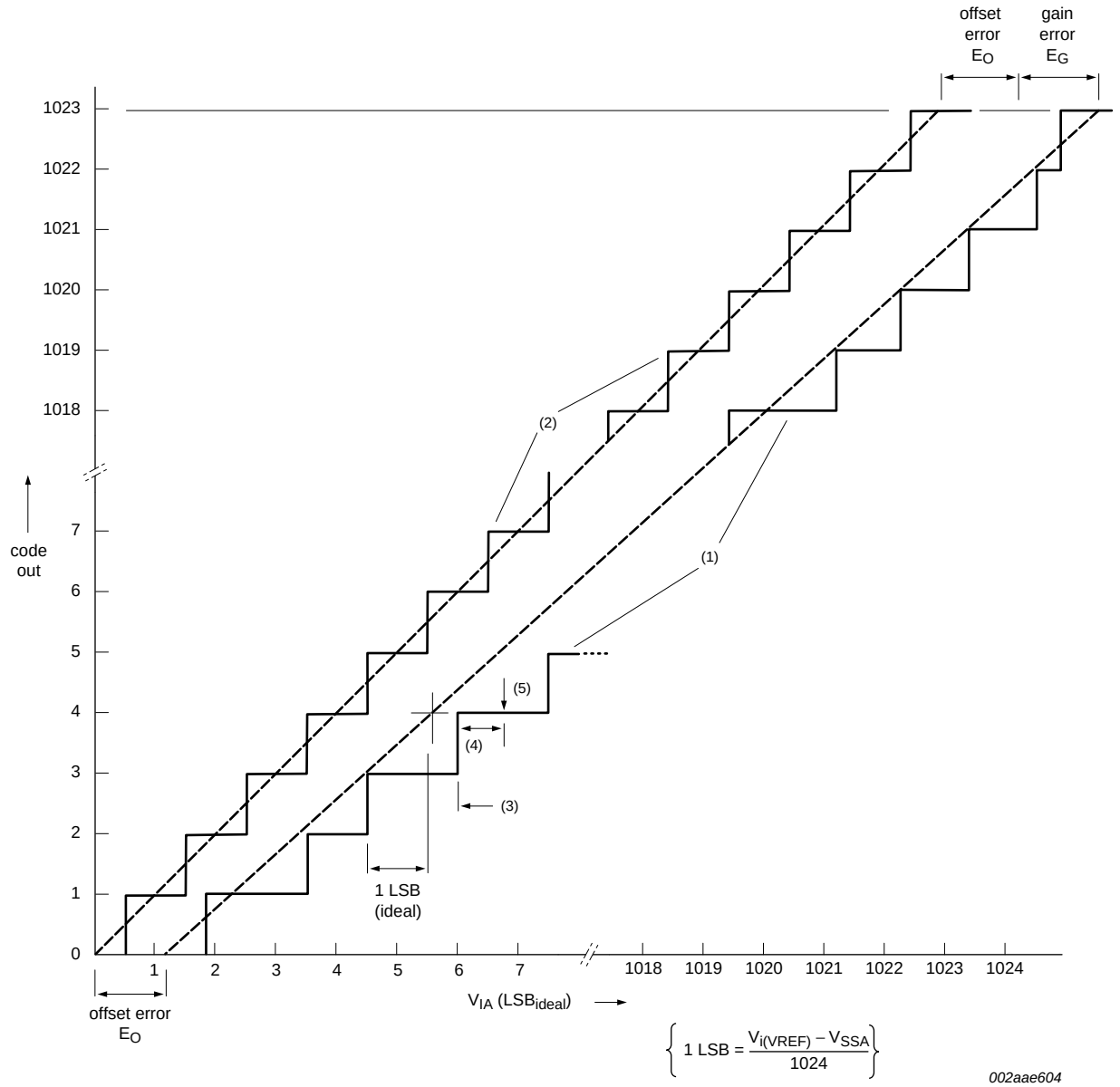
[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 19.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 19.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 19.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 19.

[8] See Figure 20.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 19. ADC characteristics

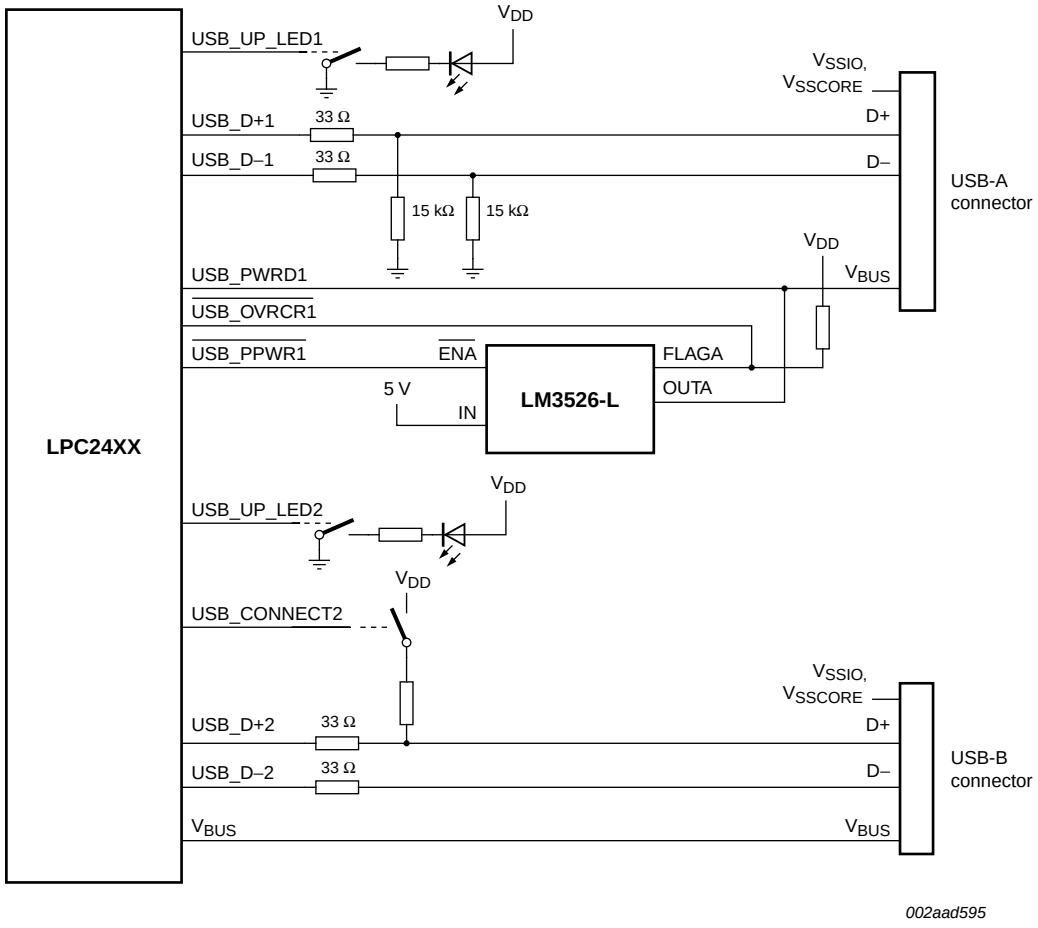


Fig 27. LPC2420/2460 USB OTG port configuration: USB port 2 device, USB port 1 host

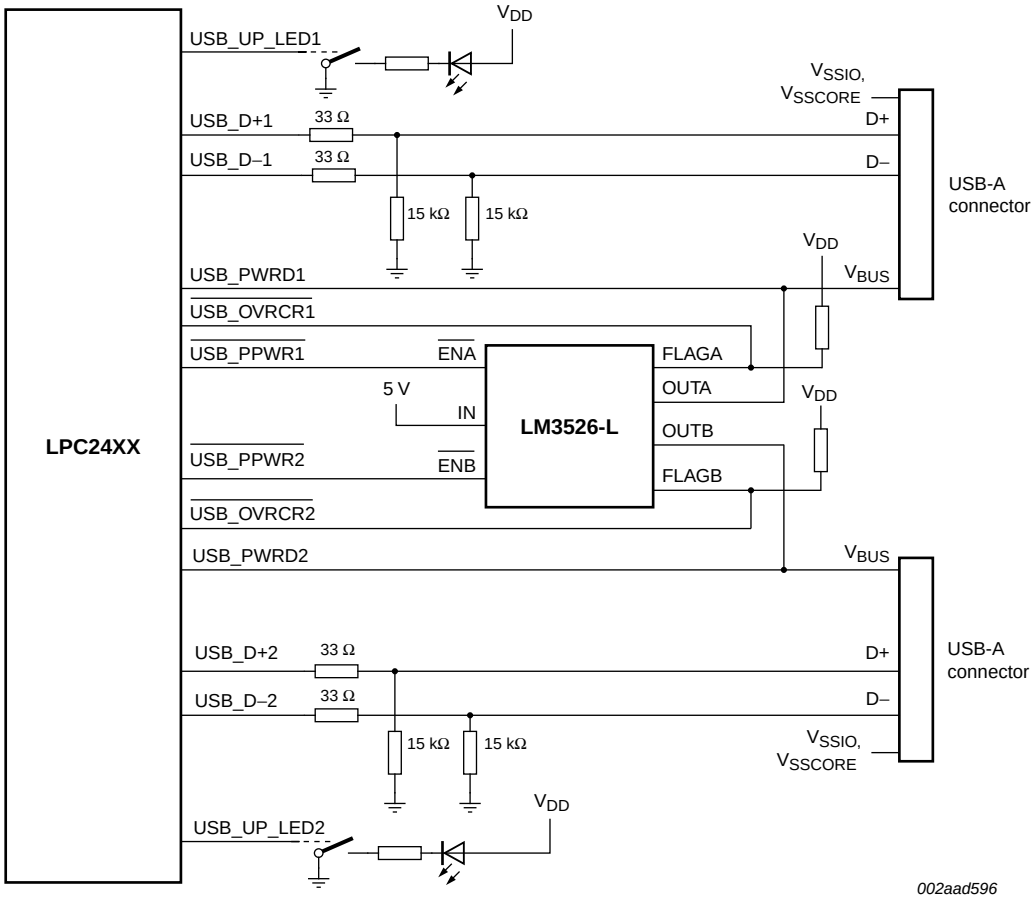


Fig 28. LPC2420/2460 USB OTG port configuration: USB port 1 host, USB port 2 host

14.3 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor C_i / (C_i + C_g). In slave mode, a minimum of 200 mV (RMS) is needed.

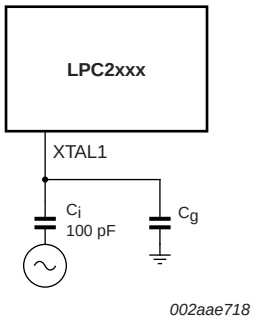


Fig 29. Slave mode operation of the on-chip oscillator