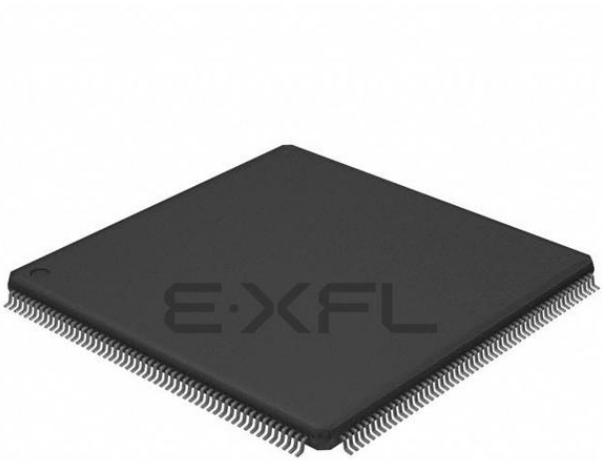

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	160
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2460fbd208-551

- EMC provides support for asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as single data rate SDRAM.
- Advanced Vectored Interrupt Controller (VIC), supporting up to 32 vectored interrupts.
- General Purpose DMA controller (GPDMA) on AHB that can be used with the SSP, I^2S, and SD/MMC interface as well as for memory-to-memory transfers.
- Serial Interfaces:
  - Ethernet MAC with MII/RMII interface and associated DMA controller (LPC2460 only). These functions reside on an independent AHB.
  - USB 2.0 full-speed dual port device/host/OTG controller with on-chip PHY and associated DMA controller.
  - Four UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO.
  - CAN controller with two channels (LPC2460 only).
  - SPI controller.
  - Two SSP controllers, with FIFO and multi-protocol capabilities. One is an alternate for the SPI port, sharing its interrupt. SSPs can be used with the GPDMA controller.
  - Three I^2C-bus interfaces (one with open-drain and two with standard port pins).
  - I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- Other peripherals:
  - SD/MMC memory card interface.
  - 160 General purpose I/O pins with configurable pull-up/down resistors.
  - 10-bit ADC with input multiplexing among 8 pins.
  - 10-bit DAC.
  - Four general purpose timers/counters with 8 capture inputs and 10 compare outputs. Each timer block has an external count input.
  - Two PWM/timer blocks with support for three-phase motor control. Each PWM has an external count inputs.
  - RTC with separate power domain. Clock source can be the RTC oscillator or the APB clock.
  - 2 kB SRAM powered from the RTC power pin, allowing data to be stored when the rest of the chip is powered off.
  - WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.
- Single 3.3 V power supply (3.0 V to 3.6 V).
- Four reduced power modes: idle, sleep, power-down, and deep power-down.
- Four external interrupt inputs configurable as edge/level sensitive. All pins on port 0 and port 2 can be used as edge sensitive interrupt sources.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, port 0/2 pin interrupt, Ethernet wake-up interrupt (LPC2460 only), CAN bus activity (LPC2460 only)).
- Two independent power domains allow fine tuning of power consumption based on needed features.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P0[3]/RXD0	204[1]	D6[1]	I/O	**P0[3] —** General purpose digital input/output pin.
			I	**RXD0 —** Receiver input for UART0.
P0[4]/ I2SRX_CLK/ RD2/CAP2[0]	168[1]	B12[1]	I/O	**P0[4] —** General purpose digital input/output pin.
			I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
			I	**RD2 —** CAN2 receiver input (LPC2460 only).
			I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/ I2SRX_WS/ TD2/CAP2[1]	166[1]	C12[1]	I/O	**P0[5] —** General purpose digital input/output pin.
			I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
			O	**TD2 —** CAN2 transmitter output (LPC2460 only).
			I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	164[1]	D13[1]	I/O	**P0[6] —** General purpose digital input/output pin.
			I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
			I/O	**SSEL1 —** Slave Select for SSP1.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/ I2STX_CLK/ SCK1/MAT2[1]	162[1]	C13[1]	I/O	**P0[7] —** General purpose digital input/output pin.
			I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
			I/O	**SCK1 —** Serial Clock for SSP1.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/ I2STX_WS/ MISO1/MAT2[2]	160[1]	A15[1]	I/O	**P0[8] —** General purpose digital input/output pin.
			I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
			O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/ I2STX_SDA/ MOSI1/MAT2[3]	158[1]	C14[1]	I/O	**P0[9] —** General purpose digital input/output pin.
			I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
			O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	98[1]	T15[1]	I/O	**P0[10] —** General purpose digital input/output pin.
			O	**TXD2 —** Transmitter output for UART2.
			I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
			O	**MAT3[0] —** Match output for Timer 3, channel 0.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P2[25]/ CKEOUT1	54[1]	R4[1]	I/O	**P2[25] —** General purpose digital input/output pin.
			O	**CKEOUT1 —** SDRAM clock enable 1.
P2[26]/ CKEOUT2/ MAT3[0]/MISO0	57[1]	T4[1]	I/O	**P2[26] —** General purpose digital input/output pin.
			O	**CKEOUT2 —** SDRAM clock enable 2.
			O	**MAT3[0] —** Match output for Timer 3, channel 0.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
P2[27]/ CKEOUT3/ MAT3[1]/MOSI0	47[1]	P3[1]	I/O	**P2[27] —** General purpose digital input/output pin.
			O	**CKEOUT3 —** SDRAM clock enable 3.
			O	**MAT3[1] —** Match output for Timer 3, channel 1.
			I/O	**MOSI0 —** Master Out Slave In for SSP0.
P2[28]/ DQMOUT0	49[1]	P4[1]	I/O	**P2[28] —** General purpose digital input/output pin.
			O	**DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
P2[29]/ DQMOUT1	43[1]	N3[1]	I/O	**P2[29] —** General purpose digital input/output pin.
			O	**DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
P2[30]/ DQMOUT2/ MAT3[2]/SDA2	31[1]	L4[1]	I/O	**P2[30] —** General purpose digital input/output pin.
			O	**DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
			O	**MAT3[2] —** Match output for Timer 3, channel 2.
			I/O	**SDA2 —** I^2C2 data input/output (this is not an open-drain pin).
P2[31]/ DQMOUT3/ MAT3[3]/SCL2	39[1]	N2[1]	I/O	**P2[31] —** General purpose digital input/output pin.
			O	**DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
			O	**MAT3[3] —** Match output for Timer 3, channel 3.
			I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
P3[0] to P3[31]			I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect block.
P3[0]/D0	197[1]	B4[1]	I/O	**P3[0] —** General purpose digital input/output pin.
			I/O	**D0 —** External memory data line 0.
P3[1]/D1	201[1]	B3[1]	I/O	**P3[1] —** General purpose digital input/output pin.
			I/O	**D1 —** External memory data line 1.
P3[2]/D2	207[1]	B1[1]	I/O	**P3[2] —** General purpose digital input/output pin.
			I/O	**D2 —** External memory data line 2.
P3[3]/D3	3[1]	E4[1]	I/O	**P3[3] —** General purpose digital input/output pin.
			I/O	**D3 —** External memory data line 3.
P3[4]/D4	13[1]	F2[1]	I/O	**P3[4] —** General purpose digital input/output pin.
			I/O	**D4 —** External memory data line 4.
P3[5]/D5	17[1]	G1[1]	I/O	**P3[5] —** General purpose digital input/output pin.
			I/O	**D5 —** External memory data line 5.
P3[6]/D6	23[1]	J1[1]	I/O	**P3[6] —** General purpose digital input/output pin.
			I/O	**D6 —** External memory data line 6.
P3[7]/D7	27[1]	L1[1]	I/O	**P3[7] —** General purpose digital input/output pin.
			I/O	**D7 —** External memory data line 7.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P3[31]/D31/ MAT1[2]	25[1]	J3[1]	I/O	**P3[31] —** General purpose digital input/output pin.
			I/O	**D31 —** External memory data line 31.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P4[0] to P4[31]			I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the Pin Connect block.
P4[0]/A0	75[1]	U9[1]	I/O	**P4[0] —**]General purpose digital input/output pin.
			I/O	**A0 —** External memory address line 0.
P4[1]/A1	79[1]	U10[1]	I/O	**P4[1] —** General purpose digital input/output pin.
			I/O	**A1 —** External memory address line 1.
P4[2]/A2	83[1]	T11[1]	I/O	**P4[2] —** General purpose digital input/output pin.
			I/O	**A2 —** External memory address line 2.
P4[3]/A3	97[1]	U16[1]	I/O	**P4[3] —** General purpose digital input/output pin.
			I/O	**A3 —** External memory address line 3.
P4[4]/A4	103[1]	R15[1]	I/O	**P4[4] —** General purpose digital input/output pin.
			I/O	**A4 —** External memory address line 4.
P4[5]/A5	107[1]	R16[1]	I/O	**P4[5] —** General purpose digital input/output pin.
			I/O	**A5 —** External memory address line 5.
P4[6]/A6	113[1]	M14[1]	I/O	**P4[6] —** General purpose digital input/output pin.
			I/O	**A6 —** External memory address line 6.
P4[7]/A7	121[1]	L16[1]	I/O	**P4[7] —** General purpose digital input/output pin.
			I/O	**A7 —** External memory address line 7.
P4[8]/A8	127[1]	J17[1]	I/O	**P4[8] —** General purpose digital input/output pin.
			I/O	**A8 —** External memory address line 8.
P4[9]/A9	131[1]	H17[1]	I/O	**P4[9] —** General purpose digital input/output pin.
			I/O	**A9 —** External memory address line 9.
P4[10]/A10	135[1]	G17[1]	I/O	**P4[10] —** General purpose digital input/output pin.
			I/O	**A10 —** External memory address line 10.
P4[11]/A11	145[1]	F14[1]	I/O	**P4[11] —** General purpose digital input/output pin.
			I/O	**A11 —** External memory address line 11.
P4[12]/A12	149[1]	C16[1]	I/O	**P4[12] —** General purpose digital input/output pin.
			I/O	**A12 —** External memory address line 12.
P4[13]/A13	155[1]	B16[1]	I/O	**P4[13] —** General purpose digital input/output pin.
			I/O	**A13 —** External memory address line 13.
P4[14]/A14	159[1]	B15[1]	I/O	**P4[14] —** General purpose digital input/output pin.
			I/O	**A14 —** External memory address line 14.
P4[15]/A15	173[1]	A11[1]	I/O	**P4[15] —** General purpose digital input/output pin.
			I/O	**A15 —** External memory address line 15.
P4[16]/A16	101[1]	U17[1]	I/O	**P4[16] —** General purpose digital input/output pin.
			I/O	**A16 —** External memory address line 16.

Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P4[17]/A17	104[1]	P14[1]	I/O	**P4[17] —** General purpose digital input/output pin.
			I/O	**A17 —** External memory address line 17.
P4[18]/A18	105[1]	P15[1]	I/O	**P4[18] —** General purpose digital input/output pin.
			I/O	**A18 —** External memory address line 18.
P4[19]/A19	111[1]	P16[1]	I/O	**P4[19] —** General purpose digital input/output pin.
			I/O	**A19 —** External memory address line 19.
P4[20]/A20/ SDA2/SCK1	109[1]	R17[1]	I/O	**P4[20] —** General purpose digital input/output pin.
			I/O	**A20 —** External memory address line 20.
			I/O	**SDA2 —** I^2C2 data input/output (this is not an open-drain pin).
			I/O	**SCK1 —** Serial Clock for SSP1.
P4[21]/A21/ SCL2/SSEL1	115[1]	M15[1]	I/O	**P4[21] —** General purpose digital input/output pin.
			I/O	**A21 —** External memory address line 21.
			I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
			I/O	**SSEL1 —** Slave Select for SSP1.
P4[22]/A22/ TXD2/MISO1	123[1]	K14[1]	I/O	**P4[22] —** General purpose digital input/output pin.
			I/O	**A22 —** External memory address line 22.
			O	**TXD2 —** Transmitter output for UART2.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
P4[23]/A23/ RXD2/MOSI1	129[1]	J15[1]	I/O	**P4[23] —** General purpose digital input/output pin.
			I/O	**A23 —** External memory address line 23.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
P4[24]/$\overline{OE}$	183[1]	B8[1]	I/O	**P4[24] —** General purpose digital input/output pin.
			O	**$\overline{OE}$ —** LOW active Output Enable signal.
P4[25]/$\overline{WE}$	179[1]	B9[1]	I/O	**P4[25] —** General purpose digital input/output pin.
			O	**$\overline{WE}$ —** LOW active Write Enable signal.
P4[26]/$\overline{BLS0}$	119[1]	L15[1]	I/O	**P4[26] —** General purpose digital input/output pin.
			O	**$\overline{BLS0}$ —** LOW active Byte Lane select signal 0.
P4[27]/$\overline{BLS1}$	139[1]	G15[1]	I/O	**P4[27] —** General purpose digital input/output pin.
			O	**$\overline{BLS1}$ —** LOW active Byte Lane select signal 1.
P4[28]/$\overline{BLS2}$/ MAT2[0]/TXD3	170[1]	C11[1]	I/O	**P4 [28] —** General purpose digital input/output pin.
			O	**$\overline{BLS2}$ —** LOW active Byte Lane select signal 2.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.
			O	**TXD3 —** Transmitter output for UART3.
P4[29]/$\overline{BLS3}$/ MAT2[1]/RXD3	176[1]	B10[1]	I/O	**P4[29] —** General purpose digital input/output pin.
			O	**$\overline{BLS3}$ —** LOW active Byte Lane select signal 3.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
			I	**RXD3 —** Receiver input for UART3.
P4[30]/$\overline{CS0}$	187[1]	B7[1]	I/O	**P4[30] —** General purpose digital input/output pin.
			O	**$\overline{CS0}$ —** LOW active Chip Select 0 signal.

7. Functional description

7.1 Architectural overview

The LPC2420/2460 microcontroller consists of an ARM7TDMI-S CPU with emulation support, the ARM7 local bus for closely coupled, high-speed access to the majority of on-chip memory, the AMBA AHB interfacing to high-speed on-chip peripherals and external memory, and the AMBA APB for connection to other on-chip peripheral functions. The microcontroller permanently configures the ARM7TDMI-S processor for little-endian byte order.

The LPC2460 only implements two AHB in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the VIC, GPDMA controller, and EMC.

The second AHB (LPC2460 only), referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

AHB peripherals are allocated a 2 MB range of addresses at the very top of the 4 GB ARM memory space. Each AHB peripheral is allocated a 16 kB address space within the AHB address space. Lower speed peripheral functions are connected to the APB. The AHB to APB bridge interfaces the APB to the AHB. APB peripherals are also allocated a 2 MB range of addresses, beginning at the 3.5 GB address point. Each APB peripheral is allocated a 16 kB address space within the APB address space.

The ARM7TDMI-S processor is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed complex instruction set computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- the standard 32-bit ARM set
- a 16-bit Thumb set

- One AHB master for transferring data. This interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data. Usually the burst size is set to half the size of the FIFO in the peripheral.
- Internal four-word FIFO per channel.
- Supports 8-bit, 16-bit, and 32-bit wide transactions.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Interrupt masking. The DMA error and DMA terminal count interrupt requests can be masked.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC2420/2460 use accelerated GPIO functions:

- GPIO registers are relocated to the ARM local bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.

Additionally, any pin on port 0 and port 2 (total of 64 pins) that is not configured as an analog input/output can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake the chip up from Power-down mode.

7.8.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Backward compatibility with other earlier devices is maintained with legacy port 0 and port 1 registers appearing at the original addresses on the APB.

7.17.1 Features

- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.
- Conforms to *Multimedia Card Specification v2.11*.
- Conforms to *Secure Digital Memory Card Physical Layer Specification, v0.96.*
- Can be used as a multimedia card bus or a secure digital memory card bus host. The SD/MMC can be connected to several multimedia cards or a single secure digital memory card.
- DMA supported through the GPDMA controller.

7.18 I^2C-bus serial I/O controller

The LPC2420/2460 contains three I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus and can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2420/2460 supports bit rates up to 400 kbit/s (Fast I^2C-bus).

7.18.1 Features

- I^2C0 is a standard I^2C compliant bus interface with open-drain pins.
- I^2C1 and I^2C2 use standard I/O pins and do not support powering off of individual devices connected to the same bus lines.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.

7.19 I^2S-bus serial I/O controllers

The I^2S-bus provides a standard communication interface for digital audio applications.

Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[9]	$V_{DD(3V3)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[9]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[9]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[9]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[11]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V	[11]	0	0	0	μA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[9]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	1.8	1.95	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	1.8	1.95	V

11. Dynamic characteristics

Table 10. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
I^2C-bus pins (P0[27] and P0[28])						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns
SSP interface						
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 17	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

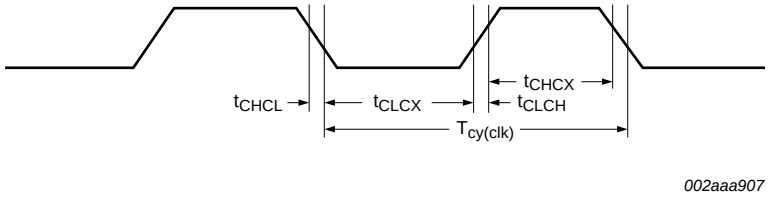


Fig 13. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Static external memory interface

Table 14. Dynamic characteristics: Static external memory interface
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles[1]						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		−0.29	0.20	2.54	ns
Read cycle parameters[1][2]						
t_{OELAV}	$\overline{OE}$ LOW to address valid time		−0.29	0.20	2.54	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		−0.78 + $T_{cy(CCLK)}$ × WAITOEN	0 + $T_{cy(CCLK)}$ × WAITOEN	0.49 + $T_{cy(CCLK)}$ × WAITOEN	ns
t_{am}	memory access time	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 12.70	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 9.57	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 8.11	ns
$t_{h(D)}$	data input hold time	[5]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		−0.49	0	0.20	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		−0.20	0.20	2.44	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		−0.59 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0.10 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time		−0.39	0	2.54	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time		−0.88	0.49	0.68	ns
Write cycle parameters[1][6]						
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		−0.88 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.10 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	0.20 + $T_{cy(CCLK)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		−0.88	0.49	0.98	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		0.68	2.54	5.86	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		0	2.64	4.79	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[3]	−0.78 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	0.10 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 1)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[3]	−0.88 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	0 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	0.59 + $T_{cy(CCLK)}$ × (WAITWR − WAITWEN + 3)	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[3]	0 + $T_{cy(CCLK)}$	0.20 + $T_{cy(CCLK)}$	2.74 + $T_{cy(CCLK)}$	ns

Table 14. Dynamic characteristics: Static external memory interface *…continued*
C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time		[3]	0.78 + $T_{cy(CCLK)}$	2.54 + $T_{cy(CCLK)}$	5.96 + $T_{cy(CCLK)}$	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		[3]	−0.29	0.20	2.54	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		[3]	0	2.54	5.37	ns

[1] V_{OH} = 2.5 V, V_{OL} = 0.2 V.

[2] V_{IH} = 2.5 V, V_{IL} = 0.5 V.

[3] $T_{cy(CCLK)} = {}^{1}/_{CCLK}$.

[4] Latest of address valid, $\overline{CS}$ LOW, $\overline{OE}$ LOW to data valid.

[5] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

[6] Byte lane state bit (PB) = 1.

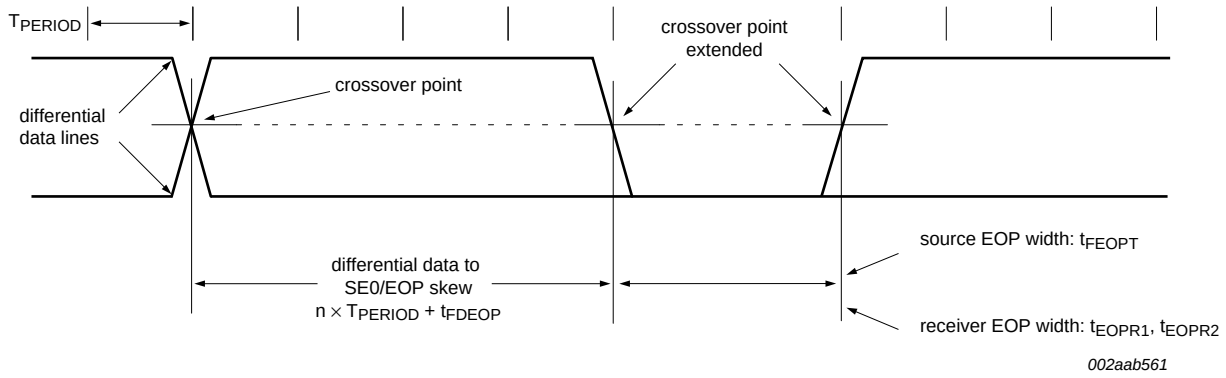


Fig 16. Differential data-to-EOP transition skew and EOP width

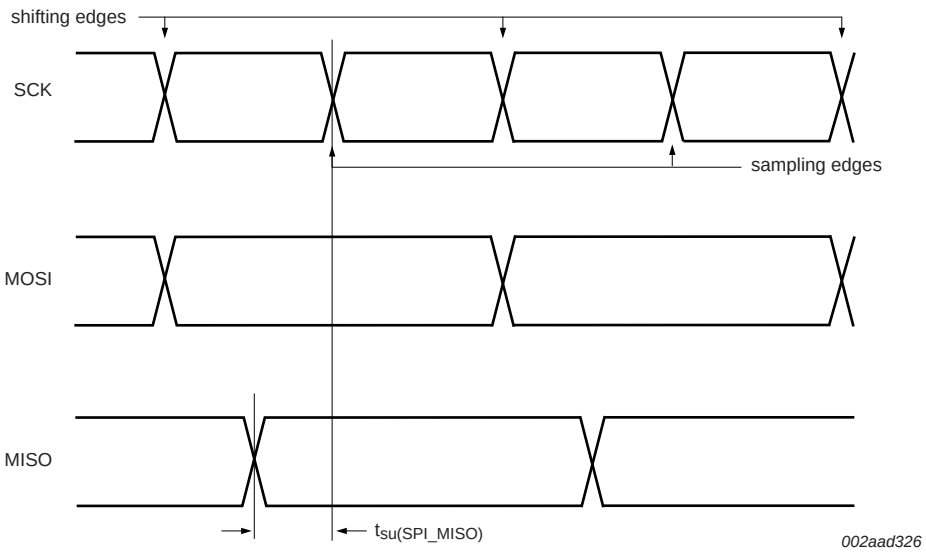


Fig 17. MISO line set-up time in SSP Master mode

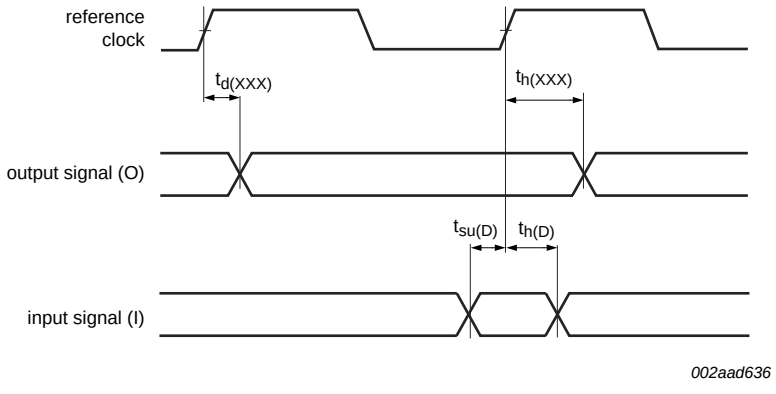


Fig 18. Signal timing

12. ADC electrical characteristics

Table 17. ADC characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB
E_G	gain error		[1][6]	-	-	±0.5	%
E_T	absolute error		[1][7]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[8]	-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 19.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 19.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 19.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 19.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 19.

[8] See Figure 20.

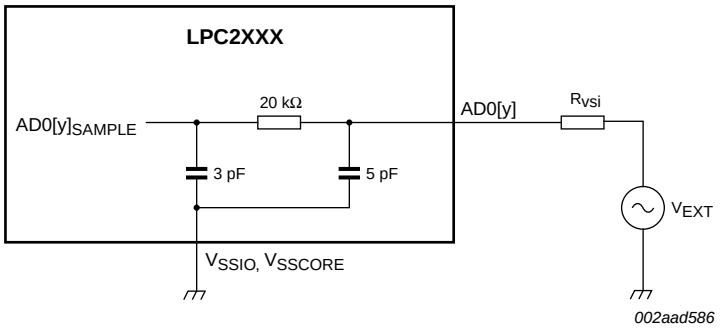


Fig 20. Suggested ADC interface - LPC2420/2460 AD0[y] pin

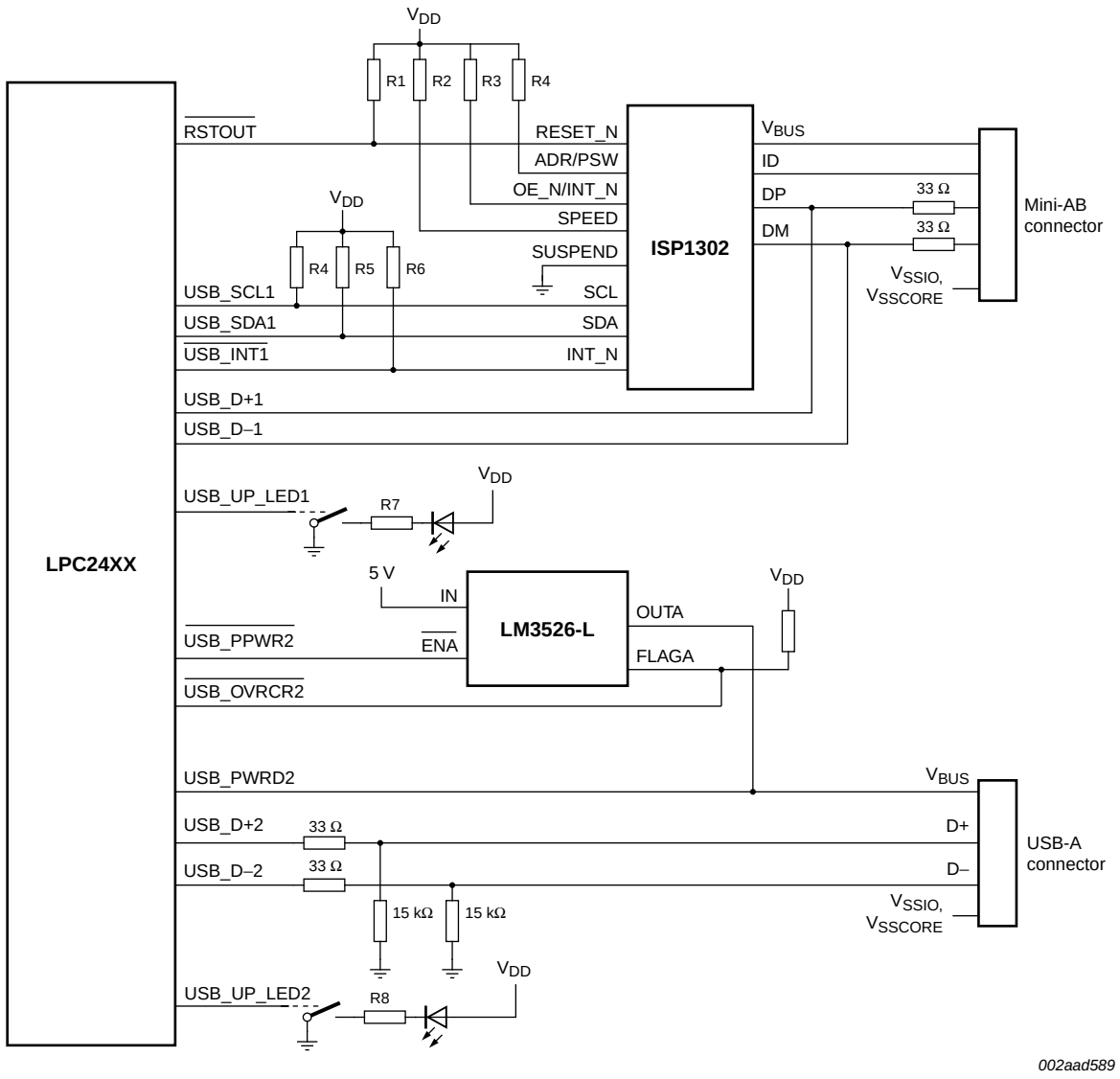


Fig 25. LPC2420/2460 USB OTG port configuration: USB port 1 OTG dual-role device, USB port 2 host

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 29), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTAL2 pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 30 and in Table 19 and Table 20. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 30 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

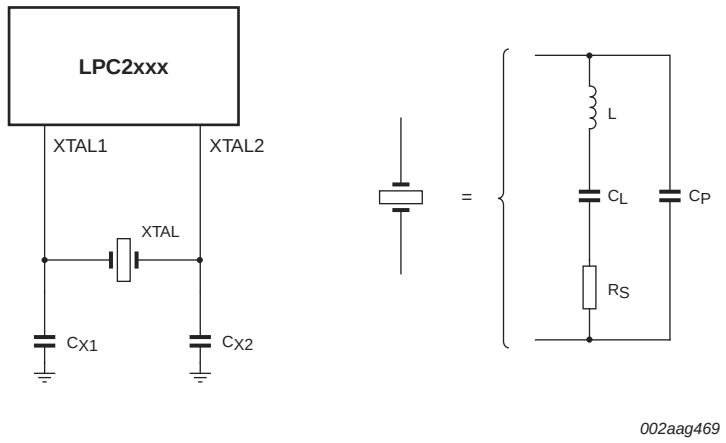
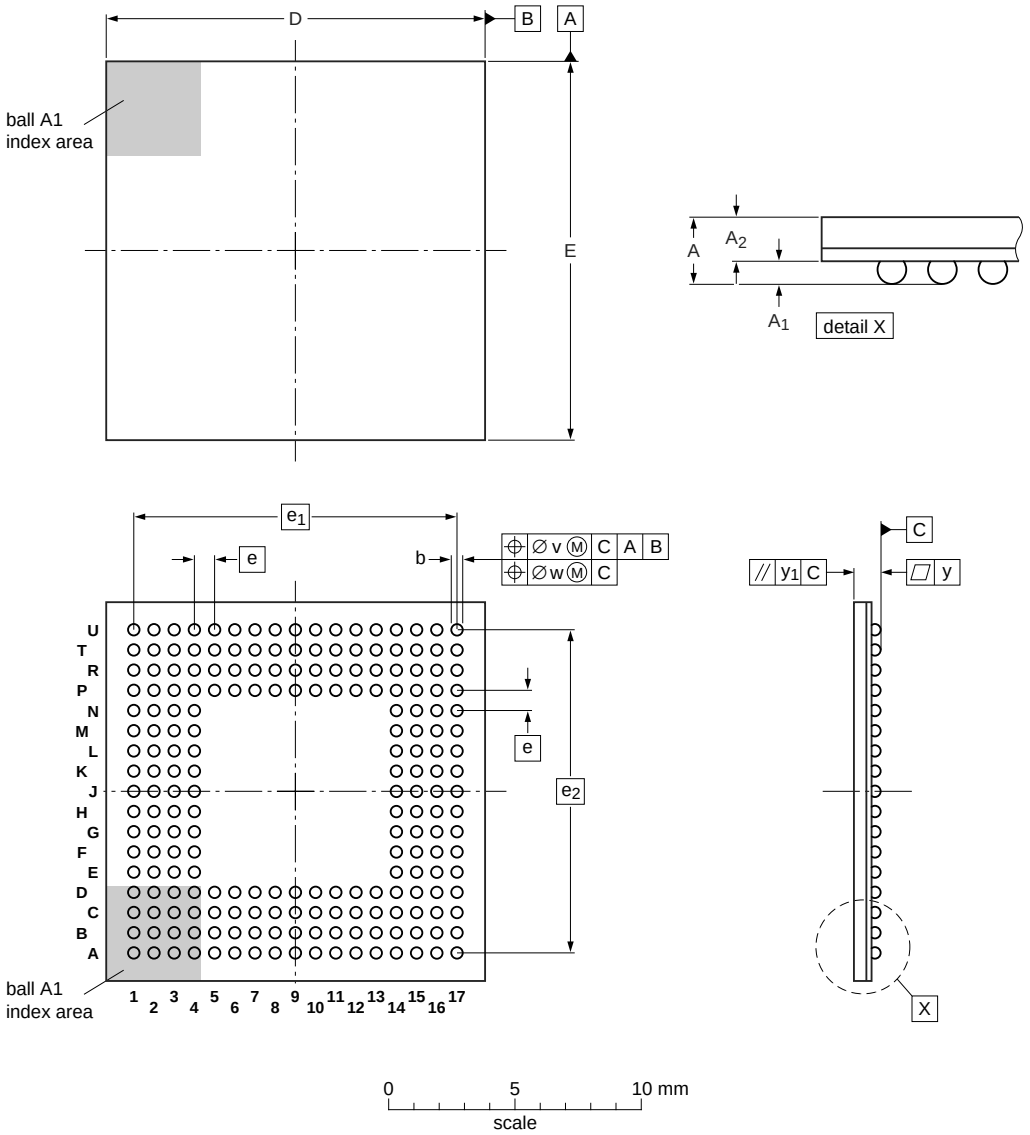


Fig 30. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 19. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 35. Package outline SOT950-1 (TFBGA208)

16. Abbreviations

Table 22. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DCC	Debug Communication Channel
DMA	Direct Memory Access
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GP	General Purpose
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
IAP	In-Application Programming
ISP	In-System Programming
JTAG	Joint Test Action Group
MII	Media Independent Interface
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SD/MMC	Secure Digital/MultiMediaCard
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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