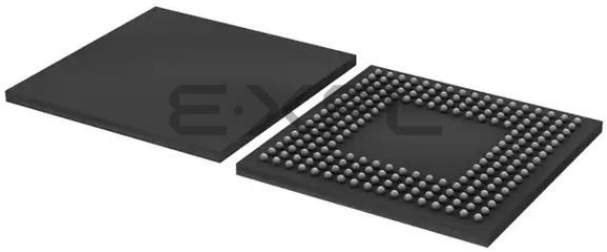

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Number of I/O	160
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
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Oscillator Type	Internal
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Supplier Device Package	208-TFBGA (15x15)
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Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
17	P1[5]/ENET_TX_ER/ MCIPWR/PWM0[3]		-		-		-
Row B							
1	P3[2]/D2	2	P3[10]/D10	3	P3[1]/D1	4	P3[0]/D0
5	P1[1]/ENET_TXD1	6	V_{SSIO}	7	P4[30]/$\overline{CS0}$	8	P4[24]/$\overline{OE}$
9	P4[25]/$\overline{WE}$	10	P4[29]/$\overline{BLS3}$/ MAT2[1]/RXD3	11	P1[6]/ENET_TX_CLK/ MCIDAT0/PWM0[4]	12	P0[4]/I2SRX_CLK/RD2/ CAP2[0]
13	$V_{DD(3V3)}$	14	P3[19]/D19/ PWM0[4]/DCD1	15	P4[14]/A14	16	P4[13]/A13
17	P2[0]/PWM1[1]/TXD1/ TRACECLK		-		-		-
Row C							
1	P3[13]/D13	2	TDI	3	RTCK	4	P0[2]/TXD0
5	P3[9]/D9	6	P3[22]/D22/ PCAP0[0]/RI1	7	P1[8]/ENET_CRS_DV/ ENET_CRS	8	P1[10]/ENET_RXD1
9	$V_{DD(3V3)}$	10	P3[21]/D21/ PWM0[6]/DTR1	11	P4[28]/$\overline{BLS2}$/ MAT2[0]/TXD3	12	P0[5]/I2SRX_WS/TD2/ CAP2[1]
13	P0[7]/I2STX_CLK/SCK1 /MAT2[1]	14	P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	15	P3[18]/D18/ PWM0[3]/CTS1	16	P4[12]/A12
17	$V_{DD(3V3)}$		-		-		-
Row D							
1	$\overline{TRST}$	2	P3[28]/D28/ CAP1[1]/PWM1[5]	3	TDO	4	P3[12]/D12
5	P3[11]/D11	6	P0[3]/RXD0	7	$V_{DD(3V3)}$	8	P3[8]/D8
9	P1[2]/ENET_TXD2/ MCICLK/PWM0[1]	10	P1[16]/ENET_MDC	11	$V_{DD(DCDC)(3V3)}$	12	V_{SSCORE}
13	P0[6]/I2SRX_SDA/ SSEL1/MAT2[0]	14	P1[7]/ENET_COL/ MCIDAT1/PWM0[5]	15	P2[2]/PWM1[3]/ CTS1/PIPESTAT1	16	P1[13]/ENET_RX_DV
17	P2[4]/PWM1[5]/ DSR1/TRACESYNC		-		-		-
Row E							
1	P0[26]/AD0[3]/ AOUT/RXD3	2	TCK	3	TMS	4	P3[3]/D3
14	P2[1]/PWM1[2]/RXD1/ PIPESTAT0	15	V_{SSIO}	16	P2[3]/PWM1[4]/ DCD1/PIPESTAT2	17	P2[6]/PCAP1[0]/ RI1/TRACEPKT1
Row F							
1	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	2	P3[4]/D4	3	P3[29]/D29/ MAT1[0]/PWM1[6]	4	DBGEN
14	P4[11]/A11	15	P3[17]/D17/ PWM0[2]/RXD1	16	P2[5]/PWM1[6]/ DTR1/TRACEPKT0	17	P3[16]/D16/ PWM0[1]/TXD1
Row G							
1	P3[5]/D5	2	P0[24]/AD0[1]/ I2SRX_WS/CAP3[1]	3	$V_{DD(3V3)}$	4	V_{DDA}
14	n.c.	15	P4[27]/$\overline{BLS1}$	16	P2[7]/RD2/ RTS1/TRACEPKT2	17	P4[10]/A10

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Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row H							
1	P0[23]/AD0[0]/ I2SRX_CLK/CAP3[0]	2	P3[14]/D14	3	P3[30]/D30/ MAT1[1]/RTS1	4	$V_{DD(DCDC)(3V3)}$
14	V_{SSIO}	15	P2[8]/TD2/ TXD2/TRACEPKT3	16	P2[9]/ USB_CONNECT1/ RXD2/EXTIN0	17	P4[9]/A9
Row J							
1	P3[6]/D6	2	V_{SSA}	3	P3[31]/D31/MAT1[2]	4	n.c.
14	P0[16]/RXD1/ SSEL0/SSEL	15	P4[23]/A23/ RXD2/MOSI1	16	P0[15]/TXD1/ SCK0/SCK	17	P4[8]/A8
Row K							
1	VREF	2	RTCX1	3	$\overline{\text{RSTOUT}}$	4	V_{SSCORE}
14	P4[22]/A22/ TXD2/MISO1	15	P0[18]/DCD1/ MOSI0/MOSI	16	$V_{DD(3V3)}$	17	P0[17]/CTS1/ MISO0/MISO
Row L							
1	P3[7]/D7	2	RTCX2	3	V_{SSIO}	4	P2[30]/DQMOUT2/ MAT3[2]/SDA2
14	n.c.	15	P4[26]/$\overline{\text{BLS0}}$	16	P4[7]/A7	17	P0[19]/DSR1/ MCICLK/SDA1
Row M							
1	P3[15]/D15	2	$\overline{\text{RESET}}$	3	VBAT	4	XTAL1
14	P4[6]/A6	15	P4[21]/A21/ SCL2/SSEL1	16	P0[21]/RI1/ MCIPWR/RD1	17	P0[20]/DTR1/ MCICMD/SCL1
Row N							
1	ALARM	2	P2[31]/DQMOUT3/ MAT3[3]/SCL2	3	P2[29]/DQMOUT1	4	XTAL2
14	P2[12]/$\overline{\text{EINT2}}$/ MCIDAT2/I2STX_WS	15	P2[10]/$\overline{\text{EINT0}}$	16	V_{SSIO}	17	P0[22]/RTS1/ MCIDAT0/TD1
Row P							
1	P1[31]/$\overline{\text{USB\_OVRCR2}}$/ SCK1/AD0[5]	2	P1[30]/USB_PWRD2/ V_{BUS}/AD0[4]	3	P2[27]/CKEOUT3/ MAT3[1]/MOSI0	4	P2[28]/DQMOUT0
5	P2[24]/CKEOUT0	6	$V_{DD(3V3)}$	7	P1[18]/USB_UP_LED1/ PWM1[1]/CAP1[0]	8	$V_{DD(3V3)}$
9	P1[23]/USB_RX_DP1/ PWM1[4]/MISO0	10	V_{SSCORE}	11	$V_{DD(DCDC)(3V3)}$	12	V_{SSIO}
13	P2[15]/$\overline{\text{CS3}}$/ CAP2[1]/SCL1	14	P4[17]/A17	15	P4[18]/A18	16	P4[19]/A19
17	$V_{DD(3V3)}$		-		-		-
Row R							
1	P0[12]/$\overline{\text{USB\_PPWR2}}$/ MISO1/AD0[6]	2	P0[13]/USB_UP_LED2/ MOSI1/AD0[7]	3	P0[28]/SCL0	4	P2[25]/CKEOUT1
5	P3[24]/D24/ CAP0[1]/PWM1[1]	6	P0[30]/USB_D−1	7	P2[19]/CLKOUT1	8	P1[21]/USB_TX_DM1/ PWM1[3]/SSEL0
9	V_{SSIO}	10	P1[26]/$\overline{\text{USB\_SSPND1}}$/ PWM1[6]/CAP0[0]	11	P2[16]/$\overline{\text{CAS}}$	12	P2[14]/$\overline{\text{CS2}}$/ CAP2[0]/SDA1

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Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	P2[17]/$\overline{\text{RAS}}$	14	P0[11]/RXD2/SCL2/ MAT3[1]	15	P4[4]/A4	16	P4[5]/A5
17	P4[20]/A20/ SDA2/SCK1		-		-		-
Row T							
1	P0[27]/SDA0	2	P0[31]/USB_D+2	3	P3[26]/D26/ MAT0[1]/PWM1[3]	4	P2[26]/CKEOUT2/ MAT3[0]/MISO0
5	V_{SSIO}	6	P3[23]/D23/ CAP0[0]/PCAP1[0]	7	P0[14]/$\overline{\text{USB\_HSTEN2}}$/ USB_CONNECT2/ SSEL1	8	P2[20]/$\overline{\text{DYCS0}}$
9	P1[24]/USB_RX_DM1/ PWM1[5]/MOSI0	10	P1[25]/$\overline{\text{USB\_LS1}}$/ USB_HSTEN1/MAT1[1]	11	P4[2]/A2	12	P1[27]/$\overline{\text{USB\_INT1}}$/ USB_OVRCR1/CAP0[1]
13	P1[28]/USB_SCL1/ PCAP1[0]/MAT0[0]	14	P0[1]/TD1/RXD3/SCL1	15	P0[10]/TXD2/SDA2/ MAT3[0]	16	P2[13]/$\overline{\text{EINT3}}$/ MCIDAT3/I2STX_SDA
17	P2[11]/$\overline{\text{EINT1}}$/ MCIDAT1/I2STX_CLK		-		-		-
Row U							
1	USB_D−2	2	P3[25]/D25/ MAT0[0]/PWM1[2]	3	P2[18]/CLKOUT0	4	P0[29]/USB_D+1
5	P2[23]/$\overline{\text{DYCS3}}$/ CAP3[1]/SSEL0	6	P1[19]/$\overline{\text{USB\_TX\_E1}}$/ USB_PPWR1/CAP1[1]	7	P1[20]/USB_TX_DP1/ PWM1[2]/SCK0	8	P1[22]/USB_RCV1/ USB_PWRD1/MAT1[0]
9	P4[0]/A0	10	P4[1]/A1	11	P2[21]/$\overline{\text{DYCS1}}$	12	P2[22]/$\overline{\text{DYCS2}}$/ CAP3[0]/SCK0
13	$V_{DD(3V3)}$	14	P1[29]/USB_SDA1/ PCAP1[1]/MAT0[1]	15	P0[0]/RD1/TXD3/SDA1	16	P4[3]/A3
17	P4[16]/A16		-		-		-

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Ball	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect block.
P0[0]/RD1/ TXD3/SDA1	94[1]	U15[1]	I/O	**P0[0] —** General purpose digital input/output pin.
			I	**RD1 —** CAN1 receiver input (LPC2460 only).
			O	**TXD3 —** Transmitter output for UART3.
			I/O	**SDA1 —** I^2C1 data input/output (this is not an open-drain pin).
P0[1]/TD1/RXD3/ SCL1	96[1]	T14[1]	I/O	**P0[1] —** General purpose digital input/output pin.
			O	**TD1 —** CAN1 transmitter output (LPC2460 only).
			I	**RXD3 —** Receiver input for UART3.
			I/O	**SCL1 —** I^2C1 clock input/output (this is not an open-drain pin).
P0[2]/TXD0	202[1]	C4[1]	I/O	**P0[2] —** General purpose digital input/output pin.
			O	**TXD0 —** Transmitter output for UART0.

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Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[7]/ ENET_COL/ MCIDAT1/ PWM0[5]	153[1]	D14[1]	I/O	**P1[7] —** General purpose digital input/output pin.
			I	**ENET_COL —** Ethernet Collision detect (MII interface) (LPC2460 only).
			I/O	**MCIDAT1 —** Data line 1 for SD/MMC interface.
			O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
P1[8]/ ENET_CRS_DV/ ENET_CRS	190[1]	C7[1]	I/O	**P1[8] —** General purpose digital input/output pin.
			I	**ENET_CRS_DV/ENET_CRS —** Ethernet Carrier Sense/Data Valid (RMII interface)/ Ethernet Carrier Sense (MII interface) (LPC2460 only).
P1[9]/ ENET_RXD0	188[1]	A6[1]	I/O	**P1[9] —** General purpose digital input/output pin.
			I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface) (LPC2460 only).
P1[10]/ ENET_RXD1	186[1]	C8[1]	I/O	**P1[10] —** General purpose digital input/output pin.
			I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface) (LPC2460 only).
P1[11]/ ENET_RXD2/ MCIDAT2/ PWM0[6]	163[1]	A14[1]	I/O	**P1[11] —** General purpose digital input/output pin.
			I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface) (LPC2460 only).
			I/O	**MCIDAT2 —** Data line 2 for SD/MMC interface.
			O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]/ ENET_RXD3/ MCIDAT3/ PCAP0[0]	157[1]	A16[1]	I/O	**P1[12] —** General purpose digital input/output pin.
			I	**ENET_RXD3 —** Ethernet Receive Data (MII interface) (LPC2460 only).
			I/O	**MCIDAT3 —** Data line 3 for SD/MMC interface.
			I	**PCAP0[0] —** Capture input for PWM0, channel 0.
P1[13]/ ENET_RX_DV	147[1]	D16[1]	I/O	**P1[13] —** General purpose digital input/output pin.
			I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface) (LPC2460 only).
P1[14]/ ENET_RX_ER	184[1]	A7[1]	I/O	**P1[14] —** General purpose digital input/output pin.
			I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface) (LPC2460 only).
P1[15]/ ENET_REF_CLK/ ENET_RX_CLK	182[1]	A8[1]	I/O	**P1[15] —** General purpose digital input/output pin.
			I	**ENET_REF_CLK/ENET_RX_CLK —** Ethernet Reference Clock (RMII interface)/ Ethernet Receive Clock (MII interface) (LPC2460 only).
P1[16]/ ENET_MDC	180[1]	D10[1]	I/O	**P1[16] —** General purpose digital input/output pin.
			O	**ENET_MDC —** Ethernet MIIM clock (LPC2460 only).
P1[17]/ ENET_MDIO	178[1]	A9[1]	I/O	**P1[17] —** General purpose digital input/output pin.
			I/O	**ENET_MDIO —** Ethernet MIIM data input and output (LPC2460 only).

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Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[18]/ USB_UP_LED1/ PWM1[1]/ CAP1[0]	66[1]	P7[1]	I/O	**P1[18] —** General purpose digital input/output pin.
			O	**USB_UP_LED1 —** USB port 1 GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled), or when host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when host is enabled and detects activity on the bus.
			O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/ USB_TX_E1/ USB_PPWR1/ CAP1[1]	68[1]	U6[1]	I/O	**P1[19] —** General purpose digital input/output pin.
			O	**USB_TX_E1 —** Transmit Enable signal for USB port 1 (OTG transceiver).
			O	**USB_PPWR1 —** Port Power enable signal for USB port 1.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P1[20]/ USB_TX_DP1/ PWM1[2]/SCK0	70[1]	U7[1]	I/O	**P1[20] —** General purpose digital input/output pin.
			O	**USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver).
			O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
			I/O	**SCK0 —** Serial clock for SSP0.
P1[21]/ USB_TX_DM1/ PWM1[3]/SSEL0	72[1]	R8[1]	I/O	**P1[21] —** General purpose digital input/output pin.
			O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
			O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
			I/O	**SSEL0 —** Slave Select for SSP0.
P1[22]/ USB_RCV1/ USB_PWRD1/ MAT1[0]	74[1]	U8[1]	I/O	**P1[22] —** General purpose digital input/output pin.
			I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
			I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
P1[23]/ USB_RX_DP1/ PWM1[4]/MISO0	76[1]	P9[1]	I/O	**P1[23] —** General purpose digital input/output pin.
			I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
			O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
			I/O	**MISO0 —** Master In Slave Out for SSP0.
P1[24]/ USB_RX_DM1/ PWM1[5]/MOSI0	78[1]	T9[1]	I/O	**P1[24] —** General purpose digital input/output pin.
			I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
			O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
			I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/ USB_LS1/ USB_HSTEN1/ MAT1[1]	80[1]	T10[1]	I/O	**P1[25] —** General purpose digital input/output pin.
			O	**USB_LS1 —** Low-speed status for USB port 1 (OTG transceiver).
			O	**USB_HSTEN1 —** Host Enabled status for USB port 1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.

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Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P1[26]/ USB_SSPND1/ PWM1[6]/ CAP0[0]	82[1]	R10[1]	I/O	**P1[26] —** General purpose digital input/output pin.
			O	**USB_SSPND1 —** USB port 1 Bus Suspend status (OTG transceiver).
			O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/ USB_INT1/ USB_OVRCR1/ CAP0[1]	88[1]	T12[1]	I/O	**P1[27] —** General purpose digital input/output pin.
			I	**USB_INT1 —** USB port 1 OTG transceiver interrupt (OTG transceiver).
			I	**USB_OVRCR1 —** USB port 1 Over-Current status.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/ USB_SCL1/ PCAP1[0]/ MAT0[0]	90[1]	T13[1]	I/O	**P1[28] —** General purpose digital input/output pin.
			I/O	**USB_SCL1 —** USB port 1 I^2C-bus serial clock (OTG transceiver).
			I	**PCAP1[0] —** Capture input for PWM1, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/ USB_SDA1/ PCAP1[1]/ MAT0[1]	92[1]	U14[1]	I/O	**P1[29] —** General purpose digital input/output pin.
			I/O	**USB_SDA1 —** USB port 1 I^2C-bus serial data (OTG transceiver).
			I	**PCAP1[1] —** Capture input for PWM1, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 0.
P1[30]/ USB_PWRD2/ V_{BUS}/AD0[4]	42[2]	P2[2]	I/O	**P1[30] —** General purpose digital input/output pin.
			I	**USB_PWRD2 —** Power Status for USB port 2.
			I	**V_{BUS} —** Monitors the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
			I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/ USB_OVRCR2/ SCK1/AD0[5]	40[2]	P1[2]	I/O	**P1[31] —** General purpose digital input/output pin.
			I	**USB_OVRCR2 —** Over-Current status for USB port 2.
			I/O	**SCK1 —** Serial Clock for SSP1.
			I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]			I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect block.
P2[0]/PWM1[1]/ TXD1/ TRACECLK	154[1]	B17[1]	I/O	**P2[0] —** General purpose digital input/output pin.
			O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
			O	**TXD1 —** Transmitter output for UART1.
			O	**TRACECLK —** Trace Clock.
P2[1]/PWM1[2]/ RXD1/ PIPESTAT0	152[1]	E14[1]	I/O	**P2[1] —** General purpose digital input/output pin.
			O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
			I	**RXD1 —** Receiver input for UART1.
			O	**PIPESTAT0 —** Pipeline Status, bit 0.
P2[2]/PWM1[3]/ CTS1/ PIPESTAT1	150[1]	D15[1]	I/O	**P2[2] —** General purpose digital input/output pin.
			O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
			I	**CTS1 —** Clear to Send input for UART1.
			O	**PIPESTAT1 —** Pipeline Status, bit 1.

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Table 4. Pin description *…continued*

Symbol	Pin	Ball	Type	Description
P4[17]/A17	104[1]	P14[1]	I/O	**P4[17] —** General purpose digital input/output pin.
			I/O	**A17 —** External memory address line 17.
P4[18]/A18	105[1]	P15[1]	I/O	**P4[18] —** General purpose digital input/output pin.
			I/O	**A18 —** External memory address line 18.
P4[19]/A19	111[1]	P16[1]	I/O	**P4[19] —** General purpose digital input/output pin.
			I/O	**A19 —** External memory address line 19.
P4[20]/A20/ SDA2/SCK1	109[1]	R17[1]	I/O	**P4[20] —** General purpose digital input/output pin.
			I/O	**A20 —** External memory address line 20.
			I/O	**SDA2 —** I^2C2 data input/output (this is not an open-drain pin).
			I/O	**SCK1 —** Serial Clock for SSP1.
P4[21]/A21/ SCL2/SSEL1	115[1]	M15[1]	I/O	**P4[21] —** General purpose digital input/output pin.
			I/O	**A21 —** External memory address line 21.
			I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
			I/O	**SSEL1 —** Slave Select for SSP1.
P4[22]/A22/ TXD2/MISO1	123[1]	K14[1]	I/O	**P4[22] —** General purpose digital input/output pin.
			I/O	**A22 —** External memory address line 22.
			O	**TXD2 —** Transmitter output for UART2.
			I/O	**MISO1 —** Master In Slave Out for SSP1.
P4[23]/A23/ RXD2/MOSI1	129[1]	J15[1]	I/O	**P4[23] —** General purpose digital input/output pin.
			I/O	**A23 —** External memory address line 23.
			I	**RXD2 —** Receiver input for UART2.
			I/O	**MOSI1 —** Master Out Slave In for SSP1.
P4[24]/$\overline{OE}$	183[1]	B8[1]	I/O	**P4[24] —** General purpose digital input/output pin.
			O	**$\overline{OE}$ —** LOW active Output Enable signal.
P4[25]/$\overline{WE}$	179[1]	B9[1]	I/O	**P4[25] —** General purpose digital input/output pin.
			O	**$\overline{WE}$ —** LOW active Write Enable signal.
P4[26]/$\overline{BLS0}$	119[1]	L15[1]	I/O	**P4[26] —** General purpose digital input/output pin.
			O	**$\overline{BLS0}$ —** LOW active Byte Lane select signal 0.
P4[27]/$\overline{BLS1}$	139[1]	G15[1]	I/O	**P4[27] —** General purpose digital input/output pin.
			O	**$\overline{BLS1}$ —** LOW active Byte Lane select signal 1.
P4[28]/$\overline{BLS2}$/ MAT2[0]/TXD3	170[1]	C11[1]	I/O	**P4 [28] —** General purpose digital input/output pin.
			O	**$\overline{BLS2}$ —** LOW active Byte Lane select signal 2.
			O	**MAT2[0] —** Match output for Timer 2, channel 0.
			O	**TXD3 —** Transmitter output for UART3.
P4[29]/$\overline{BLS3}$/ MAT2[1]/RXD3	176[1]	B10[1]	I/O	**P4[29] —** General purpose digital input/output pin.
			O	**$\overline{BLS3}$ —** LOW active Byte Lane select signal 3.
			O	**MAT2[1] —** Match output for Timer 2, channel 1.
			I	**RXD3 —** Receiver input for UART3.
P4[30]/$\overline{CS0}$	187[1]	B7[1]	I/O	**P4[30] —** General purpose digital input/output pin.
			O	**$\overline{CS0}$ —** LOW active Chip Select 0 signal.

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- Asynchronous page mode read
- Programmable Wait States
- Bus turnaround delay
- Output enable and write enable delays
- Extended wait

- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048, 4096, and 8192 row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.7 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected LPC2420/2460 peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master.

7.7.1 Features

- Two DMA channels. Each channel can support a unidirectional transfer.
- The GPDMA can transfer data between the 16 kB SRAM, external memory, and peripherals such as the SD/MMC, two SSPs, and the I^2S interface.
- Single DMA and burst DMA request signals. Each peripheral connected to the GPDMA can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the GPDMA.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 1 has the lowest priority. If requests from two channels become active at the same time, the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. The GPDMA is programmed by writing to the DMA control registers over the AHB slave interface.

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7.10.2.1 Features

- OHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

7.10.3 USB OTG controller

USB OTG is a supplement to the *USB 2.0 specification* that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG controller integrates the host controller, device controller, and a master-only I^2C-bus interface to implement OTG dual-role device functionality. The dedicated I^2C-bus interface controls an external OTG transceiver.

7.10.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

7.11 CAN controller and acceptance filters (LPC2460 only)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.11.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.

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The VBAT pin supplies power only to the RTC and the Battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that can be used by external hardware to restore chip power and resume operation.

7.23.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- An alarm output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC and Battery RAM.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values. This enhancement enables the RTC to be used as a System Timer.
- 2 kB data SRAM powered by VBAT.
- RTC and Battery RAM power supply is isolated from the rest of the chip.

7.24 Clocking and power control

7.24.1 Crystal oscillators

The LPC2420/2460 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2420/2460 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.24.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy.

Upon power-up or any chip reset, the LPC2420/2460 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.24.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The

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8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	core and external rail		3.0	3.6	V
$V_{DD(DCDC)(3V3)}$	DC-to-DC converter supply voltage (3.3 V)			3.0	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			−0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		−0.5	+4.6	V
$V_{i(VREF)}$	input voltage on pin VREF			−0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		−0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(3V3)}$ supply voltage is present	[2]	−0.5	+6.0	V
		other I/O pins	[2][3]	−0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin	[4]	-	100	mA
I_{SS}	ground current	per ground pin	[4]	-	100	mA
T_{stg}	storage temperature	non-operating	[5]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[6]	−2500	+2500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SSIO}/V_{SSCORE} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 7. Thermal characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 8. Thermal resistance value (C/W): ±15 %

V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

LQFP208		**TFBGA208**	
θja		**θja**	
JEDEC (4.5 in × 4 in)		**JEDEC (4.5 in × 4 in)**	
0 m/s	27.4	0 m/s	41
1 m/s	25.7	1 m/s	35
2.5 m/s	24.4	2.5 m/s	31
Single-layer (4.5 in × 3 in)		**8-layer (4.5 in × 3 in)**	
0 m/s	35.4	0 m/s	34.9
1 m/s	31.2	1 m/s	30.9
2.5 m/s	29.2	2.5 m/s	28
θjc	8.8	θjc	8.3
θjb	15.4	θjb	13.6

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11. Dynamic characteristics

Table 10. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
I^2C-bus pins (P0[27] and P0[28])						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns
SSP interface						
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 17	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

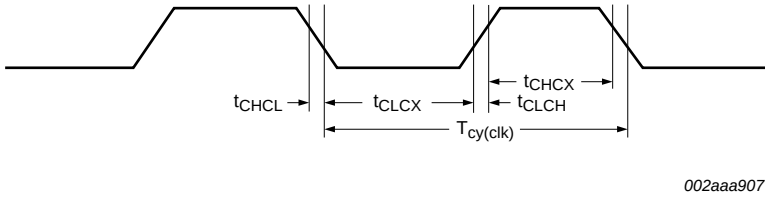

Fig 13. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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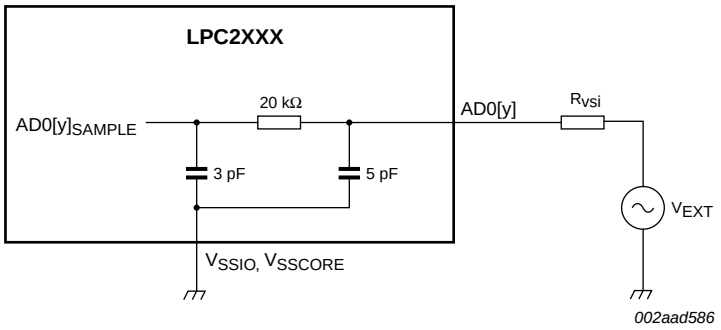

Fig 20. Suggested ADC interface - LPC2420/2460 AD0[y] pin

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14.2 Suggested USB interface solutions

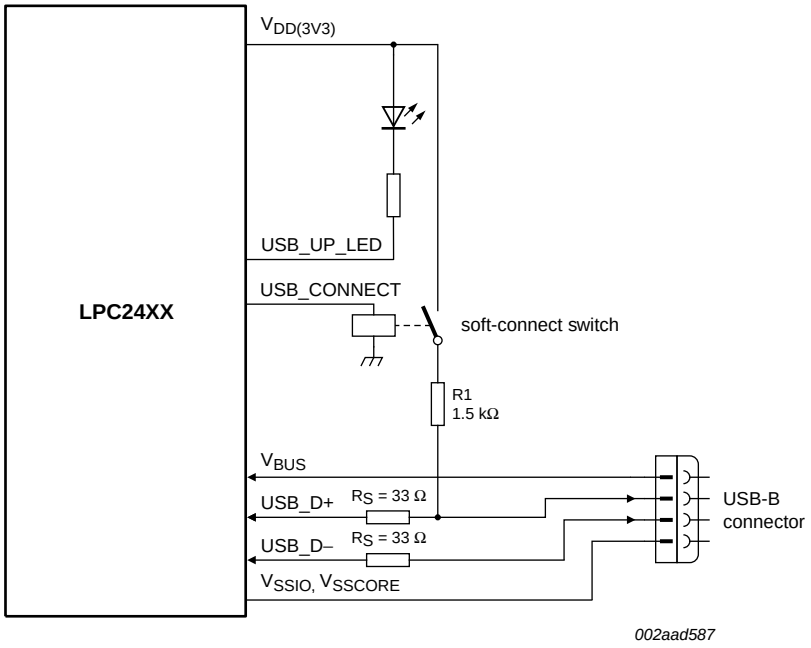

Fig 23. LPC2420/2460 USB interface on a self-powered device

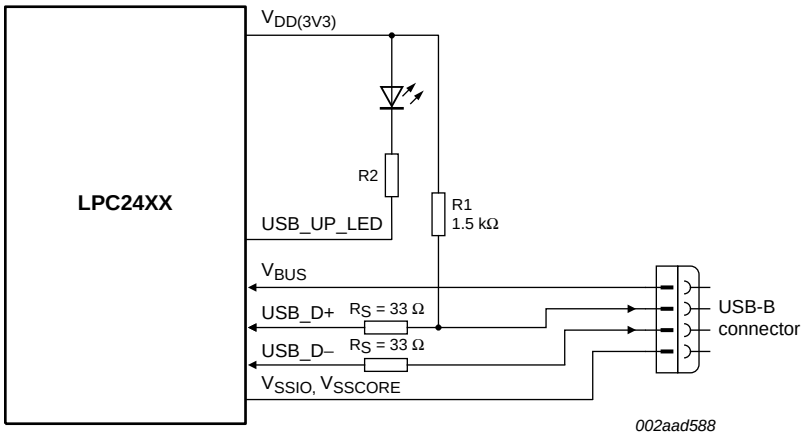

Fig 24. LPC2420/2460 USB interface on a bus-powered device

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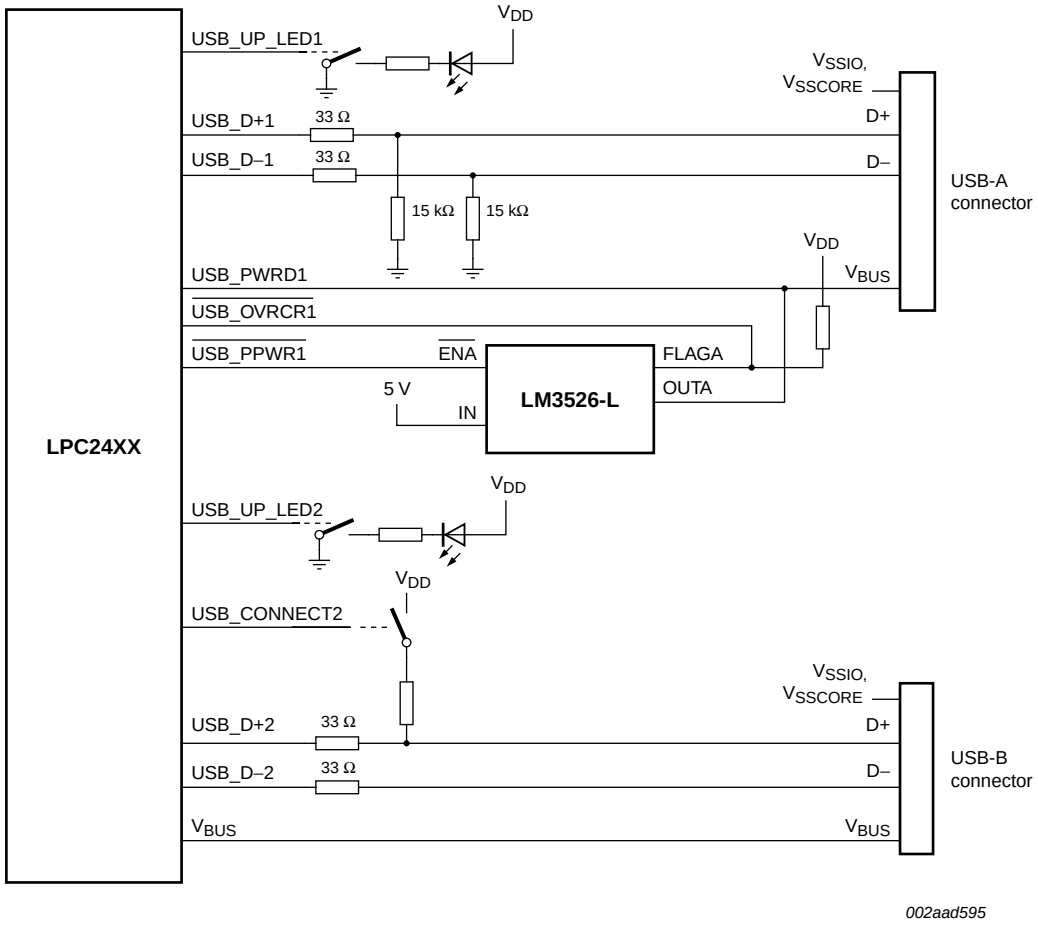

Fig 27. LPC2420/2460 USB OTG port configuration: USB port 2 device, USB port 1 host

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Table 20. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.4 RTC 32 kHz oscillator component selection

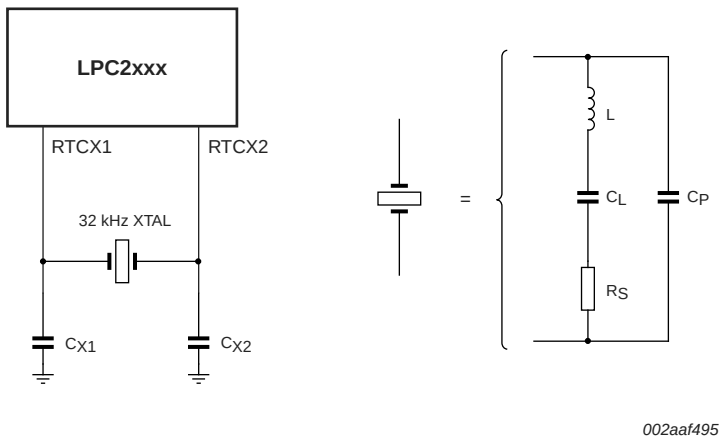

Fig 31. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 31. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 21 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 21 that belong to a specific C_L. The value of external capacitances C_{X1} and C_{X2} specified in this table are calculated from the internal parasitic capacitances and the C_L. Parasitics from PCB and package are not taken into account.

Table 21. Recommended values for the RTC external 32 kHz oscillator C_{X1}/C_{X2} components

Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
11 pF	< 100 kΩ	18 pF, 18 pF
13 pF	< 100 kΩ	22 pF, 22 pF
15 pF	< 100 kΩ	27 pF, 27 pF

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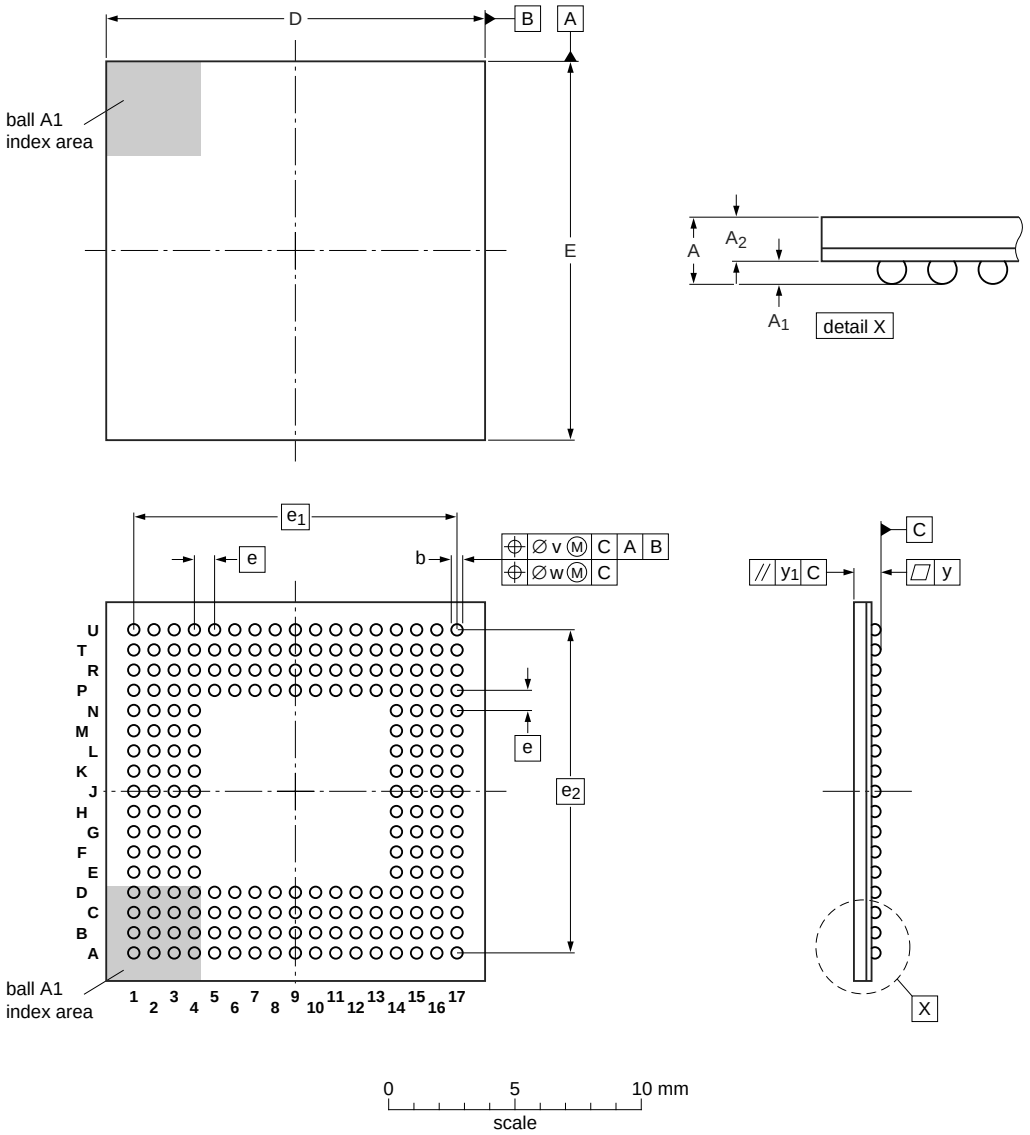
TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 35. Package outline SOT950-1 (TFBGA208)

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Table 23. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2420_60 v.6	20110823	Product data sheet	-	LPC2420_60 v.5
Modifications:	• Table 4 “Pin description”: Updated description for USB_UP_LED1 and USB_UP_LED2. • Table 4 “Pin description”: Added Table note 8 for DBGEN, TMS, TDI, $\overline{\text{TRST}}$, and RTCK pins. • Table 4 “Pin description”: Added Table note 9 for TCK and TDO pins. • Table 4 “Pin description”: Added Table note 11 for XTAL1 and XTAL2 pins. • Table 4 “Pin description”: Added Table note 12 for RTCX1 and RTCX2 pins. • Table 6 “Limiting values”: Added “non-operating” to conditions of storage spec. • Table 6 “Limiting values”: Updated Table note [5]. • Added Table 8 “Thermal resistance value (C/W): ±15 %”. • Table 9 “Static characteristics”: Removed R_{pu}. • Table 9 “Static characteristics”: Changed V_{hys} Typ value of I^2C-bus pins to $0.05V_{DD(3V3)}$. • Added Table 11 “Dynamic characteristic: internal oscillators”. • Added Table 12 “Dynamic characteristic: I/O pins[1]”. • Table 14 “Dynamic characteristics: Static external memory interface”: Updated min, typical and max values for $t_{h(D)}$. • Table 14 “Dynamic characteristics: Static external memory interface”: Updated min, typical and max values for t_{WEHDNV}. • Table 14 “Dynamic characteristics: Static external memory interface”: Removed “AHB clock = 1 MHz”. • Table 14 “Dynamic characteristics: Static external memory interface”: Swapped current min and max values for t_{am}. • Table 15 “Dynamic characteristics: Dynamic external memory interface”: Added Table note 1. • Table 15 “Dynamic characteristics: Dynamic external memory interface”: Removed “AHB clock = 1 MHz”. • Added Table 16 “Dynamic characteristics: Dynamic external memory interface”. • Added Section 10.3 “Electrical pin characteristics”. • Added Section 14.3 “Crystal oscillator XTAL input and component selection”. • Added Section 14.4 “RTC 32 kHz oscillator component selection”. • Updated Section 14.5 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Added Section 14.6 “Standard I/O pin configuration” • Added Section 14.7 “Reset pin configuration” • Moved Figure 13 “External clock timing (with an amplitude of at least Vi(RMS) = 200 mV)” to below Table 10 “Dynamic characteristics”. • Updated Figure 19 “ADC characteristics”.			
LPC2420_60 v.5	20100224	Preliminary data sheet	-	LPC2420_60 v.4
Modifications:	• Table 9: Merged power-down mode information into one table. • Table 9: Changed typical values from 19 to 20 for $I_{DD(DCDC)dpd(3V3)}$, I_{BATact}, and I_{BAT}. • Added Table 16 “Dynamic characteristics: Dynamic external memory interface”. • Added Table 18 “DAC electrical characteristics”.			
LPC2420_60 v.4	20091015	Preliminary data sheet	-	LPC2420_60 v.3

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