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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	DSI, Ethernet, RS-232
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc8126mp8000

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Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Table 3. Buses and Memory Controller

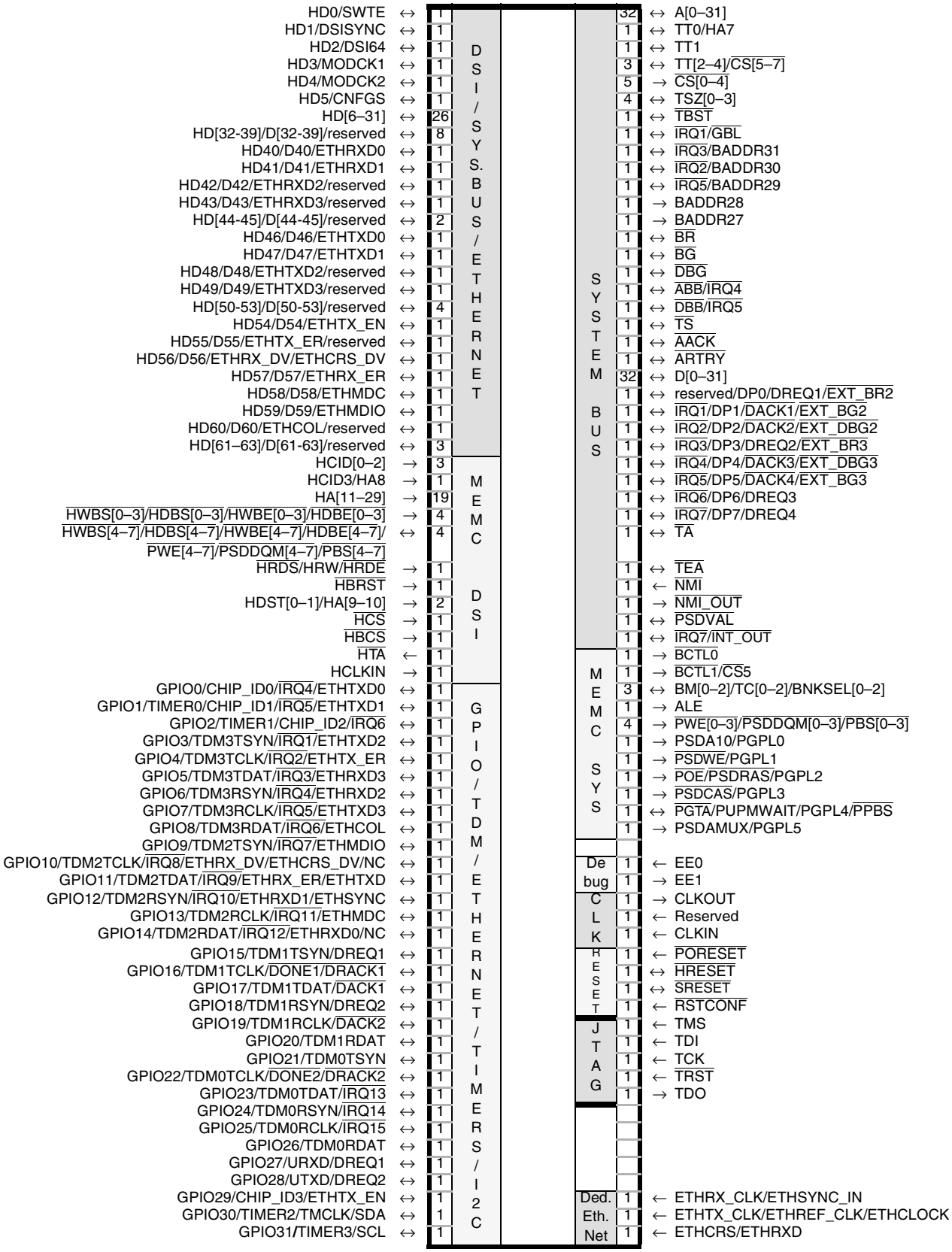
Feature	Description
60x-Compatible System Bus	• 64/32-bit data and 32-bit address 60x bus. • Support for multiple-master designs. • Four-beat burst transfers (eight-beat in 32-bit wide mode). • Port size of 64, 32, 16, and 8 controlled by the internal memory controller. • Bus can access external memory expansion or off-device peripherals, or it can enable an external host device to access internal resources. • Slave support, direct access by an external host to internal resources including the M1 and M2 memories. • On-device arbitration between up to four master devices.
Direct Slave Interface (DSI)	A 32/64-bit wide slave host interface that operates only as a slave device under the control of an external host processor. • 21–25 bit address, 32/64-bit data. • Direct access by an external host to internal and external resources, including the M1 and the M2 memories as well as external devices on the system bus. • Synchronous and asynchronous accesses, with burst capability in the synchronous mode. • Dual or single-strobe modes. • Write and read buffers improve host bandwidth. • Byte enable signals enables 1, 2, 4, and 8 byte write access granularity. • Sliding window mode enables access with reduced number of address pins. • Chip ID decoding enables using one $\overline{CS}$ signal for multiple DSPs. • Broadcast $\overline{CS}$ signal enables parallel write to multiple DSPs. • Big-endian, little-endian, and munged little-endian support.
3-Mode Signal Multiplexing	• 64-bit DSI, 32-bit system bus. • 32-bit DSI, 64-bit system bus. • 32-bit DSI, 32-bit system bus.
Memory Controller	Flexible eight-bank memory controller: • Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine. • Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash memory, and other user-definable peripherals. • Byte enables for either 64-bit or 32-bit bus width mode. • Eight external memory banks (banks 0–7). Two additional memory banks (banks 9, 11) control IPBus peripherals and internal memories. Each bank has the following features: —32-bit address decoding with programmable mask. —Variable block sizes (32 KB to 4 GB). —Selectable memory controller machine. —Two types of data errors check/correction: normal odd/even parity and read-modify-write (RMW) odd/even parity for single accesses. —Write-protection capability. —Control signal generation machine selection on a per-bank basis. —Support for internal or external masters on the system bus. —Data buffer controls activated on a per-bank basis. —Atomic operation. —RMW data parity check (on system bus only). —Extensive external memory-controller/bus-slave support. —Parity byte select pin, which enables a fast, glueless connection to RMW-parity devices (on the system bus only). —Data pipeline to reduce data set-up time for synchronous devices.

Table 8. Power and Packaging

Feature	Description
Reduced Power Dissipation	• Low-power CMOS design. • Separate power supply for internal logic (1.2 V for 400 MHz or 500 MHz) and I/O (3.3 V). • Low-power standby modes. • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).
Packaging	• 0.8 mm pitch Flip-Chip Plastic Ball-Grid Array (FC-PBGA). • 431-connection (ball). • 20 mm × 20 mm.

Table 9. Software Support

Feature	Description
Real-Time Operating System (RTOS)	The real-time operating system (RTOS) fully supports device architecture (multi-core, memory hierarchy, ICache, timers, DMA controller, interrupts, peripherals), as follows: • High-performance and deterministic, delivering predictive response time. • Optimized to provide low interrupt latency with high data throughput. • Preemptive and priority-based multitasking. • Fully interrupt/event driven. • Small memory footprint. • Comprehensive set of APIs.
Multi-Core Support	• One instance of kernel code in all four SC140 cores. • Dynamic and static memory allocation from local memory (M1) and shared memory (M2).
Distributed System Support	Transparent inter-task communications between tasks running inside the SC140 cores and the other tasks running in on-board devices or remote network devices: • Messaging mechanism between tasks using mailboxes and semaphores. • Networking support; data transfer between tasks running inside and outside the device using networking protocols. • Includes integrated device drivers for such peripherals as TDM, UART, and external buses.
Software Support	• Task debugging utilities integrated with compilers and vendors. • Board support package (BSP) for the application development system (ADS). • Integrated development environment (IDE): —C/C++ compiler with in-line assembly so developers can generate highly optimized DSP code. Translates C/C++ code into parallel fetch sets and maintains high code density. —Librarian. User can create libraries for modularity. —A collection of C/C++ functions for developer use. —Highly efficient linker to produce executables from object code. —Seamlessly integrated real-time, non-intrusive multi-mode debugger for debugging highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. —Device simulation models enable design and simulation before hardware availability. —Profiler using a patented binary code instrumentation (BCI) technique helps developers identify program design inefficiencies. —Version control. Metrowerks® CodeWarrior® includes plug-ins for ClearCase, Visual SourceSafe, and CVS.
Boot Options	• External memory. • External host. • UART. • TDM. • I^2C



Power signals are: V_{DD}, V_{DDH}, V_{CCSYN}, GND, GND_H, and GND_{SYN}. Reserved signals can be left unconnected. NC signals must not be connected.

Figure 1-1. MSC8126 External Signals

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD46	Input/ Output	**Host Data Bus 46** Bit 46 of the DSI data bus.
D46	Input/ Output	**System Bus Data 46** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD0	Output	**Ethernet Transmit Data 0** In MII and RMII modes, bit 0 of the Ethernet transmit data.
HD47	Input/ Output	**Host Data Bus 47** Bit 47 of the DSI data bus.
D47	Input/ Output	**System Bus Data 47** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD1	Output	**Ethernet Transmit Data 1** In MII and RMII modes, bit 1 of the Ethernet transmit data.
HD48	Input/ Output	**Host Data Bus 48** Bit 48 of the DSI data bus.
D48	Input/ Output	**System Bus Data 48** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD2	Output	**Ethernet Transmit Data 2** In MII mode only, bit 2 of the Ethernet transmit data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD49	Input/ Output	**Host Data Bus 49** Bit 49 of the DSI data bus.
D49	Input/ Output	**System Bus Data 49** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD3	Output	**Ethernet Transmit Data 3** In MII mode only, bit 3 of the Ethernet transmit data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD[50–53]	Input/ Output	**Host Data Bus 50–53** Bits 50–53 of the DSI data bus.
D[50–53]	Input/ Output	**System Bus Data 50–53** For write transactions, the bus master drives valid data on this bus. For read transactions, the slave drives valid data on this bus.
Reserved	Input	If the Ethernet port is enabled and multiplexed with the DSI/System bus, these signals are reserved and can be left unconnected.
HD54	Input/ Output	**Host Data Bus 54** Bit 54 of the DSI data bus.
D54	Input/ Output	**System Bus Data 54** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTX_EN	Output	**Ethernet Transmit Data Enable** In MII and RMII modes, indicates that the transmit data is valid.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD55	Input/ Output	**Host Data Bus 55** Bit 55 of the DSI data bus.
D55	Input/ Output	**System Bus Data 55** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTX_ER	Output	**Ethernet Transmit Data Error** In MII mode only, indicates a transmit data error.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD56	Input/ Output	**Host Data Bus 56** Bit 56 of the DSI data bus.
D56	Input/ Output	**System Bus Data 56** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRX_DV	Input	**Ethernet Receive Data Valid** Indicates that the receive data is valid.
ETHCRS_DV	Input	**Ethernet Carrier Sense/Receive Data Valid** In RMII mode, indicates that a carrier is detected and after the connection is established that the receive data is valid.
HD57	Input/ Output	**Host Data Bus 57** Bit 57 of the DSI data bus.
D57	Input/ Output	**System Bus Data 57** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRX_ER	Input	**Ethernet Receive Data Error** In MII and RMII modes, indicates a receive data error.
HD58	Input/ Output	**Host Data Bus 58** Bit 58 of the DSI data bus.
D58	Input/ Output	**System Bus Data 58** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHMDC	Output	**Ethernet Management Clock** In MII and RMII modes, used for the MDIO reference clock.
HD59	Input/ Output	**Host Data Bus 59** Bit 59 of the DSI data bus.
D59	Input/ Output	**System Bus Data 59** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHMDIO	Input/ Output	**Ethernet Management Data** In MII and RMII modes, used for station management data input/output.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD60	Input/ Output	**Host Data Bus 60** Bit 60 of the DSI data bus.
D60	Input/ Output	**System Bus Data 60** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHCOL	Input/ Output	**Ethernet Collision** In MII mode only, indicates that a collision was detected.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD[61–63]	Input/ Output	**Host Data Bus 61–63** Bits 61–63 of the DSI data bus.
D[61–63]	Input/ Output	**System Bus Data 61–63** For write transactions, the bus master drives valid data on this bus. For read transactions, the slave drives valid data on this bus.
Reserved	Input	If the Ethernet port is enabled and multiplexed with the DSI/System bus, these signals are reserved and can be left unconnected.
HCID[0–2]	Input	**Host Chip ID 0–2** With HCID3, carries the chip ID of the DSI. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID, or if $\overline{\text{HBCS}}$ is asserted.
HCID3	Input	**Host Chip ID 3** With HCI[0–2], carries the chip ID of the DSI. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID, or if $\overline{\text{HBCS}}$ is asserted.
HA8	Input	**Host Bus Address 8** Used by an external host to access the internal address space.
HA[11–29]	Input	**Host Bus Address 11–29** Used by external host to access the internal address space.
$\overline{\text{HWBS[0–3]}}$	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
$\overline{\text{HDBS[0–3]}}$	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
$\overline{\text{HWBE[0–3]}}$	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host read or write accesses.
$\overline{\text{HDBE[0–3]}}$	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host write accesses

1.6 GPIO, TDM, UART, and Timer Signals

The general-purpose input/output (GPIO), time-division multiplexed (TDM), universal asynchronous receiver/transmitter (UART), and timer signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. **Table 1-7** describes the signals in this group.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals

Signal Name	Type	Description
GPIO0	Input/ Output	**General-Purpose Input Output 0** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
CHIP_ID0	Input	**Chip ID 0** Determines the chip ID of the MSC8126 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTXD0	Output	**Ethernet Transmit Data 0** For MII or RMII mode, bit 0 of the Ethernet transmit data.
GPIO1	Input/ Output	**General-Purpose Input Output 1** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
TIMER0	Input/ Output	**Timer 0** Each signal is configured as either input to or output from the counter. See the *MSC8126 Reference Manual* for configuration details.
CHIP_ID1	Input	**Chip ID 1** Determines the chip ID of the MSC8126 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of the fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTXD1	Output	**Ethernet Transmit Data 1** For MII or RMII mode, bit 1 of the Ethernet transmit data.
GPIO2	Input/ Output	**General-Purpose Input Output 2** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual*.
TIMER1	Input/ Output	**Timer 1** Each signal is configured as either input to or output from the counter. For the configuration of the signal direction, refer to the *MSC8126 Reference Manual*.
CHIP_ID2	Input	**Chip ID 2** Determines the chip ID of the MSC8126 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of the fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO18	Input/ Output	**General-Purpose Input Output 18** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RSYN	Input/ Output	**TDM1 Receive Frame Sync** The receive sync signal for TDM 1. As an input, this can be the DATA_B data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual*.
DREQ2	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
GPIO19	Input/ Output	**General-Purpose Input Output 19** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RCLK	Input/ Output	**TDM1 Receive Clock** The receive clock signal for TDM 1. As an input, this can be the DATA_C data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{DACK2}}$	Output	**DMA Acknowledge 2** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
GPIO20	Input/ Output	**General-Purpose Input Output 20** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RDAT	Input/ Output	**TDM1 Serial Receiver Data** The receive data signal for TDM 1. As an input, this can be the DATA_A data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual*.
GPIO21	Input/ Output	**General-Purpose Input Output 21** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TSYN	Input/ Output	**TDM0 Transmit frame Sync** Transmit Frame Sync for TDM 0.
GPIO22	Input/ Output	**General-Purpose Input Output 22** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TCLK	Input	**TDM 0 Transmit Clock** Transmit Clock for TDM 0.
$\overline{\text{DONE2}}$	Input/ Output	**DMA Done 2** Signifies that the channel must be terminated. If the DMA generates DONE, the channel handling this peripheral is inactive. As an input to the DMA, DONE closes the channel much like a normal channel closing. **Note:** See the *MSC8126 Reference Manual* chapters on DMA and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and signal direction.
$\overline{\text{DRACK2}}$	Output	**DMA Data Request Acknowledge 2** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO23	Input/ Output	**General-Purpose Input Output 23** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TDAT	Input/ Output	**TDM0 Serial Transmitter Data** The transmit data signal for TDM 0. As an output, this can be the DATA_D data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ13}}$	Input	**Interrupt Request 13** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO24	Input/ Output	**General-Purpose Input Output 24** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0RSYN	Input/ Output	**TDM0 Receive Frame Sync** The receive sync signal for TDM 0. As an input, this can be the DATA_B data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ14}}$	Input	**Interrupt Request 14** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO25	Input/ Output	**General-Purpose Input Output 25** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0RCLK	Input/ Output	**TDM0 Receive Clock** The receive clock signal for TDM 0. As an input, this can be the DATA_C data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ15}}$	Input	**Interrupt Request 15** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO26	Input/ Output	**General-Purpose Input Output 26** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0RDAT	Input/ Output	**TDM0 Serial Receiver Data** The receive data signal for TDM 0. As an input, this can be the DATA_A data signal for TDM 0. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
GPIO27	Input/ Output	**General-Purpose Input Output 27** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
URXD	Input	**UART Receive Data**
GPIO28	Input/ Output	**General-Purpose Input Output 28** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
DREQ2	Input	**DMA Request 2** Used by an external peripheral to request DMA service.
UTXD	Output	**UART Transmit Data**

2.5.1 Output Buffer Impedances

Table 2-5. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	50
Memory controller	50
Parallel I/O	50
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8126 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 2-10** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DD} levels and then the V_{DDH} levels (see **Figure 2-3**).
- CLKIN should start toggling at least 16 cycles (starting after V_{DDH} reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 2-2** and **Figure 2-3**).
- CLKIN must not be pulled high during V_{DDH} power-up. CLKIN can toggle during this period.

The following figures show acceptable start-up sequence examples. **Figure 2-2** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 2-3** shows a sequence in which V_{DDH} is raised after V_{DD} and CLKIN begins to toggle as V_{DDH} rises.

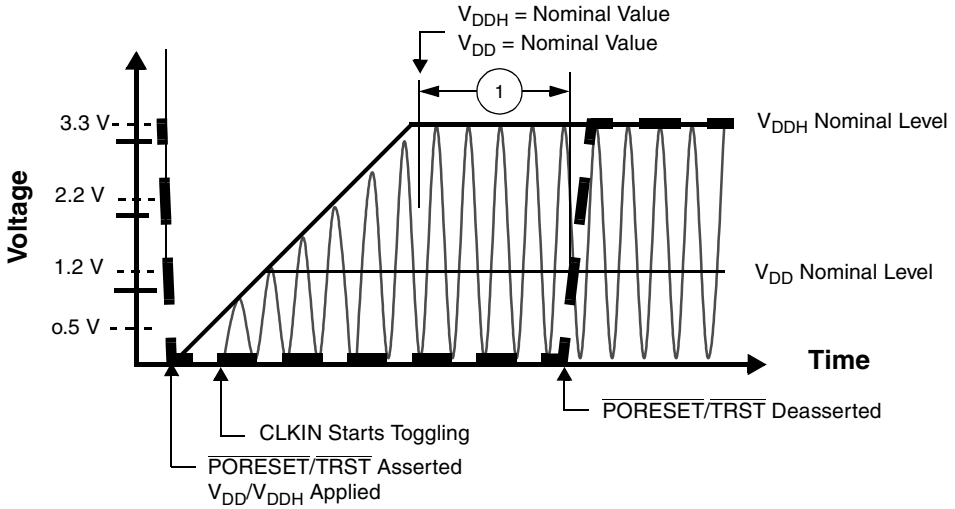


Figure 2-2. Start-Up Sequence with V_{DD} and V_{DDH} Raised Together

2.5.5 System Bus Access Timing

2.5.5.1 Core Data Transfers

Generally, all MSC8126 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2-12** shows.

Table 2-12. Tick Spacing for Memory Controller Signals

BCLK/SC140 clock	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:4, 1:6, 1:8, 1:10	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:3	1/6 REFCLK	1/2 REFCLK	4/6 REFCLK
1:5	2/10 REFCLK	1/2 REFCLK	7/10 REFCLK

Figure 2-5 is a graphical representation of **Table 2-12**.

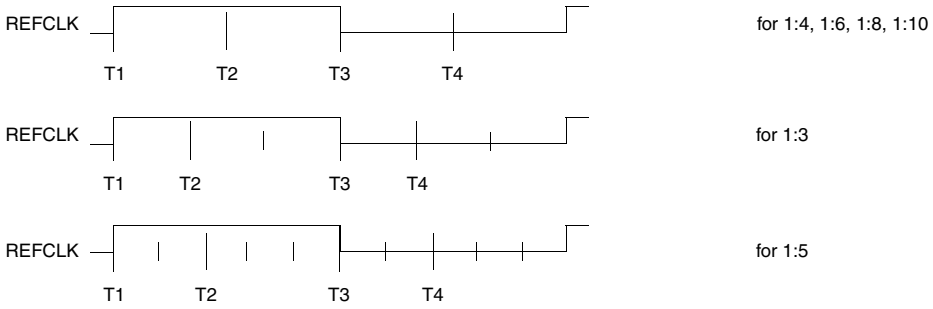


Figure 2-5. Internal Tick Spacing for Memory Controller Signals

2.5.6.2 DSI Synchronous Mode

Table 2-18. DSI Inputs—Synchronous Mode

No.	Characteristic	Expression	Min	Max	Units
120	HCLKIN Cycle Time[1, 2]	HTC	10.0	55.6	ns
121	HCLKIN high Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
122	HCLKIN low Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.4	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes: **1.** Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 2-6** for HCLKIN frequency limits.

Table 2-19. DSI Outputs—Synchronous Mode

No.	Characteristic	Min	Max	Units
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	6.3	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	7.6	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.0	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	5.9	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	6.3	ns

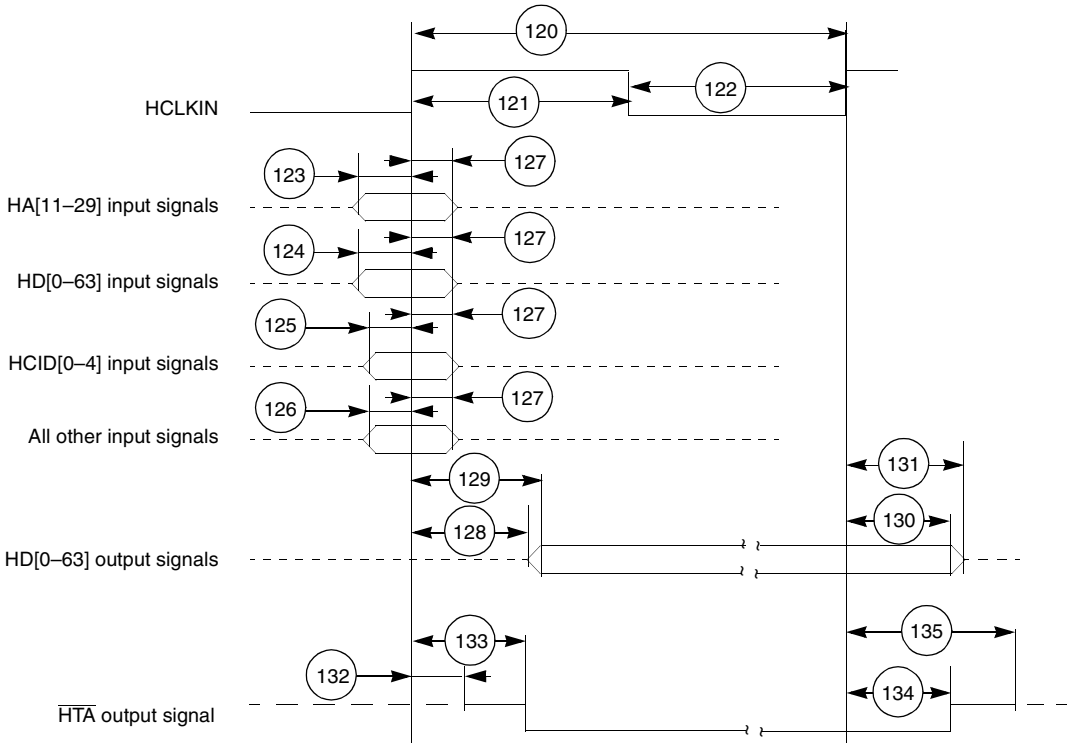


Figure 2-12. DSI Synchronous Mode Signals Timing Diagram

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 2-23. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

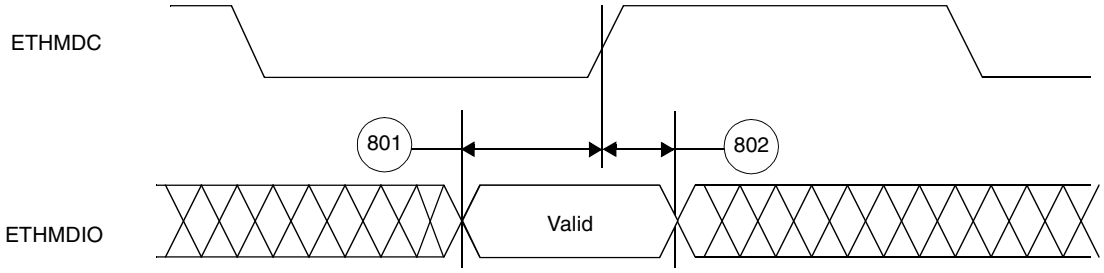


Figure 2-18. MDIO Timing Relationship to MDC

2.5.10.2 MII Mode Timing

Table 2-24. MII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay	1	12.6	ns

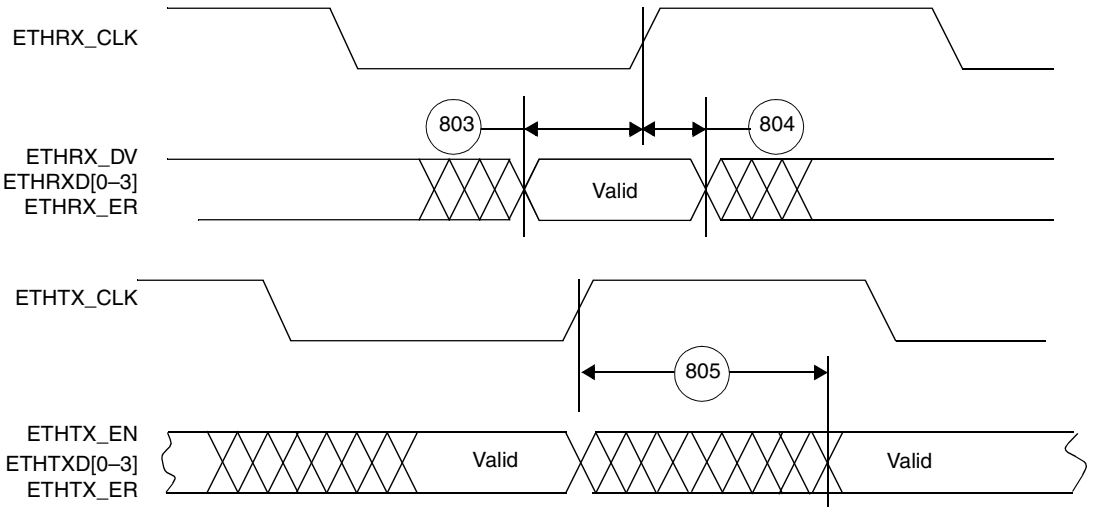


Figure 2-19. MII Mode Signal Timing

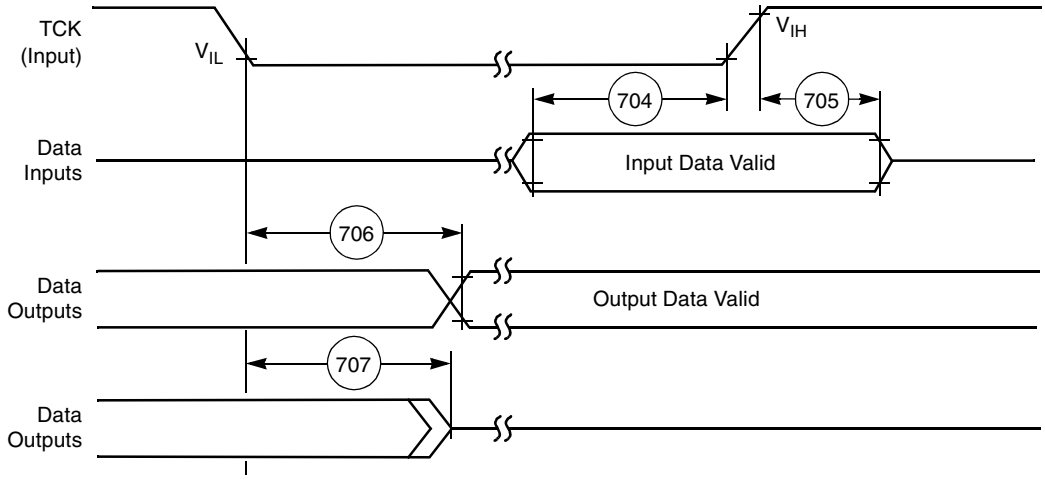


Figure 2-25. Boundary Scan (JTAG) Timing Diagram

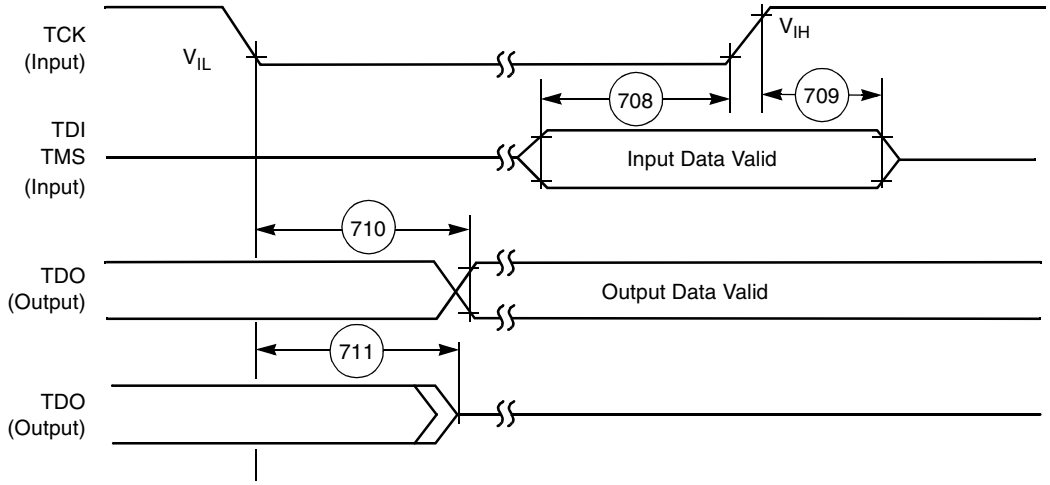


Figure 2-26. Test Access Port Timing Diagram

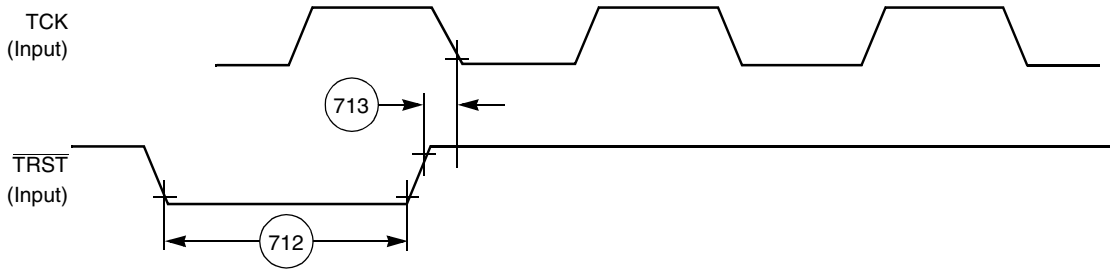


Figure 2-27. $\overline{TRST}$ Timing Diagram

Bottom View

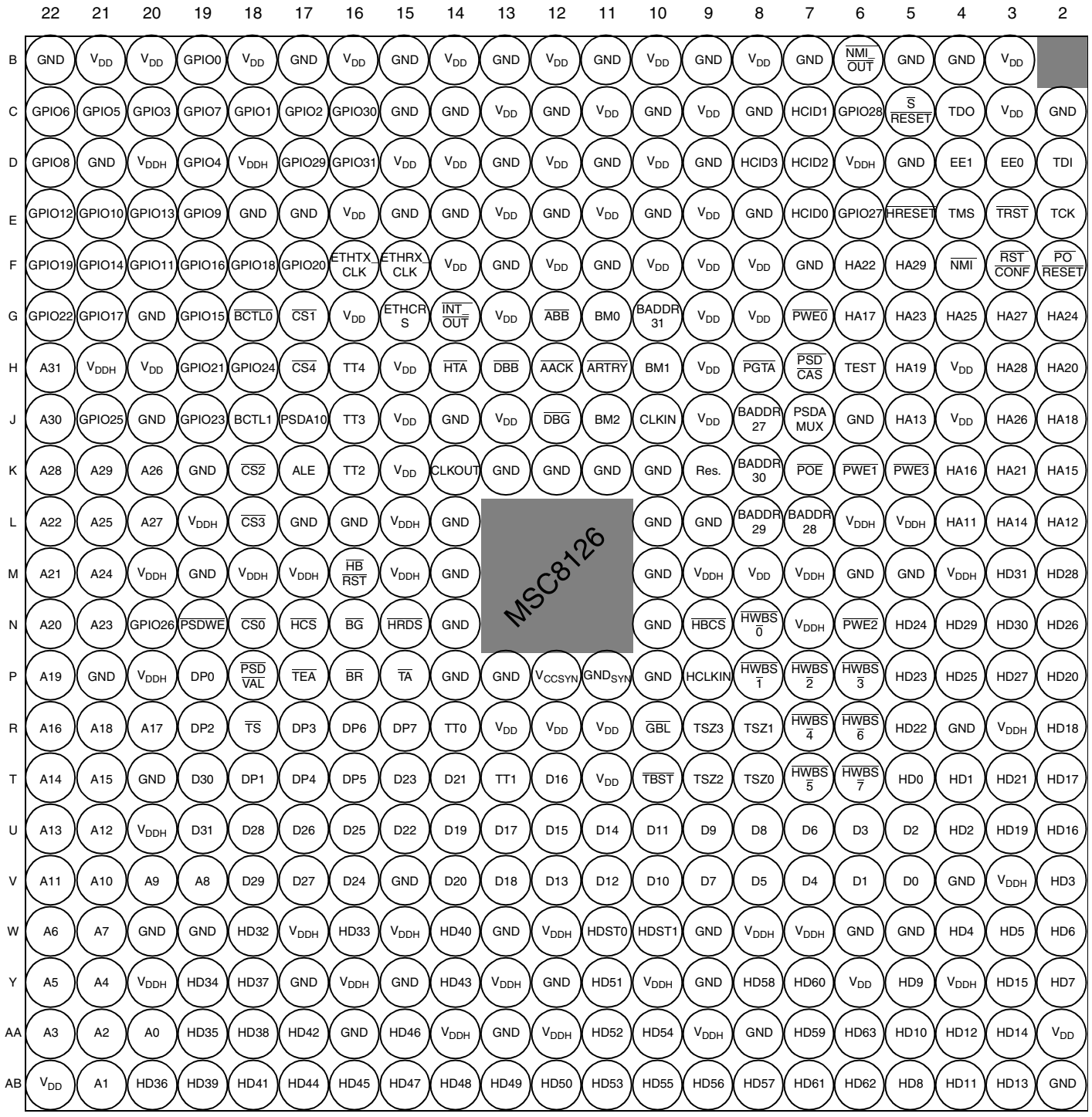


Figure 3-2. MSC8126 Package, Bottom View

Table 3-1. MSC8126 Signal Listing By Name

Signal Name	Location Designator	Signal Name	Location Designator
A0	AA20	BADDR27	J8
A1	AB21	BADDR28	L7
A2	AA21	BADDR29	L8
A3	AA22	BADDR30	K8
A4	Y21	BADDR31	G10
A5	Y22	$\overline{\text{BCTL0}}$	G18
A6	W22	$\overline{\text{BCTL1}}$	J18
A7	W21	$\overline{\text{BG}}$	N16
A8	V19	BNKSEL0	G11
A9	V20	BNKSEL1	H10
A10	V21	BNKSEL2	J11
A11	V22	BM0	G11
A12	U21	BM1	H10
A13	U22	BM2	J11
A14	T22	$\overline{\text{BR}}$	P16
A15	T21	CHIP_ID0	B19
A16	R22	CHIP_ID1	C18
A17	R20	CHIP_ID2	C17
A18	R21	CHIP_ID3	D17
A19	P22	CLKIN	J10
A20	N22	CLKOUT	K14
A21	M22	CNFGS	W3
A22	L22	$\overline{\text{CS0}}$	N18
A23	N21	$\overline{\text{CS1}}$	G17
A24	M21	$\overline{\text{CS2}}$	K18
A25	L21	$\overline{\text{CS3}}$	L18
A26	K20	$\overline{\text{CS4}}$	H17
A27	L20	$\overline{\text{CS5}}$	K16
A28	K22	$\overline{\text{CS5}}$	J18
A29	K21	$\overline{\text{CS6}}$	J16
A30	J22	$\overline{\text{CS7}}$	H16
A31	H22	D0	V5
$\overline{\text{AACK}}$	H12	D1	V6
$\overline{\text{ABB}}$	G12	D2	U5
ALE	K17	D3	U6
$\overline{\text{ARTRY}}$	H11	D4	V7

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
GND	B13	GND	L14
GND	B15	GND	L16
GND	B17	GND	L17
GND	B22	GND	M5
GND	C2	GND	M6
GND	C8	GND	M10
GND	C10	GND	M14
GND	C12	GND	M19
GND	C14	GND	N10
GND	C15	GND	N14
GND	D5	GND	P10
GND	D9	GND	P13
GND	D11	GND	P14
GND	D13	GND	P21
GND	D21	GND	R4
GND	E8	GND	T20
GND	E10	GND	V4
GND	E12	GND	V15
GND	E14	GND	W5
GND	E15	GND	W6
GND	E17	GND	W9
GND	E18	GND	W13
GND	F7	GND	W19
GND	F11	GND	W20
GND	F13	GND	Y9
GND	G20	GND	Y12
GND	J6	GND	Y15
GND	J14	GND	Y17
GND	J20	GND	AA8
GND	K10	GND	AA13
GND	K11	GND	AA16
GND	K12	GND	AB2
GND	K13	GND_{SYN}	P11
GND	K19	GPIO0	B19
GND	L9	GPIO1	C18
GND	L10	GPIO2	C17

Table 3-2. MSC8126 Signal Listing by Ball Designator (Continued)

Des.	Signal Name	Des.	Signal Name
E12	GND	G6	HA17
E13	V_{DD}	G7	PWE0/PSDDQM0/PBS0
E14	GND	G8	V_{DD}
E15	GND	G9	V_{DD}
E16	V_{DD}	G10	IRQ3/BADDR31
E17	GND	G11	BM0/TC0/BNKSEL0
E18	GND	G12	ABB/IRQ4
E19	GPIO9/TDM2TSYN/IRQ7/ETHMDIO	G13	V_{DD}
E20	GPIO13/TDM2RCLK/IRQ11/ETHMDC	G14	IRQ7/INT_OUT
E21	GPIO10/TDM2TCLK/IRQ8/ETHRX_DV/ETHCRS_DV/NC	G15	ETHCRS/ETHRXD
E22	GPIO12/TDM2RSYN/IRQ10/ETHRXD1/ETHSYNC	G16	V_{DD}
F2	PORESET	G17	CS1
F3	RSTCONF	G18	BCTL0
F4	NMI	G19	GPIO15/TDM1TSYN/DREQ1
F5	HA29	G20	GND
F6	HA22	G21	GPIO17/TDM1TDAT/DACK1
F7	GND	G22	GPIO22/TDM0TCLK/DONE2/DRACK2
F8	V_{DD}	H2	HA20
F9	V_{DD}	H3	HA28
F10	V_{DD}	H4	V_{DD}
F11	GND	H5	HA19
F12	V_{DD}	H6	TEST
F13	GND	H7	PSDCAS/PGPL3
F14	V_{DD}	H8	PGTA/PUPMWAIT/PGPL4/PPBS
F15	ETHRX_CLK/ETHSYNC_IN	H9	V_{DD}
F16	ETHTX_CLK/ETHREF_CLK/ETHCLOCK	H10	BM1/TC1/BNKSEL1
F17	GPIO20/TDM1RDAT	H11	ARTRY
F18	GPIO18/TDM1RSYN/DREQ2	H12	AACK
F19	GPIO16/TDM1TCLK/DONE1/DRACK1	H13	DBB/IRQ5
F20	GPIO11/TDM2TDAT/IRQ9/ETHRX_ER/ETHTXD	H14	HTA
F21	GPIO14/TDM2RDAT/IRQ12/ETHRXD0/NC	H15	V_{DD}
F22	GPIO19/TDM1RCLK/DACK2	H16	TT4/CS7
G2	HA24	H17	CS4
G3	HA27	H18	GPIO24/TDM0RSYN/IRQ14
G4	HA25	H19	GPIO21/TDM0TSYN
G5	HA23	H20	V_{DD}

- In CLKOUT synchronization mode (for 400 MHz devices only), CLKOUT is the main clock to SDRAM. Use the following connections:
  - — Connect the oscillator output through a buffer to CLKIN.
  - — Connect CLKOUT through a zero-delay buffer to the slave device (for example, SDRAM) using the following guidelines:
    - The maximum delay between the slave and CLKOUT must not exceed 0.7 ns.
    - The maximum load on CLKOUT must not exceed 10 pF.
    - Use a zero-delay buffer with a jitter less than 0.3 ns.
  - — All clock modes are valid in this clock scheme.

Note: See the Clock chapter in the *MSC8126 Reference Manual* for details.

- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8126 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DDH} or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- When they are used, $\overline{\text{INT\_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.
- When the Ethernet controller is enabled and the SMII mode is selected, GPIO10 and GPIO14 must not be connected externally to any signal line.

Note: For details on configuration, see the *MSC8126 User's Guide* and *MSC8126 Reference Manual*. For additional information, refer to the *MSC8126 Design Checklist* (AN2903).

4.4 External SDRAM Selection

The external bus speed implemented in a system determines the speed of the SDRAM used on that bus. However, because of differences in timing characteristics among various SDRAM manufacturers, you may have use a faster speed rated SDRAM to assure efficient data transfer across the bus. For example, for 166 MHz operation, you may have to use 183 or 200 MHz SDRAM. Always perform a detailed timing analysis using the MSC8126 bus timing values and the manufacturer specifications for the SDRAM to ensure correct operation within your system design. The output delay listed in SDRAM specifications is usually given for a load of 30 pF. Scale the number to your specific board load using the typical scaling number provided by the SDRAM manufacturer.