Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	DSI, Ethernet, RS-232
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc8126tmp6400

Table 4. DMA Controller

Feature	Description
Multi-Channel DMA Controller	• 16 time-multiplexed unidirectional channels. • Services up to four external peripherals. • Supports $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol on two external peripherals. • Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates: —A watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination. —A hungry request to indicate that the FIFO can accept more data. • Priority-based time-multiplexing between channels using 16 internal priority levels. • Round-robin time-multiplexing between channels. • A flexible channel configuration: —All channels support all features. —All channels connect to the system bus or local bus. • Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO.

Table 5. Serial Interfaces

Feature	Description
Time-Division Multiplexing (TDM)	Up to four independent TDM modules, each with the following features: • Optional operating configurations: —Totally independent receive and transmit channels, each having one data line, one clock line, and one frame sync line. —Four data lines with one clock and one frame sync shared among the transmit and receive lines. • Connects gluelessly to most T1/E1 framers as well as to common buses such as the ST-BUS. • Hardware A-law/μ-law conversion. • Up to 62.5 Mbps per TDM (62.5 MHz bit clock if one data line is used, 31.25 MHz if two data lines are used, 15.63 MHz if four data lines are used). • Up to 256 channels. • Up to 16 MB per channel buffer (granularity 8 bytes), where A/μ law buffer size is double (granularity 16 byte). • Receive buffers share one global write offset pointer that is written to the same offset relative to their start address. • Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address. • All channels share the same word size. • Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering. • Each channel can be programmed to be active or inactive. • 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively. • The TDM transmitter sync signal (TxTSYN) can be configured as either input or output. • Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock. • Frame sync can be programmed as active low or active high. • Selectable delay (0–3 bits) between the frame sync signal and the beginning of the frame. • MSB or LSB first support.

Table 5. Serial Interfaces (Continued)

Feature	Description
Ethernet Controller	• Complies with **IEEE** Std 802® including Std. 802.3™, 802.3u™, 802.3x™, and 802.3ac™. • Three Ethernet physical interfaces: —10/100 Mbps MII. —10/100 Mbps RMII. —10/100 Mbps SMII. • Full and half-duplex support. • Full-duplex flow control (automatic PAUSE frame generation or software programmed PAUSE frame generation and recognition). • Out-of-sequence transmit queue for initiating flow-control. • Programmable maximum frame length supports jumbo frames (up to 9.6 K) and virtual local area network (VLAN) tags and priority. • Retransmission from transmit FIFO following a collision. • CRC generation and verification of inbound/outbound packets. • Address recognition: —Each exact match can be programmed to be accepted or rejected. —Broadcast address (accept/reject). —Exact match 48-bit individual (unicast) address. —Hash (256-bit hash) check of individual (unicast) addresses. —Hash (256-bit hash) check of group (multicast) addresses. —Promiscuous mode. • Pattern matching: —Up to 16 unique 4-byte patterns. —Pattern match on bit-basis. —Matching range up to 256 bytes deep into the frame. —Offsets to a maximum of 252 bytes. —Programmable pattern size in 4-byte increments up to 64 bytes. —Accept or reject frames if a match is detected. —Up to eight unicast addresses for exact matches. —Pattern matching accepts/rejects IP addresses. • Filing of receive frames based on pattern match; prioritization of frames. • Insertion with expansion or replacement for transmit frames; VLAN tag insertion. • RMON statistics. • Master DMA on the local bus for fetching descriptors and accessing the buffers. • Ethernet PHY can be exposed either on GPIO pins or on the high most significant bits of the DSI/system when the DSI and the system bus are both 32 bits. • MPC8260 8-byte width buffer descriptor mode as well as 32-byte width buffer descriptor mode. • MII Bridge (MIIGSK): —Programmable selection of the 50 MHz RMII reference clock source (external or internal). —Independent 2 bit wide transmit and receive data paths. —Six operating modes. —Four general-purpose control signals. —Programmable transmitted inter-frame bits to support inter-frame gap for frames in the SMII domain. • SMII features: —Convey complete MII information between the PHY and MAC. —Allow direct MAC-to-MAC communication in SMII mode. —Can generate an interrupt request line while receiving inter-frame segments.

1.4 Direct Slave Interface, System Bus, Ethernet, and Interrupt Signals

The direct slave interface (DSI) is combined with the system bus because they share some common signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. **Table 1-5** describes the signals in this group.

Note: Although there are fifteen interrupt request (IRQ) connections to the core processors, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration enables only $\overline{\text{IRQ}}$[1–7], but includes two input lines each for $\overline{\text{IRQ}}$[1–3] and $\overline{\text{IRQ}}$7. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions. Additional alternate IRQ lines and $\overline{\text{IRQ}}$[8–15] are enabled through the GPIO signal lines.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals

Signal Name	Type	Description
HD0	Input/ Output	**Host Data Bus 0** Bit 0 of the DSI data bus.
SWTE	Input	**Software Watchdog Timer Disable**. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD1	Input/ Output	**Host Data Bus 1** Bit 1 of the DSI data bus.
DSISYNC	Input	**DSI Synchronous** Distinguishes between synchronous and asynchronous operation of the DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD2	Input/ Output	**Host Data Bus 2** Bit 2 of the DSI data bus.
DSI64	Input	**DSI 64** Defines the width of the DSI and SYSTEM Data buses. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD3	Input/ Output	**Host Data Bus 3** Bit 3 of the DSI data bus.
MODCK1	Input	**Clock Mode 1** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD4	Input/ Output	**Host Data Bus 4** Bit 4 of the DSI data bus.
MODCK2	Input	**Clock Mode 2** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD5	Input/ Output	**Host Data Bus 5** Bit 5 of the DSI data bus.
CNFGS	Input	**Configuration Source** One signal out of two that indicates reset configuration mode. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD[6–31]	Input/ Output	**Host Data Bus 6–31** Bits 6–31 of the DSI data bus.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD46	Input/ Output	**Host Data Bus 46** Bit 46 of the DSI data bus.
D46	Input/ Output	**System Bus Data 46** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD0	Output	**Ethernet Transmit Data 0** In MII and RMII modes, bit 0 of the Ethernet transmit data.
HD47	Input/ Output	**Host Data Bus 47** Bit 47 of the DSI data bus.
D47	Input/ Output	**System Bus Data 47** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD1	Output	**Ethernet Transmit Data 1** In MII and RMII modes, bit 1 of the Ethernet transmit data.
HD48	Input/ Output	**Host Data Bus 48** Bit 48 of the DSI data bus.
D48	Input/ Output	**System Bus Data 48** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD2	Output	**Ethernet Transmit Data 2** In MII mode only, bit 2 of the Ethernet transmit data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD49	Input/ Output	**Host Data Bus 49** Bit 49 of the DSI data bus.
D49	Input/ Output	**System Bus Data 49** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTXD3	Output	**Ethernet Transmit Data 3** In MII mode only, bit 3 of the Ethernet transmit data.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD[50–53]	Input/ Output	**Host Data Bus 50–53** Bits 50–53 of the DSI data bus.
D[50–53]	Input/ Output	**System Bus Data 50–53** For write transactions, the bus master drives valid data on this bus. For read transactions, the slave drives valid data on this bus.
Reserved	Input	If the Ethernet port is enabled and multiplexed with the DSI/System bus, these signals are reserved and can be left unconnected.
HD54	Input/ Output	**Host Data Bus 54** Bit 54 of the DSI data bus.
D54	Input/ Output	**System Bus Data 54** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTX_EN	Output	**Ethernet Transmit Data Enable** In MII and RMII modes, indicates that the transmit data is valid.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HWBS[4–7]	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
HDBS[4–7]	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
HWBE[4–7]	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host write accesses.
HDBE[4–7]	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host read or write accesses
PWE[4–7]	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These signals select byte lanes for write operations.
PSDDQM[4–7]	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These signals select specific byte lanes of SDRAM devices.
PBS[4–7]	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these signals is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
HRDS	Input	**Host Read Data Strobe** (In Asynchronous dual mode) Used as a strobe for host read accesses.
HRW	Input	**Host Read/Write Select** (in Asynchronous/Synchronous single mode) Host read/write select.
HRDE	Input	**Host Read Data Enable** (In Synchronous dual mode) Indicates valid data for host read accesses.
HBRST	Input	**Host Burst** The host asserts this signal to indicate that the current transaction is a burst transaction in synchronous mode only.
HDST[0–1]	Input	**Host Data Structure 0–1** Defines the data structure of the host access in DSI little-endian mode.
HA[9–10]		**Host Bus Address 9–10** Used by an external host to access the internal address space.
HCS	Input	**Host Chip Select** DSI chip select. The DSI is accessed only if HCS is asserted and HCID[0–3] matches the Chip_ID.
HBCS	Input	**Host Broadcast Chip Select** DSI chip select for broadcast mode. Enables more than one DSI to share the same host chip-select signal for broadcast write accesses.
HTA	Output	**Host Transfer Acknowledge** Upon a read access, indicates to the host when the data on the data bus is valid. Upon a write access, indicates to the host that the data on the data bus was written to the DSI write buffer.
HCLKIN	Input	**Host Clock Input** Host clock signal for DSI synchronous mode.
A[0–31]	Input/ Output	**Address Bus** When the MSC8126 is in external master bus mode, these signals function as the system address bus. The MSC8126 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8126 is in internal master bus mode, these signals are used as address lines connected to memory devices and are controlled by the MSC8126 memory controller.
TT0	Input/ Output	**Bus Transfer Type 0** The bus master drives this signals during the address tenure to specify the type of the transaction.
HA7		**Host Bus Address 7** Used by an external host to access the internal address space.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
IRQ7	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
INT_OUT	Output	**Interrupt Output** This output indicates whether an unmasked interrupt is pending in the MSC8126 internal interrupt controller.

Notes:
1. See the System Interface Unit (SIU) chapter in the *MSC8126 Reference Manual* for details on how to configure these signals.
2. When used as the bus control arbiter, the MSC8126 can support up to three external bus masters. Each master uses its own set of Bus Request, Bus Grant, and Data Bus Grant signals (BR/BG/DBG, EXT_BR2/EXT_BG2/EXT_DBG2, and EXT_BR3/EXT_BG3/EXT_DBG3). Each of these signal sets must be configured to indicate whether the external master is or is not a MSC8126 master device. See the Bus Configuration Register (BCR) description in the System Interface Unit (SIU) chapter in the *MSC8126 Reference Manual* for details on how to configure these signals. The second and third set of signals is defined by EXT_xxx to indicate that they can only be used with external master devices. The first set of signals (BR/BG/DBG) have a dual function. When the MSC8126 is not the bus arbiter, it uses these signals (BR/BG/DBG) to obtain master control of the bus.

1.5 Memory Controller Signals

Refer to the Memory Controller chapter in the *MSC8126 Reference Manual* for details on configuring these signals.

Table 1-6. Memory Controller Signals

Signal Name	Type	Description
BCTL0	Output	**System Bus Buffer Control 0** Controls buffers on the data bus. Usually used with BCTL1. The exact function of this signal is defined by the value of SIUMCR[BCTLC].
BCTL1	Output	**System Bus Buffer Control 1** Controls buffers on the data bus. Usually used with BCTL0. The exact function of this signal is defined by the value of SIUMCR[BCTLC].
CS5	Output	**System and Local Bus Chip Select 5** Enables specific memory devices or peripherals connected to MSC8126 buses.
BM[0–2]	Input	**Boot Mode 0–2** Defines the boot mode of the MSC8126. This signal is sampled on PORESET deassertion.
TC[0–2]	Input/ Output	**Transfer Code 0–2** The bus master drives these signals during the address tenure to specify the type of the code.
BNKSEL[0–2]	Output	**Bank Select 0–2** Selects the SDRAM bank when the MSC8126 is in 60x-compatible bus mode.
ALE	Output	**Address Latch Enable** Controls the external address latch used in an external master bus.
PWE[0–3]	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These signals select byte lanes for write operations.
PSDDQM[0–3]	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These signals select specific byte lanes of SDRAM devices.
PBS[0–3]	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these signals is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO11	Input/ Output	**General-Purpose Input Output 11** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2TDAT	Input/ Output	**TDM2 Serial Transmitter Data** The transmit data signal for TDM 2. As an output, this can be the DATA_D data signal for TDM 2. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ9}}$	Input	**Interrupt Request 9** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRX_ER	Input	**Ethernet Receive Data Error** In MII and RMII modes, indicates a receive data error.
ETHTXD	Output	**Ethernet Transmit Data** In SMII, used as the Ethernet transmit data line.
GPIO12	Input/ Output	General-Purpose Input Output 12 One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2RSYN	Input/ Output	**TDM2 Receive Frame Sync** The receive sync signal for TDM 2. As an input, this can be the DATA_B data signal for TDM 2. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ10}}$	Input	**Interrupt Request 10** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRXD1	Input	**Ethernet Receive Data 1** Bit 1 of the Ethernet receive data (MII and RMII mode).
ETHSYNC	Output	**Ethernet Sync Signal** In SMII mode, this is the Ethernet sync signal input.
GPIO13	Input/ Output	**General-Purpose Input Output 13** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM2RCLK	Input/ Output	**TDM2 Receive Clock** The receive clock signal for TDM 2. As an input, this can be the DATA_C data signal for TDM 2. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ11}}$	Input	**Interrupt Request 11** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHMDC	Output	**Ethernet Management Clock** Used for the MDIO reference clock for MII, RMII, and SMII modes.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO18	Input/ Output	**General-Purpose Input Output 18** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RSYN	Input/ Output	**TDM1 Receive Frame Sync** The receive sync signal for TDM 1. As an input, this can be the DATA_B data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual*.
DREQ2	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
GPIO19	Input/ Output	**General-Purpose Input Output 19** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RCLK	Input/ Output	**TDM1 Receive Clock** The receive clock signal for TDM 1. As an input, this can be the DATA_C data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{DACK2}}$	Output	**DMA Acknowledge 2** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
GPIO20	Input/ Output	**General-Purpose Input Output 20** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM1RDAT	Input/ Output	**TDM1 Serial Receiver Data** The receive data signal for TDM 1. As an input, this can be the DATA_A data signal for TDM 1. For configuration details, refer to the *MSC8126 Reference Manual*.
GPIO21	Input/ Output	**General-Purpose Input Output 21** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TSYN	Input/ Output	**TDM0 Transmit frame Sync** Transmit Frame Sync for TDM 0.
GPIO22	Input/ Output	**General-Purpose Input Output 22** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM0TCLK	Input	**TDM 0 Transmit Clock** Transmit Clock for TDM 0.
$\overline{\text{DONE2}}$	Input/ Output	**DMA Done 2** Signifies that the channel must be terminated. If the DMA generates DONE, the channel handling this peripheral is inactive. As an input to the DMA, DONE closes the channel much like a normal channel closing. **Note:** See the *MSC8126 Reference Manual* chapters on DMA and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and signal direction.
$\overline{\text{DRACK2}}$	Output	**DMA Data Request Acknowledge 2** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.

2.5.5.3 DMA Data Transfers

Table 2-16 describes the DMA signal timing.

Table 2-16. DMA Signals

No.	Characteristic	Ref = CLKIN		Ref = CLKOUT		Units
		Min	Max	Min	Max	
37	DREQ set-up time before the 50% level of the falling edge of REFCLK	5.0	—	5.0	—	ns
38	DREQ hold time after the 50% level of the falling edge of REFCLK	0.5	—	0.5	—	ns
39	$\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK	5.0	—	5.0	—	ns
40	$\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK	0.5	—	0.5	—	ns
41	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge	0.5	7.5	0.5	8.4	ns
Note:	CLKOUT synchronization mode is not supported in cores operating above 400 MHz.					

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-16**. **Figure 2-8** shows synchronous peripheral interaction.

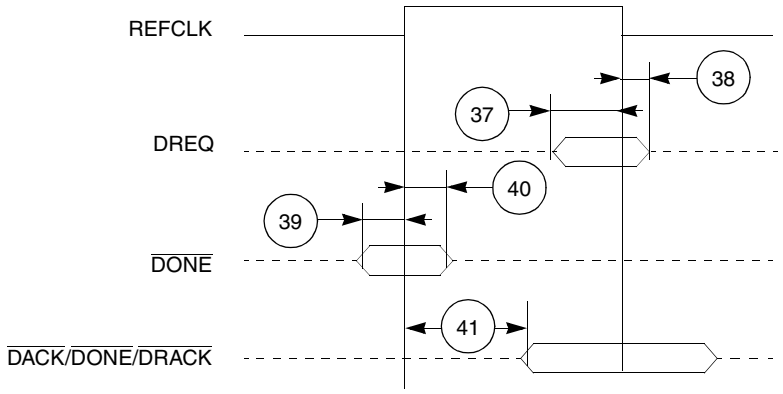

Figure 2-8. DMA Signals

2.5.6 DSI Timing

The timings in the following sections are based on a 20 pF capacitive load.

2.5.6.1 DSI Asynchronous Mode

Table 2-17. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Max	Unit
100	Attributes[1] set-up time before strobe ($\overline{\text{HWBS[n]}}$) assertion	1.5	—	ns
101	Attributes[1] hold time after data strobe deassertion	1.3	—	ns
102	Read/Write data strobe deassertion width: • DCR[HTAAD] = 1 — Consecutive access to the same DSI — Different device with DCR[HTADT] = 01 — Different device with DCR[HTADT] = 10 — Different device with DCR[HTADT] = 11 • DCR[HTAAD] = 0	 $1.8 + T_{REFCLK}$ $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$ $1.8 + T_{REFCLK}$	—	 ns ns ns ns ns
103	Read data strobe deassertion to output data high impedance	—	8.5	ns
104	Read data strobe assertion to output data active from high impedance	2.0	—	ns
105	Output data hold time after read data strobe deassertion	2.2	—	ns
106	Read/Write data strobe assertion to $\overline{\text{HTA}}$ active from high impedance	2.2	—	ns
107	Output data valid to $\overline{\text{HTA}}$ assertion	3.2	—	ns
108	Read/Write data strobe assertion to $\overline{\text{HTA}}$ valid[2]	—	6.7	ns
109	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0)	—	6.5	ns
110	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1)	—	6.5	ns
111	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1 • DCR[HTADT] = 01 • DCR[HTADT] = 10 • DCR[HTADT] = 11	—	 $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$	 ns ns ns
112	Read/Write data strobe assertion width	$1.8 + T_{REFCLK}$	—	ns
201	Host data input set-up time before write data strobe deassertion	1.0	—	ns
202	Host data input hold time after write data strobe deassertion	1.5	—	ns

Notes:
1. *Attributes* refers to the following signals: $\overline{\text{HCS}}$, HA[11–29], HCID[0–4], HDST, HRW, $\overline{\text{HRDS}}$, and $\overline{\text{HWBSn}}$.
2. This specification is tested in dual strobe mode. Timing in single strobe mode is guaranteed by design.
3. All values listed in this table are tested or guaranteed by design.

2.5.6.2 DSI Synchronous Mode

Table 2-18. DSI Inputs—Synchronous Mode

No.	Characteristic	Expression	Min	Max	Units
120	HCLKIN Cycle Time[1, 2]	HTC	10.0	55.6	ns
121	HCLKIN high Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
122	HCLKIN low Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.4	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes: **1.** Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 2-6** for HCLKIN frequency limits.

Table 2-19. DSI Outputs—Synchronous Mode

No.	Characteristic	Min	Max	Units
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	6.3	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	7.6	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.0	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	5.9	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	6.3	ns

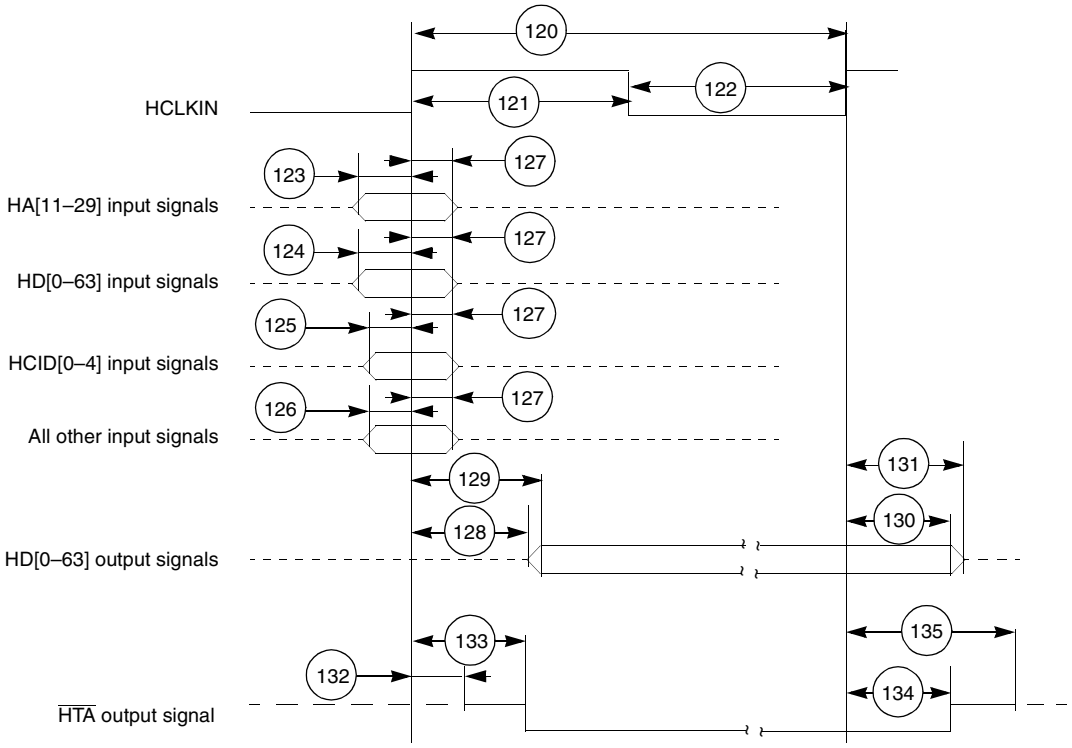

Figure 2-12. DSI Synchronous Mode Signals Timing Diagram

2.5.7 TDM Timing

Table 2-20. TDM Timing

No.	Characteristic	Expression	Ref = CLKIN		Units
			Min	Max	
300	TDMxRCLK/TDMxTCLK	TC[1]	16	—	ns
301	TDMxRCLK/TDMxTCLK high pulse width	(0.5 ±0.1) × TC	7	—	ns
302	TDMxRCLK/TDMxTCLK low pulse width	(0.5 ±0.1) × TC	7	—	ns
303	TDM receive all input set-up time		1.3	—	ns
304	TDM receive all input hold time		1.0	—	ns
305	TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3]		2.8	—	ns
306	TDMxTCLK high to TDMxTDAT/TDMxRCLK output valid[2,3]		—	8.8	ns
307	All output hold time[5]		2.5	—	ns
308	TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3]		—	10.5	ns
309	TDMxTCLK high to TDMXTSYN output valid[2]		—	8.5	ns
310	TDMxTSYN output hold time[5]		2.5	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See the *MSC8126 Reference Manual* for details.
4. CLKOUT synchronization is not supported for cores operating at above 400 MHz.
5. Values are based on 10 pF capacitive load.

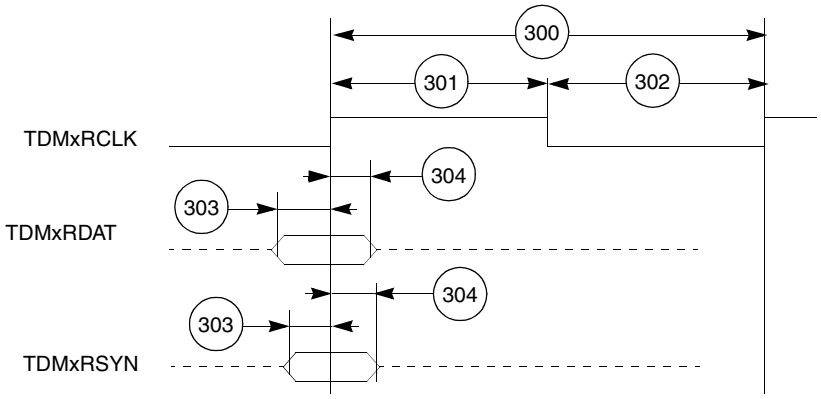

Figure 2-13. TDM Inputs Signals

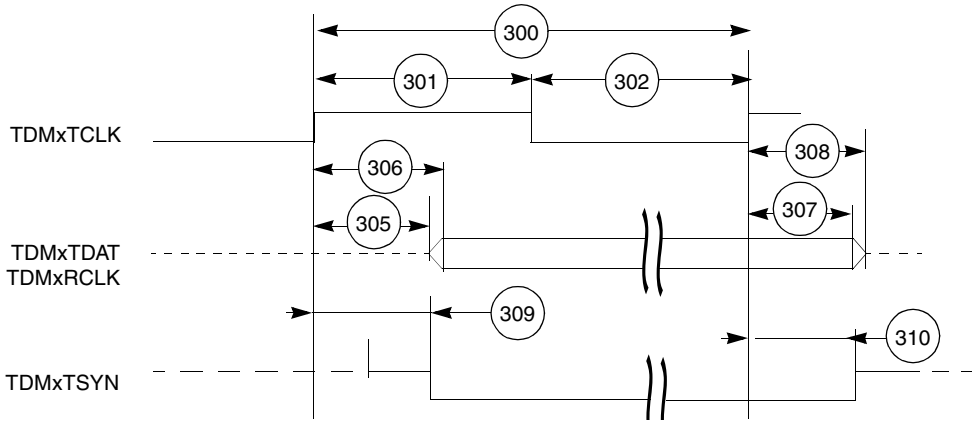

Figure 2-14. TDM Output Signals

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 2-23. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

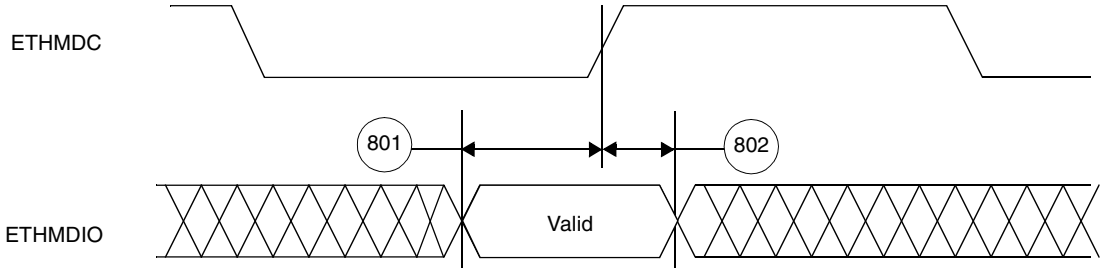

Figure 2-18. MDIO Timing Relationship to MDC

2.5.10.2 MII Mode Timing

Table 2-24. MII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay	1	12.6	ns

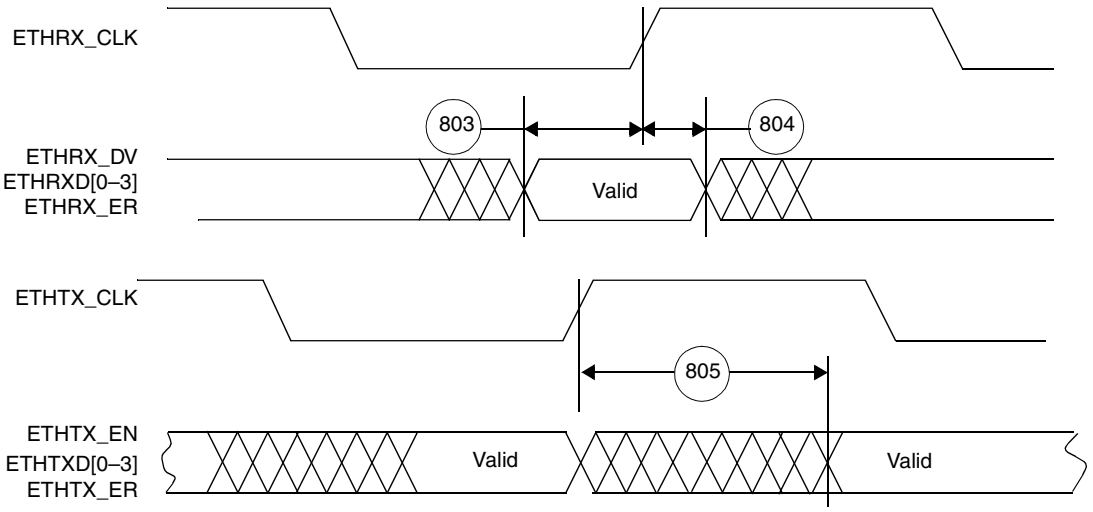

Figure 2-19. MII Mode Signal Timing

2.5.11 GPIO Timing

Table 2-27. GPIO Timing

No.	Characteristics	Ref = CLKIN		Ref = CLKOUT		Unit
		Min	Max	Min	Max	
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	6.1	—	6.9	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	1.1	—	1.3	—	ns
603	REFCLK edge to high impedance on GPIO out	—	5.4	—	6.2	ns
604	GPIO in valid to REFCLK edge (GPIO in set-up time)	3.5	—	3.7	—	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	—	0.5	—	ns
Note:	CLKOUT synchronization mode is not supported for cores operating at above 400 MHz.					

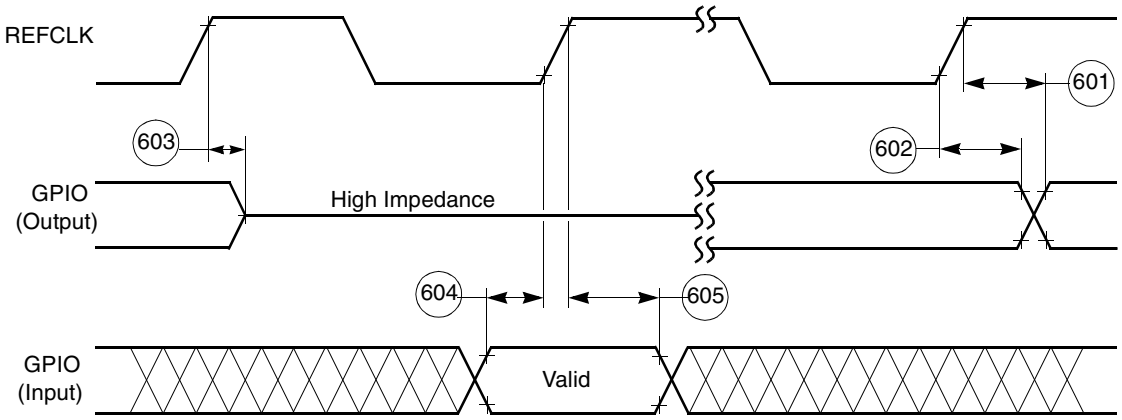

Figure 2-22. GPIO Timing

2.5.12 EE Signals

Table 2-28. EE Pin Timing

Number	Characteristics	Type	Min
65	EE0 (input)	Asynchronous	4 core clock periods
66	EE1 (output)	Synchronous to Core clock	1 core clock period

Notes: **1.** The core clock is the SC140 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Refer to **Table 1-4** on page 1-6 for details on EE pin functionality.

Figure 2-23 shows the signal behavior of the EE pins.

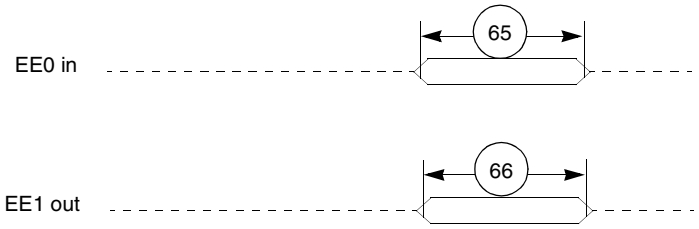

Figure 2-23. EE Pin Timing

2.5.13 JTAG Signals

Table 2-29. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/(T_C × 4); maximum 25 MHz)	0.0	25	MHz
701	TCK cycle time	40.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V • High • Low	 20.0 16.0	 — —	 ns ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	20.0	—	ns
706	TCK low to output data valid	0.0	30.0	ns
707	TCK low to output high impedance	0.0	30.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	20.0	—	ns
710	TCK low to TDO data valid	0.0	20.0	ns
711	TCK low to TDO high impedance	0.0	20.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns
713	$\overline{\text{TRST}}$ set-up time to TCK low	30.0	—	ns
Note:	All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.			

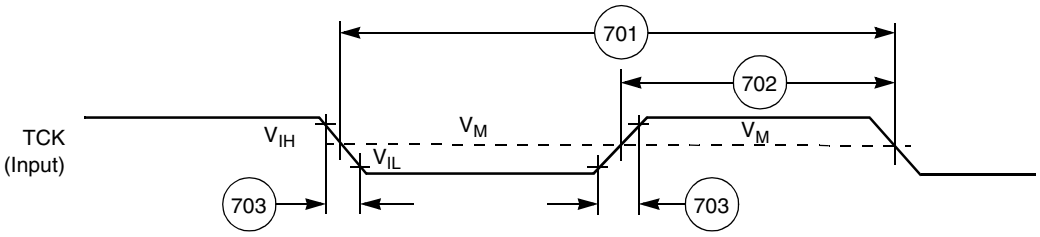

Figure 2-24. Test Clock Input Timing Diagram

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
DP3	R17	ETHRXD0	F21
DP4	T17	ETHRXD0	W14
DP5	T16	ETHRXD1	E22
DP6	R16	ETHRXD1	AB18
DP7	R15	ETHRXD2	C22
$\overline{\text{DRACK1}}$	F19	ETHRXD2	AA17
$\overline{\text{DRACK2}}$	G22	ETHRXD3	C21
DREQ1	E6	ETHRXD3	Y14
DREQ1	G19	ETHSYNC	E22
DREQ1	P19	ETHSYNC_IN	F15
DREQ2	C6	ETHTX_CLK	F16
DREQ2	F18	ETHTX_EN	D17
DREQ2	R17	ETHTX_EN	AA10
DREQ3	R16	ETHTX_ER	D19
DREQ4	R15	ETHTX_ER	AB10
DSI64	U4	ETHTXD	F20
DSISYNC	T4	ETHTXD0	B19
EE0	D3	ETHTXD0	AA15
EE1	D4	ETHTXD1	C18
ETHCLOCK	F16	ETHTXD1	AB15
ETHCOL	D22	ETHTXD2	C20
ETHCOL	Y7	ETHTXD2	AB14
ETHCRS	G15	ETHTXD3	C19
ETHCRS_DV	E21	ETHTXD3	AB13
ETHCRS_DV	AB9	$\overline{\text{EXT\_BG2}}$	T18
ETHMDC	E20	$\overline{\text{EXT\_BG3}}$	T16
ETHMDC	Y8	$\overline{\text{EXT\_BR2}}$	P19
ETHMDIO	E19	$\overline{\text{EXT\_BR3}}$	R17
ETHMDIO	AA7	$\overline{\text{EXT\_DBG2}}$	R19
ETHREF_CLK	F16	$\overline{\text{EXT\_DBG3}}$	T17
ETHRX_CLK	F15	$\overline{\text{GBL}}$	R10
ETHRX_DV	E21	GND	B4
ETHRX_DV	AB9	GND	B5
ETHRX_ER	F20	GND	B7
ETHRX_ER	AB8	GND	B9
ETHRXD	G15	GND	B11

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
GND	B13	GND	L14
GND	B15	GND	L16
GND	B17	GND	L17
GND	B22	GND	M5
GND	C2	GND	M6
GND	C8	GND	M10
GND	C10	GND	M14
GND	C12	GND	M19
GND	C14	GND	N10
GND	C15	GND	N14
GND	D5	GND	P10
GND	D9	GND	P13
GND	D11	GND	P14
GND	D13	GND	P21
GND	D21	GND	R4
GND	E8	GND	T20
GND	E10	GND	V4
GND	E12	GND	V15
GND	E14	GND	W5
GND	E15	GND	W6
GND	E17	GND	W9
GND	E18	GND	W13
GND	F7	GND	W19
GND	F11	GND	W20
GND	F13	GND	Y9
GND	G20	GND	Y12
GND	J6	GND	Y15
GND	J14	GND	Y17
GND	J20	GND	AA8
GND	K10	GND	AA13
GND	K11	GND	AA16
GND	K12	GND	AB2
GND	K13	GND_{SYN}	P11
GND	K19	GPIO0	B19
GND	L9	GPIO1	C18
GND	L10	GPIO2	C17

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
HRESET	E5	IRQ5	L8
HRW	N15	IRQ5	T16
HTA	H14	IRQ6	C17
HWBE0	N8	IRQ6	D22
HWBE1	P8	IRQ6	R16
HWBE2	P7	IRQ7	E19
HWBE3	P6	IRQ7	G14
HWBE4	R7	IRQ7	R15
HWBE5	T7	IRQ8	E21
HWBE6	R6	IRQ9	F20
HWBE7	T6	IRQ10	E22
HWBS0	N8	IRQ11	E20
HWBS1	P8	IRQ12	F21
HWBS2	P7	IRQ13	J19
HWBS3	P6	IRQ14	H18
HWBS4	R7	IRQ15	J21
HWBS5	T7	MODCK1	V2
HWBS6	R6	MODCK2	W4
HWBS7	T6	HWBE4	R7
INT_OUT	G14	HWBE5	T7
IRQ1	C20	HWBE6	R6
IRQ1	R10	HWBE7	T6
IRQ1	T18	NC	E21
IRQ2	D19	NC	F21
IRQ2	K8	NMI	F4
IRQ2	R19	NMI_OUT	B6
IRQ3	C21	PBS0	G7
IRQ3	G10	PBS1	K6
IRQ3	R17	PBS2	N6
IRQ4	B19	PBS3	K5
IRQ4	C22	PBS4	R7
IRQ4	G12	PBS5	T7
IRQ4	T17	PBS6	R6
IRQ5	C18	PBS7	T6
IRQ5	C19	PGPL0	J17
IRQ5	H13	PGPL1	N19

Table 3-2. MSC8126 Signal Listing by Ball Designator

Des.	Signal Name	Des.	Signal Name
B3	V_{DD}	C18	GPIO1/TIMER0/CHIP_ID1/$\overline{\text{IRQ5}}$/ETHTXD1
B4	GND	C19	GPIO7/TDM3RCLK/$\overline{\text{IRQ5}}$/ETHTXD3
B5	GND	C20	GPIO3/TDM3TSYN/$\overline{\text{IRQ1}}$/ETHTXD2
B6	$\overline{\text{NMI\_OUT}}$	C21	GPIO5/TDM3TDAT/$\overline{\text{IRQ3}}$/ETHRXD3
B7	GND	C22	GPIO6/TDM3RSYN/$\overline{\text{IRQ4}}$/ETHRXD2
B8	V_{DD}	D2	TDI
B9	GND	D3	EE0
B10	V_{DD}	D4	EE1
B11	GND	D5	GND
B12	V_{DD}	D6	V_{DDH}
B13	GND	D7	HCID2
B14	V_{DD}	D8	HCID3/HA8
B15	GND	D9	GND
B16	V_{DD}	D10	V_{DD}
B17	GND	D11	GND
B18	V_{DD}	D12	V_{DD}
B19	GPIO0/CHIP_ID0/$\overline{\text{IRQ4}}$/ETHTXD0	D13	GND
B20	V_{DD}	D14	V_{DD}
B21	V_{DD}	D15	V_{DD}
B22	GND	D16	GPIO31/TIMER3/SCL
C2	GND	D17	GPIO29/CHIP_ID3/ETHTX_EN
C3	V_{DD}	D18	V_{DDH}
C4	TDO	D19	GPIO4/TDM3TCLK/$\overline{\text{IRQ2}}$/ETHTX_ER
C5	$\overline{\text{SRESET}}$	D20	V_{DDH}
C6	GPIO28/DREQ2/UTXD	D21	GND
C7	HCID1	D22	GPIO8/TDM3RDAT/$\overline{\text{IRQ6}}$/ETHCOL
C8	GND	E2	TCK
C9	V_{DD}	E3	$\overline{\text{TRST}}$
C10	GND	E4	TMS
C11	V_{DD}	E5	$\overline{\text{HRESET}}$
C12	GND	E6	GPIO27/DREQ1/URXD
C13	V_{DD}	E7	HCID0
C14	GND	E8	GND
C15	GND	E9	V_{DD}
C16	GPIO30/TIMER2/TMCLK/SDA	E10	GND
C17	GPIO2/TIMER1/CHIP_ID2/$\overline{\text{IRQ6}}$	E11	V_{DD}

Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8126	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	1.2 V	–40° to 105°C	400	MSC8126TVT6400
		Lead-bearing				MSC8126TMP6400
		Lead-free		0° to 90°C	500	MSC8126VT8000
		Lead-bearing				MSC8126MP8000

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations not listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GMBH
Technical Information Center
Schatzbogen 7
81829 München, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MSC8126
Rev. 11
4/2006

freescale™
semiconductor