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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	DSI, Ethernet, RS-232
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	1.436MB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc8126tvt6400

Table 1. Extended SC140 Cores and Core Memories

Feature	Description
SC140 Core	Four SC140 cores: • Up to 8000 MMACS using 16 ALUs running at up to 500 MHz. • A total of 1436 KB of internal SRAM (224 KB per core + 16 KB ICache per core + the shared M2 memory). Each SC140 core provides the following: • Up to 2000 MMACS using an internal 500 MHz clock. A MAC operation includes a multiply-accumulate command with the associated data move and pointer update. • 4 ALUs per SC140 core. • 16 data registers, 40 bits each. • 27 address registers, 32 bits each. • Hardware support for fractional and integer data types. • Very rich 16-bit wide orthogonal instruction set. • Up to six instructions executed in a single clock cycle. • Variable-length execution set (VLES) that can be optimized for code density and performance. • JTAG port complies with **IEEE**® Std 1149.1™. • Enhanced on-device emulation (EOnCE) with real-time debugging capabilities.
Extended Core	Each SC140 core is embedded within an extended core that provides the following: • 224 KB M1 memory that is accessed by the SC140 core with zero wait states. • Support for atomic accesses to the M1 memory. • 16 KB instruction cache, 16 ways. • A four-entry write buffer that frees the SC140 core from waiting for a write access to finish. • External cache support by asserting the global signal (GBL) when predefined memory banks are accessed. • Programmable interrupt controller (PIC). • Local interrupt controller (LIC).
Multi-Core Shared Memories	• M2 memory (shared memory): —A 476 KB memory working at the core frequency. —Accessible from the local bus. —Accessible from all four SC140 cores using the MQBus. • 4 KB bootstrap ROM.
M2-Accessible Multi-Core Bus (MQBus)	• A QBus protocol multi-master bus connecting the four SC140 cores and the VCOP to the M2 memory. • Data bus access of up to 128-bit read and up to 64-bit write. • Operation at the SC140 core frequency. • A central efficient round-robin arbiter controlling SC140 core access on the MQBus. • Atomic operation control of access to M2 memory by the four SC140 cores and the local bus.

Table 2. Phase-Lock Loop (PLL)

Feature	Description
Internal PLL	• Generates up to 500 MHz core clock and up to 166 MHz bus clocks for the 60x-compatible local and system buses and other modules. • PLL values are determined at reset based on configuration signal values.

Table 10. Application Development System (ADS) Board

Feature	Description
MSC8126ADS	• Host debug through single JTAG connector supports both processors. • MSC8103 as the MSC8126 host with both devices on the board. The MSC8103 system bus connects to the MSC8126 DSI. • Flash memory for stand-alone applications. • Communications ports: —10/100Base-T. —155 Mbit ATM over Optical. —T1/E1 TDM interface. —H.110. —Voice codec. —RS-232. —High-density (MICTOR) logic analyzer connectors to monitor MSC8126 signals —6U CompactPCI form factor. • Emulates MSC8126 DSP farm by connecting to three other ADS boards.

Product Documentation

The documents listed in **Table 11** are required for a complete description of the MSC8126 and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale Semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back of this document.

Table 11. MSC8126 Documentation

Name	Description	Order Number
MSC8126 Technical Data	MSC8126 features list and physical, electrical, timing, and package specifications.	MSC8126
MSC8126 User's Guide	User information includes system functionality, getting started, and programming topics.	Availability TBD
MSC8126 Reference Manual	Detailed functional description of the MSC8126 memory and peripheral configuration, operation, and register programming.	MSC8126RM
StarCore™ SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set.	MNSC140CORE
Application Notes	Documents describing specific applications or optimized device operation including code examples.	See the website product page.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
HD55	Input/ Output	**Host Data Bus 55** Bit 55 of the DSI data bus.
D55	Input/ Output	**System Bus Data 55** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHTX_ER	Output	**Ethernet Transmit Data Error** In MII mode only, indicates a transmit data error.
Reserved	Input	In RMII mode, this signal is reserved and can be left unconnected.
HD56	Input/ Output	**Host Data Bus 56** Bit 56 of the DSI data bus.
D56	Input/ Output	**System Bus Data 56** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRX_DV	Input	**Ethernet Receive Data Valid** Indicates that the receive data is valid.
ETHCRS_DV	Input	**Ethernet Carrier Sense/Receive Data Valid** In RMII mode, indicates that a carrier is detected and after the connection is established that the receive data is valid.
HD57	Input/ Output	**Host Data Bus 57** Bit 57 of the DSI data bus.
D57	Input/ Output	**System Bus Data 57** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHRX_ER	Input	**Ethernet Receive Data Error** In MII and RMII modes, indicates a receive data error.
HD58	Input/ Output	**Host Data Bus 58** Bit 58 of the DSI data bus.
D58	Input/ Output	**System Bus Data 58** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHMDC	Output	**Ethernet Management Clock** In MII and RMII modes, used for the MDIO reference clock.
HD59	Input/ Output	**Host Data Bus 59** Bit 59 of the DSI data bus.
D59	Input/ Output	**System Bus Data 59** For write transactions, the bus master drives valid data on this line. For read transactions, the slave drives valid data on this bus.
ETHMDIO	Input/ Output	**Ethernet Management Data** In MII and RMII modes, used for station management data input/output.

Table 1-5. DSI, System Bus, Ethernet, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{BG}}$	Input/ Output	**Bus Grant**[2] When the MSC8126 acts as an internal arbiter, it asserts this signal as an output to grant bus ownership to an external bus master. When an external arbiter is used, it asserts this signal as an input to grant bus ownership to the MSC8126.
$\overline{\text{DBG}}$	Input/ Output	**Data Bus Grant**[2] When the MSC8126 acts as an internal arbiter, it asserts this signal as an output to grant data bus ownership to an external bus master. When an external arbiter is used, it asserts this signal as an input to grant data bus ownership to the MSC8126.
$\overline{\text{ABB}}$	Input/ Output	**Address Bus Busy**[1] The MSC8126 asserts this signal as an output for the duration of the address bus tenure. Following an $\overline{\text{AACK}}$, which terminates the address bus tenure, the MSC8126 deasserts $\overline{\text{ABB}}$ for a fraction of a bus cycle and then stops driving this signal. The MSC8126 does not assume bus ownership as long as it senses this signal is asserted as an input by an external bus master.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{DBB}}$	Input/ Output	**Data Bus Busy**[1] The MSC8126 asserts this signal as an output for the duration of the data bus tenure. Following a $\overline{\text{TA}}$, which terminates the data bus tenure, the MSC8126 deasserts $\overline{\text{DBB}}$ for a fraction of a bus cycle and then stops driving this signal. The MSC8126 does not assume data bus ownership as long as it senses that this signal is asserted as an input by an external bus master.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{TS}}$	Input/ Output	**Bus Transfer Start** This signal indicates the beginning of a new address bus tenure. The MSC8126 asserts this signal when one of its internal bus masters begins an address tenure. When the MSC8126 senses that this signal is asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8126 resources, memory controller support).
$\overline{\text{AACK}}$	Input/ Output	**Address Acknowledge** A bus slave asserts this signal to indicate that it has identified the address tenure. This signal terminates the address tenure.
$\overline{\text{ARTRY}}$	Input/ Output	**Address Retry** This signal indicates whether the bus master should retry the bus transaction. An external master asserts this signal to enforce data coherency with its caches and to prevent deadlock situations.
D[0–31]	Input/ Output	**Data Bus Bits 0–31** In write transactions, the bus master drives the valid data on this bus. In read transactions, the slave drives the valid data on this bus.
Reserved	Input	The primary configuration selection (default after reset) is reserved.
DP0	Input/ Output	**System Bus Data Parity 0** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 0 signal should give odd parity (odd number of ones) on the group of signals that includes data parity 0 and D[0–7].
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
$\overline{\text{EXT\_BR2}}$	Input	**External Bus Request 2** An external master asserts this signal to request bus ownership from the internal arbiter.

Table 1-6. Memory Controller Signals (Continued)

Signal Name	Type	Description
PSDA10	Output	**System Bus SDRAM A10** From the bus SDRAM controller. The precharge command defines which bank is precharged. When the row address is driven, it is a part of the row address. When column address is driven, it is a part of column address.
PGPL0	Output	**System Bus UPM General-Purpose Line 0** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PSDWE}}$	Output	**System Bus SDRAM Write Enable** From the bus SDRAM controller. Should connect to SDRAM WE input.
PGPL1	Output	**System Bus UPM General-Purpose Line 1** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{POE}}$	Output	**System Bus Output Enable** From the bus GPCM. Controls the output buffer of memory devices during read operations.
$\overline{\text{PSDRAS}}$	Output	**System Bus SDRAM $\overline{\text{RAS}}$** From the bus SDRAM controller. Should connect to SDRAM $\overline{\text{RAS}}$ input.
PGPL2	Output	**System Bus UPM General-Purpose Line 2** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PSDCAS}}$	Output	**System Bus SDRAM $\overline{\text{CAS}}$** From the bus SDRAM controller. Should connect to SDRAM $\overline{\text{CAS}}$ input.
PGPL3	Output	**System Bus UPM General-Purpose Line 3** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PGTA}}$	Input	**System GPCM TA** Terminates external transactions during GPCM operation. Requires an external pull-up resistor for proper operation.
PUPMWAIT	Input	**System Bus UPM Wait** An external device holds this signal low to force the UPM to wait until the device is ready to continue the operation.
PGPL4	Output	**System Bus UPM General-Purpose Line 4** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.
$\overline{\text{PPBS}}$	Output	**System Bus Parity Byte Select** In systems that store data parity in a separate chip, this output is used as the byte-select for that chip.
PSDAMUX	Output	**System Bus SDRAM Address Multiplexer** Controls the system bus SDRAM address multiplexer when the MSC8126 is in external master mode.
PGPL5	Output	**System Bus UPM General-Purpose Line 5** One of six general-purpose output lines from the UPM. The values and timing of this signal are programmed in the UPM.

Table 1-7. GPIO, TDM, UART, Ethernet, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO3	Input/ Output	**General-Purpose Input Output 3** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3TSYN	Input/ Output	**TDM3 Transmit Frame Sync** Transmit frame sync for TDM 3.
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTXD2	Output	**Ethernet Transmit Data 2** For MII mode only, bit 2 of the Ethernet transmit data.
GPIO4	Input/ Output	**General-Purpose Input Output 4** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3TCLK	Input	**TDM3 Transmit Clock** Transmit Clock for TDM 3
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHTX_ER	Output	**Ethernet Transmit Data Error** For MII mode only, indicates whether a transmit data error occurred.
GPIO5	Input/ Output	**General-Purpose Input/Output 5** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3TDAT	Input/ Output	**TDM3 Serial Transmitter Data** The serial transmit data signal for TDM 3. As an output, it provides the DATA_D signal for TDM 3. For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRXD3	Input	**Ethernet Receive Data 3** For MII mode only, bit 3 of the Ethernet receive data.
GPIO6	Input/ Output	**General-Purpose Input Output 6** One of 32 GPIO signals used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8126 Reference Manual* GPIO programming model.
TDM3RSYN	Input/ Output	**TDM3 Receive Frame Sync** The receive sync signal for TDM 3. As an input, this can be the DATA_B data signal for TDM 3.For configuration details, refer to the *MSC8126 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
ETHRXD2	Input	**Ethernet Receive Data 2** For MII mode only, bit 2 of the Ethernet receive data.

Table 2-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	—	3.465	V
Input low voltage[1]	V_{IL}	GND	0	0.4	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.4	V
Input leakage current, $V_{IN} = V_{DDH}$	I_{IN}	–1.0	0.09	1	µA
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, $V_{IL} = 0.4$ V[2]	I_L	–1.0	0.09	1	µA
Signal high input current, $V_{IH} = 2.0$ V[2]	I_H	–1.0	0.09	1	µA
Output high voltage, $I_{OH} = –2$ mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, $I_{OL} = 3.2$ mA	V_{OL}	—	0	0.4	V
Internal supply current: • Wait mode • Stop mode	 I_{DDW} I_{DDS}	 — —	 375[3] 290[3]	 — —	 mA mA
Typical power at 400 MHz[4]	P	—	1.15	—	W

Notes:
1. See **Figure 2-1** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.2 V core at 25°C junction temperature.
4. The typical power values were measured using an EFR code with the device running at a junction temperature of 25°C. No peripherals were enabled and the ICache was not enabled. The source code was optimized to use all the ALUs and AGUs and all four cores. It was created using CodeWarrior® 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Chapter 4** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

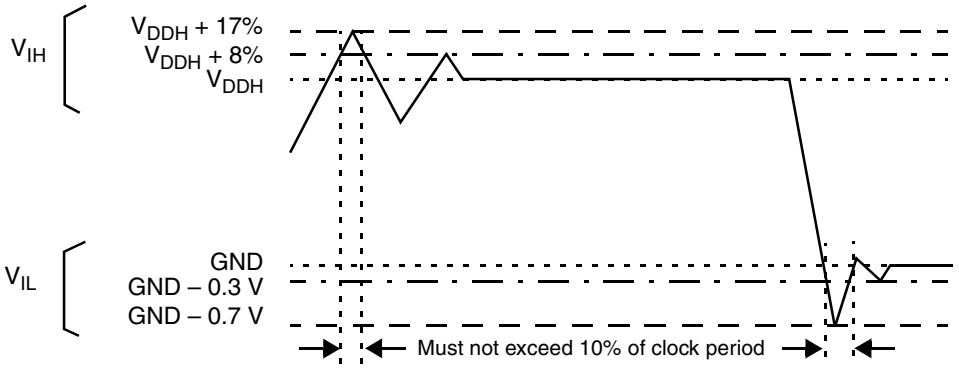

Figure 2-1. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.5 System Bus Access Timing

2.5.5.1 Core Data Transfers

Generally, all MSC8126 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 2-12** shows.

Table 2-12. Tick Spacing for Memory Controller Signals

BCLK/SC140 clock	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:4, 1:6, 1:8, 1:10	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:3	1/6 REFCLK	1/2 REFCLK	4/6 REFCLK
1:5	2/10 REFCLK	1/2 REFCLK	7/10 REFCLK

Figure 2-5 is a graphical representation of **Table 2-12**.

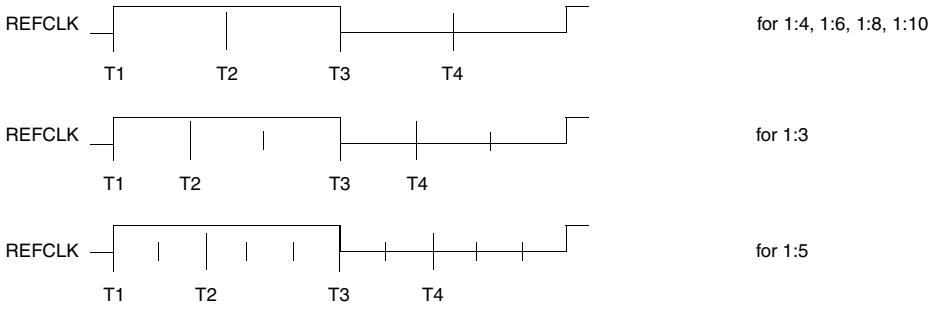

Figure 2-5. Internal Tick Spacing for Memory Controller Signals

2.5.5.2 CLKIN to CLKOUT Skew

Table 2-15 describes the CLKOUT-to-CLKIN skew timing.

Table 2-15. CLKOUT Skew

No.	Characteristic	Min[1]	Max[1]	Units
20	Rise-to-rise skew	0	0.85	ns
21	Fall-to-fall skew	–0.8	1.0	ns
22	CLKOUT phase high and low (1.2 V, 133 MHz)	2.8	—	ns

Notes:
1. A positive number indicates that CLKOUT precedes CLKIN, A negative number indicates that CLKOUT follows CLKIN.
2. Skews are measured in clock mode 29, with a CLKIN:CLKOUT ratio of 1:1. The same skew is valid for all clock modes.
3. CLKOUT skews are measured using a load of 10 pF.
4. CLKOUT skews and phase are not measured for 500/166 Mhz parts because these parts only use CLKIN mode.

For designs that use the CLKOUT synchronization mode, use the skew values listed in **Table 2-15** to adjust the rise-to-fall timing values specified for CLKIN synchronization. **Figure 2-7** shows the relationship between the CLKOUT and CLKIN timings. CLKOUT synchronization mode is not supported above 400 MHz core operation.

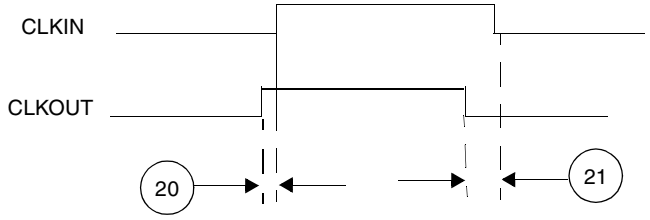

Figure 2-7. CLKOUT and CLKIN Signals.

2.5.5.3 DMA Data Transfers

Table 2-16 describes the DMA signal timing.

Table 2-16. DMA Signals

No.	Characteristic	Ref = CLKIN		Ref = CLKOUT		Units
		Min	Max	Min	Max	
37	DREQ set-up time before the 50% level of the falling edge of REFCLK	5.0	—	5.0	—	ns
38	DREQ hold time after the 50% level of the falling edge of REFCLK	0.5	—	0.5	—	ns
39	$\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK	5.0	—	5.0	—	ns
40	$\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK	0.5	—	0.5	—	ns
41	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge	0.5	7.5	0.5	8.4	ns
Note:	CLKOUT synchronization mode is not supported in cores operating above 400 MHz.					

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-16**. **Figure 2-8** shows synchronous peripheral interaction.

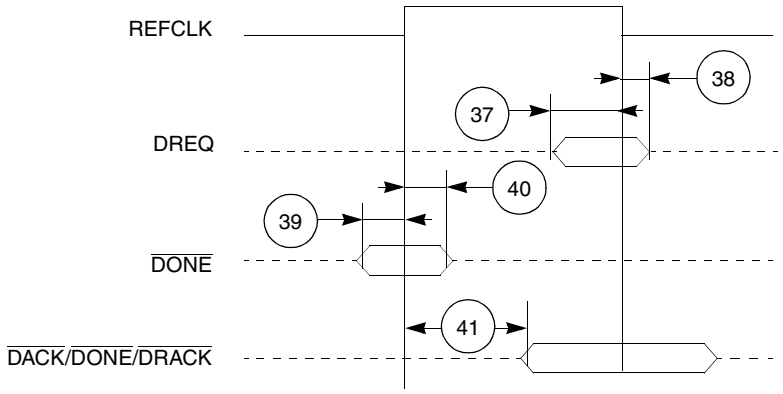

Figure 2-8. DMA Signals

2.5.6.2 DSI Synchronous Mode

Table 2-18. DSI Inputs—Synchronous Mode

No.	Characteristic	Expression	Min	Max	Units
120	HCLKIN Cycle Time[1, 2]	HTC	10.0	55.6	ns
121	HCLKIN high Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
122	HCLKIN low Pulse Width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.4	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes: **1.** Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 2-6** for HCLKIN frequency limits.

Table 2-19. DSI Outputs—Synchronous Mode

No.	Characteristic	Min	Max	Units
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	6.3	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	7.6	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.0	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	5.9	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	6.3	ns

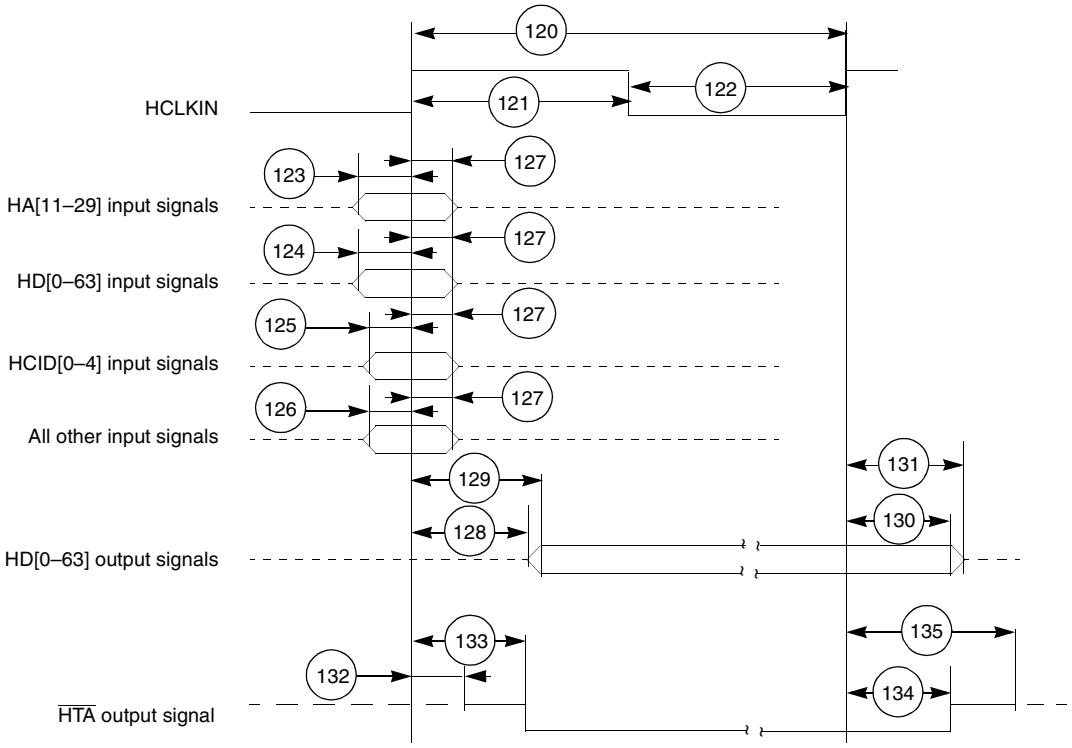

Figure 2-12. DSI Synchronous Mode Signals Timing Diagram

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 2-23. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

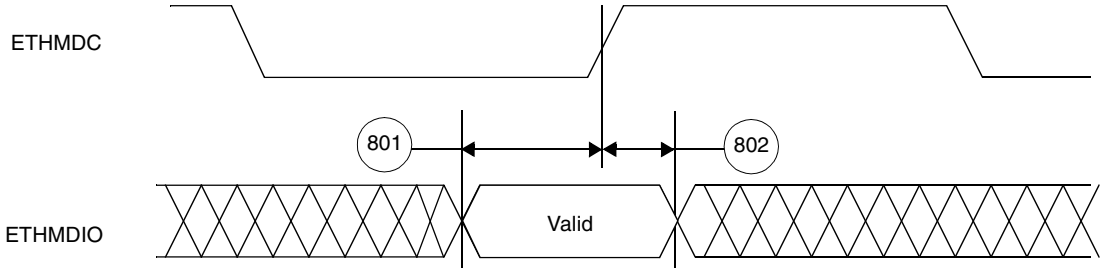

Figure 2-18. MDIO Timing Relationship to MDC

2.5.10.2 MII Mode Timing

Table 2-24. MII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay	1	12.6	ns

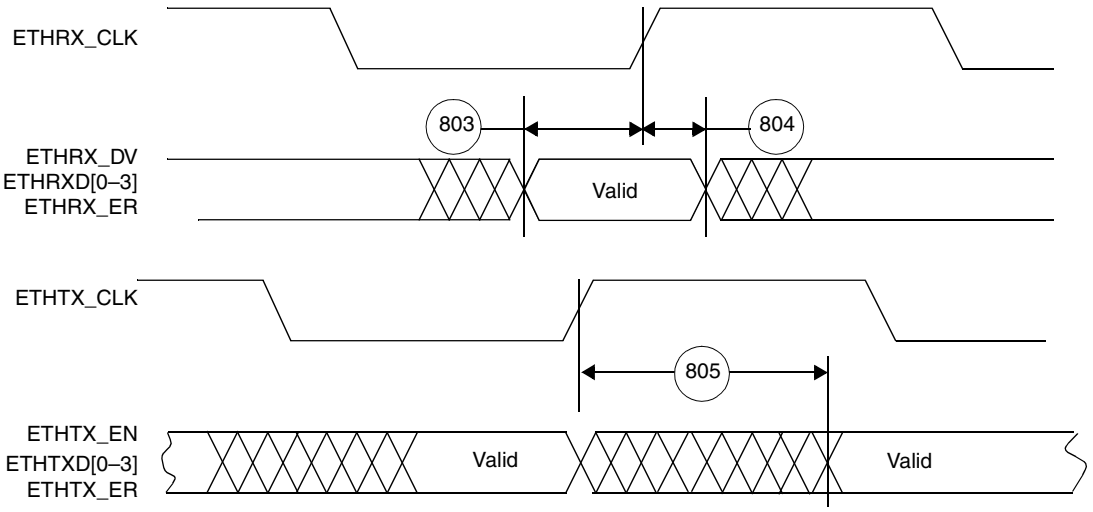

Figure 2-19. MII Mode Signal Timing

Top View

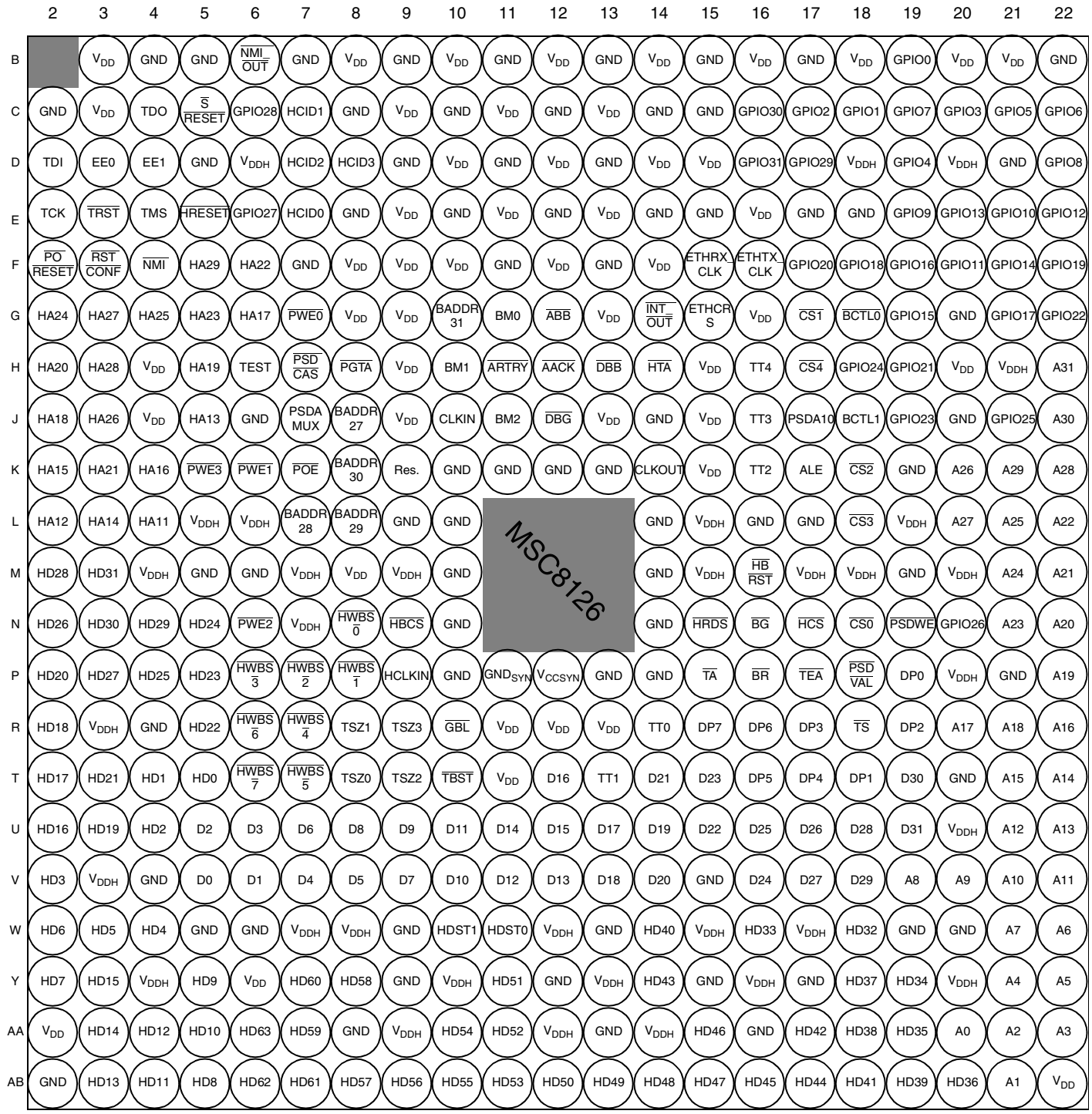

Figure 3-1. MSC8126 Package, Top View

Table 3-1. MSC8126 Signal Listing By Name

Signal Name	Location Designator	Signal Name	Location Designator
A0	AA20	BADDR27	J8
A1	AB21	BADDR28	L7
A2	AA21	BADDR29	L8
A3	AA22	BADDR30	K8
A4	Y21	BADDR31	G10
A5	Y22	$\overline{\text{BCTL0}}$	G18
A6	W22	$\overline{\text{BCTL1}}$	J18
A7	W21	$\overline{\text{BG}}$	N16
A8	V19	BNKSEL0	G11
A9	V20	BNKSEL1	H10
A10	V21	BNKSEL2	J11
A11	V22	BM0	G11
A12	U21	BM1	H10
A13	U22	BM2	J11
A14	T22	$\overline{\text{BR}}$	P16
A15	T21	CHIP_ID0	B19
A16	R22	CHIP_ID1	C18
A17	R20	CHIP_ID2	C17
A18	R21	CHIP_ID3	D17
A19	P22	CLKIN	J10
A20	N22	CLKOUT	K14
A21	M22	CNFGS	W3
A22	L22	$\overline{\text{CS0}}$	N18
A23	N21	$\overline{\text{CS1}}$	G17
A24	M21	$\overline{\text{CS2}}$	K18
A25	L21	$\overline{\text{CS3}}$	L18
A26	K20	$\overline{\text{CS4}}$	H17
A27	L20	$\overline{\text{CS5}}$	K16
A28	K22	$\overline{\text{CS5}}$	J18
A29	K21	$\overline{\text{CS6}}$	J16
A30	J22	$\overline{\text{CS7}}$	H16
A31	H22	D0	V5
$\overline{\text{AACK}}$	H12	D1	V6
$\overline{\text{ABB}}$	G12	D2	U5
ALE	K17	D3	U6
$\overline{\text{ARTRY}}$	H11	D4	V7

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
D5	V8	D41	AB18
D6	U7	D42	AA17
D7	V9	D43	Y14
D8	U8	D44	AB17
D9	U9	D45	AB16
D10	V10	D46	AA15
D11	U10	D47	AB15
D12	V11	D48	AB14
D13	V12	D49	AB13
D14	U11	D50	AB12
D15	U12	D51	Y11
D16	T12	D52	AA11
D17	U13	D53	AB11
D18	V13	D54	AA10
D19	U14	D55	AB10
D20	V14	D56	AB9
D21	T14	D57	AB8
D22	U15	D58	Y8
D23	T15	D59	AA7
D24	V16	D60	Y7
D25	U16	D61	AB7
D26	U17	D62	AB6
D27	V17	D63	AA6
D28	U18	$\overline{\text{DACK1}}$	G21
D29	V18	$\overline{\text{DACK1}}$	T18
D30	T19	$\overline{\text{DACK2}}$	F22
D31	U19	$\overline{\text{DACK2}}$	R19
D32	W18	$\overline{\text{DACK3}}$	T17
D33	W16	$\overline{\text{DACK4}}$	T16
D34	Y19	$\overline{\text{DBB}}$	H13
D35	AA19	$\overline{\text{DBG}}$	J12
D36	AB20	$\overline{\text{DONE1}}$	F19
D37	Y18	$\overline{\text{DONE2}}$	G22
D38	AA18	DP0	P19
D39	AB19	DP1	T18
D40	W14	DP2	R19

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
GPIO3	C20	HA14	L3
GPIO4	D19	HA15	K2
GPIO5	C21	HA16	K4
GPIO6	C22	HA17	G6
GPIO7	C19	HA18	J2
GPIO8	D22	HA19	H5
GPIO9	E19	HA20	H2
GPIO10	E21	HA21	K3
GPIO11	F20	HA22	F6
GPIO12	E22	HA23	G5
GPIO13	E20	HA24	G2
GPIO14	F21	HA25	G4
GPIO15	G19	HA26	J3
GPIO16	F19	HA27	G3
GPIO17	G21	HA28	H3
GPIO18	F18	HA29	F5
GPIO19	F22	$\overline{\text{HBCS}}$	N9
GPIO20	F17	$\overline{\text{HBRST}}$	M16
GPIO21	H19	HCID0	E7
GPIO22	G22	HCID1	C7
GPIO23	J19	HCID2	D7
GPIO24	H18	HCID3	D8
GPIO25	J21	HCLKIN	P9
GPIO26	N20	$\overline{\text{HCS}}$	N17
GPIO27	E6	HD0	T5
GPIO28	C6	HD1	T4
GPIO29	D17	HD2	U4
GPIO30	C16	HD3	V2
GPIO31	D16	HD4	W4
HA7	R14	HD5	W3
HA8	D8	HD6	W2
HA9	W11	HD7	Y2
HA10	W10	HD8	AB5
HA11	L4	HD9	Y5
HA12	L2	HD10	AA5
HA13	J5	HD11	AB4

Table 3-1. MSC8126 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
TIMER1	C17	V_{DD}	E11
TIMER2	C16	V_{DD}	E13
TIMER3	D16	V_{DD}	E16
TMCLK	C16	V_{DD}	F8
TMS	E4	V_{DD}	F9
$\overline{TRST}$	E3	V_{DD}	F10
$\overline{TS}$	R18	V_{DD}	F12
TSZ0	T8	V_{DD}	F14
TSZ1	R8	V_{DD}	G8
TSZ2	T9	V_{DD}	G9
TSZ3	R9	V_{DD}	G13
TT0	R14	V_{DD}	G16
TT1	T13	V_{DD}	H4
TT2	K16	V_{DD}	H9
TT3	J16	V_{DD}	H15
TT4	H16	V_{DD}	H20
URXD	E6	V_{DD}	J4
UTXD	C6	V_{DD}	J9
V_{CCSYN}	P12	V_{DD}	J13
V_{DD}	B8	V_{DD}	J15
V_{DD}	B10	V_{DD}	K15
V_{DD}	B12	V_{DD}	M8
V_{DD}	B14	V_{DD}	R11
V_{DD}	B16	V_{DD}	R12
V_{DD}	B18	V_{DD}	R13
V_{DD}	B20	V_{DD}	T11
V_{DD}	B21	V_{DD}	Y6
V_{DD}	C3	V_{DD}	AA2
V_{DD}	C9	V_{DD}	B3
V_{DD}	C11	V_{DD}	AB22
V_{DD}	C13	V_{DDH}	D6
V_{DD}	D10	V_{DDH}	D18
V_{DD}	D12	V_{DDH}	D20
V_{DD}	D14	V_{DDH}	H21
V_{DD}	D15	V_{DDH}	L5
V_{DD}	E9	V_{DDH}	L6

Table 3-2. MSC8126 Signal Listing by Ball Designator

Des.	Signal Name	Des.	Signal Name
B3	V_{DD}	C18	GPIO1/TIMER0/CHIP_ID1/$\overline{\text{IRQ5}}$/ETHTXD1
B4	GND	C19	GPIO7/TDM3RCLK/$\overline{\text{IRQ5}}$/ETHTXD3
B5	GND	C20	GPIO3/TDM3TSYN/$\overline{\text{IRQ1}}$/ETHTXD2
B6	$\overline{\text{NMI\_OUT}}$	C21	GPIO5/TDM3TDAT/$\overline{\text{IRQ3}}$/ETHRXD3
B7	GND	C22	GPIO6/TDM3RSYN/$\overline{\text{IRQ4}}$/ETHRXD2
B8	V_{DD}	D2	TDI
B9	GND	D3	EE0
B10	V_{DD}	D4	EE1
B11	GND	D5	GND
B12	V_{DD}	D6	V_{DDH}
B13	GND	D7	HCID2
B14	V_{DD}	D8	HCID3/HA8
B15	GND	D9	GND
B16	V_{DD}	D10	V_{DD}
B17	GND	D11	GND
B18	V_{DD}	D12	V_{DD}
B19	GPIO0/CHIP_ID0/$\overline{\text{IRQ4}}$/ETHTXD0	D13	GND
B20	V_{DD}	D14	V_{DD}
B21	V_{DD}	D15	V_{DD}
B22	GND	D16	GPIO31/TIMER3/SCL
C2	GND	D17	GPIO29/CHIP_ID3/ETHTX_EN
C3	V_{DD}	D18	V_{DDH}
C4	TDO	D19	GPIO4/TDM3TCLK/$\overline{\text{IRQ2}}$/ETHTX_ER
C5	$\overline{\text{SRESET}}$	D20	V_{DDH}
C6	GPIO28/DREQ2/UTXD	D21	GND
C7	HCID1	D22	GPIO8/TDM3RDAT/$\overline{\text{IRQ6}}$/ETHCOL
C8	GND	E2	TCK
C9	V_{DD}	E3	$\overline{\text{TRST}}$
C10	GND	E4	TMS
C11	V_{DD}	E5	$\overline{\text{HRESET}}$
C12	GND	E6	GPIO27/DREQ1/URXD
C13	V_{DD}	E7	HCID0
C14	GND	E8	GND
C15	GND	E9	V_{DD}
C16	GPIO30/TIMER2/TMCLK/SDA	E10	GND
C17	GPIO2/TIMER1/CHIP_ID2/$\overline{\text{IRQ6}}$	E11	V_{DD}

Table 3-2. MSC8126 Signal Listing by Ball Designator (Continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{\text{HBRST}}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{\text{TA}}$
M19	GND	P16	$\overline{\text{BR}}$
M20	V_{DDH}	P17	$\overline{\text{TEA}}$
M21	A24	P18	$\overline{\text{PSDVAL}}$
M22	A21	P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$	R5	HD22
N9	$\overline{\text{HBCS}}$	R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
N10	GND	R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
N14	GND	R8	TSZ1
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	R9	TSZ3
N16	$\overline{\text{BG}}$	R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
N17	$\overline{\text{HCS}}$	R11	V_{DD}
N18	$\overline{\text{CS0}}$	R12	V_{DD}
N19	$\overline{\text{PSDWE}}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
N22	A20	R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
P2	HD20	R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
P3	HD27	R18	$\overline{\text{TS}}$
P4	HD25	R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
P5	HD23	R20	A17
P6	$\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$	R21	A18
P7	$\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$	R22	A16
P8	$\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

4.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to the non-active value, via resistors to V_{DDH} or GND, except for the following:

- If the DSI is unused (DDR[DSIDIS] is set), $\overline{\text{HCS}}$ and $\overline{\text{HBCS}}$ must pulled up and all the rest of the DSI signals can be disconnected.
- When the DSI uses synchronous mode, $\overline{\text{HTA}}$ must be pulled up. In asynchronous mode, $\overline{\text{HTA}}$ should be pulled either up or down, depending on design requirements.
- $\overline{\text{HDST}}$ can be disconnected if the DSI is in big-endian mode, or if the DSI is in little-endian mode and the DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, pull up $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ and $\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/$\overline{\text{PSDDQM[4–7]}}$/$\overline{\text{PBS[4–7]}}$.
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ must be pulled up.
- When the DSI is in asynchronous mode, $\overline{\text{HBRST}}$ and HCLKIN should either be disconnected or pulled up.
- The following signals must be pulled up: $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{PSDVAL}}$, and $\overline{\text{AACK}}$.
- In single-master mode (BCR[EBM] = 0) with internal arbitration (PPC_ACR[EARB] = 0):
  - $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ can be left unconnected.
  - $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, and $\overline{\text{GBL}}$ can be left unconnected if they are multiplexed to the system bus functionality. For any other functionality, connect the signal lines based on the multiplexed functionality.
  - $\overline{\text{BR}}$ must be pulled up.
  - $\overline{\text{EXT\_BR[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- If there is an external bus master (BCR[EBM] = 1):
  - $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ must be pulled up.
  - $\overline{\text{EXT\_BR[2–3]}}$, $\overline{\text{EXT\_BG[2–3]}}$, and $\overline{\text{EXT\_DBG[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- In single-master mode, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ can be selected as $\overline{\text{IRQ}}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.

Note: The MSC8126 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8126 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.