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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	DAI/O, EBI/EMI, I²C, Parallel, SPI
Clock Rate	150MHz
Non-Volatile Memory	ROM (128kB)
On-Chip RAM	82kB
Voltage - I/O	3.3V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/cs495314-cvz

Table of Contents

4 Hardware Functional Description

4.1 Coyote 32-bit DSP Core

The CS4953xx is a dual-core DSP with separate X and Y data and P code memory spaces. Each core is a high-performance, 32-bit, user-programmable, fixed-point DSP that is capable of performing two multiply accumulate (MAC) operations per clock cycle. Each core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

Both DSP cores are coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the digital audio input (DAI) and digital audio output (DAO), external memory, or any DSP core memory, all without the intervention of the DSP. The DMA engine offloads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS4953xx functionality is controlled by application codes that are stored in on-board ROM or downloaded to the CS4953xx from a host MCU or external FLASH/EEPROM. Users can choose to use standard audio decoder and post-processor modules which are available from Cirrus Logic.

The CS4953xx is suitable for audio decoder, audio post-processor, audio encoder, DVD audio/video player, and digital broadcast decoder applications.

4.1.1 DSP Memory

Each DSP core has its own on-chip data and program RAM and ROM and does not require external memory for any of today's popular audio algorithms including Dolby Digital Surround EX, AAC Multichannel, DTS-ES 96/24, and THX Ultra2.

The memory maps for the DSPs are as follows. All memory sizes are composed of 32-bit words.

Table 3. CS49530x DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16K SRAM, 16K ROM	10K SRAM, 8K ROM
Y	16K SRAM, 32K ROM	16K SRAM, 16K ROM
P	8K SRAM, 32K ROM	8K SRAM, 24K ROM

Table 4. CS49531x DSP Memory Sizes

Memory Type	DSP A	DSP B
X	16K SRAM, 16K ROM	10K SRAM, 8K ROM
Y	24K SRAM, 32K ROM	16K SRAM, 16K ROM
P	8K SRAM, 32K ROM	8K SRAM, 24K ROM

4.1.2 DMA Controller

The powerful 12-channel DMA controller can move data between eight on-chip resources. Each resource has its own arbiter: X, Y, and P RAM/ROMs on DSP A; X, Y, and P RAM/ROMs on DSP B; external memory; and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service interval for each DMA channel as well as up to six interrupt events, is programmable.

5.5 Thermal Data (144-pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		—	48	—	
Four-layer Board[2]		—	40	—	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		—	.39	—	
Four-layer Board[2]		—	.33	—	

5.6 Thermal Data (128-pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{ja}				°C / Watt
Two-layer Board[1]		—	53	—	
Four-layer Board[2]		—	44	—	
Thermal Resistance (Junction to Top of Package)	ψ_{jt}				°C / Watt
Two-layer Board[1]		—	.45	—	
Four-layer Board[2]		—	.39	—	

Notes: 1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz copper covering 20 % of the top & bottom layers.

2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-ounce copper covering 20 % of the top & bottom layers and 0.5-ounce copper covering 90 % of the internal power plane and ground plane layers.

3. To calculate the die temperature for a given power dissipation

$$T_j = \text{Ambient Temperature} + [\ (\text{Power Dissipation in Watts}) * \theta_{ja}\ ]$$

4. To calculate the case temperature for a given power dissipation

$$T_c = T_j - [\ (\text{Power Dissipation in Watts}) * \psi_{jt}\ ]$$

5.7 Switching Characteristics—$\overline{\text{RESET}}$

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low	T_{rstl}	1	—	µs
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	/m	100	ns
Configuration pins setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	—	ns
Configuration pins hold after $\overline{\text{RESET}}$ high	T_{rsthld}	20	—	ns

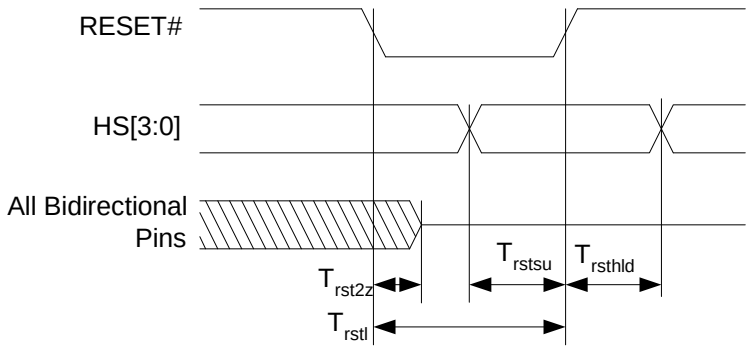


Figure 1. $\overline{\text{RESET}}$ Timing

5.8 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency[1]	F_{xtal}	12.288	24.576	MHz
XTI period	T_{clki}	41	81.4	ns
XTI high time	T_{clkih}	16.4	/m	ns
XTI low time	T_{clkil}	16.4	—	ns
External Crystal Load Capacitance (parallel resonant)[2]	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR	—	50	Ω

1. Part characterized with the following crystal frequency values: 12.288 and 24.576
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals which require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

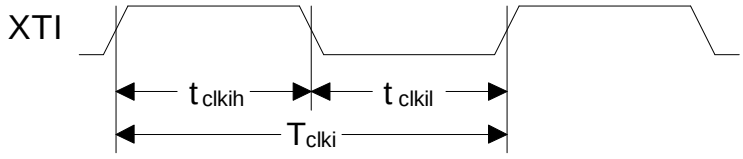


Figure 2. XTI Timing

5.10 Switching Characteristics — Serial Control Port - SPI Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	25	MHz
SCP_CS falling to SCP_CLK rising[2]	t_{spicss}	24	—	—	ns
SCP_CLK low time[2]	t_{spickl}	20	—	—	ns
SCP_CLK high time[2]	t_{spickh}	20	—	—	ns
Setup time SCP_MOSI input	t_{spidsu}	5	—	—	ns
Hold time SCP_MOSI input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MISO output valid[2]	t_{spidov}	—	—	11	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising[2]	$t_{spiirqh}$	—	—	20	ns
$\overline{\text{SCP\_CS}}$ rising to $\overline{\text{SCP\_IRQ}}$ falling[2]	$t_{spiirql}$	0	—	—	ns
SCP_CLK low to $\overline{\text{SCP\_CS}}$ rising[2]	t_{spicsh}	24	—	—	ns
$\overline{\text{SCP\_CS}}$ rising to SCP_MISO output high-Z	$t_{spicsdz}$	—	20	—	ns
SCP_CLK rising to $\overline{\text{SCP\_BSY}}$ falling[2]	$t_{spicbsyl}$	—	3∗DCLKP+20	—	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{xtal}/3$.
2. When SCP1 is in SPI slave mode, very slow rise and fall times of the SCP_CLK edges may make the edges of the SCP_CLK more susceptible to noise, resulting in non-smooth edges. Any glitch at the threshold levels of the SCP port input signals could result in abnormal operation of the port.

   In systems that have noise coupling onto SCP_CLK, slow rise and fall times may cause host communication problems. Increasing rise time makes host communication more reliable.

5.11 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1,2]	f_{spisck}	—	—	$F_{xtal}/2$	MHz
$\overline{SCP\_CS}$ falling to SCP_CLK rising [3]	t_{spicss}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
SCP_CLK low time	t_{spickl}	16.9	—	—	ns
SCP_CLK high time	t_{spickh}	16.9	—	—	ns
Setup time SCP_MISO input	t_{spidsu}	11	—	—	ns
Hold time SCP_MISO input	t_{spidh}	5	—	—	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	—	—	11	ns
SCP_CLK low to $\overline{SCP\_CS}$ falling	t_{spicsl}	7	—	—	ns
SCP_CLK low to $\overline{SCP\_CS}$ rising	t_{spicsh}	—	11*DCLKP + (SCP_CLK PERIOD)/2	—	ns
Bus free time between active $\overline{SCP\_CS}$	t_{spicsx}	—	3*DCLKP	—	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	—	—	20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See Section 5.8.
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter

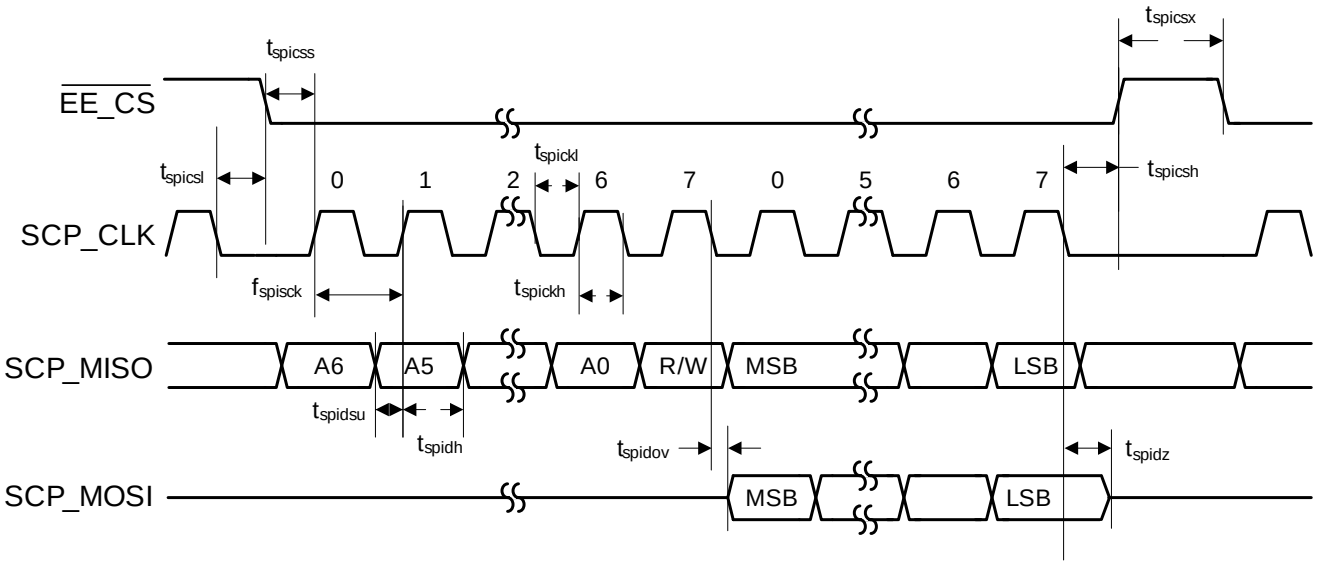


Figure 4. Serial Control Port - SPI Master Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency[1]	f_{iicck}	—	—	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	—	—	µs
SCP_CLK high time	t_{iicckh}	1.25	—	—	µs
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25	—	—	µs
START condition to SCP_CLK falling	$t_{iicstscl}$	1.25	—	—	µs
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	—	—	µs
Bus free time between STOP and START conditions	t_{iicbft}	3	—	—	µs
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100	—	—	ns
Hold time SCP_SDA input after SCP_CLK falling[2]	t_{iich}	0	—	—	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	—	—	18	ns
SCP_CLK falling to $\overline{\text{SCP\_IRQ}}$ rising	$t_{iicirqh}$	—	—	3∗DCLKP + 40	ns
NAK condition to $\overline{\text{SCP\_IRQ}}$ low	$t_{iicirql}$	—	3∗DCLKP + 20	—	ns
SCP_CLK rising to $\overline{\text{SCB\_BSY}}$ low	$t_{iicbsyl}$	—	3∗DCLKP + 20	—	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP\_BSY}}$ pin should be implemented to prevent overflow of the input data buffer.
2. This parameter is measured from the ViL level at the falling edge of the clock.

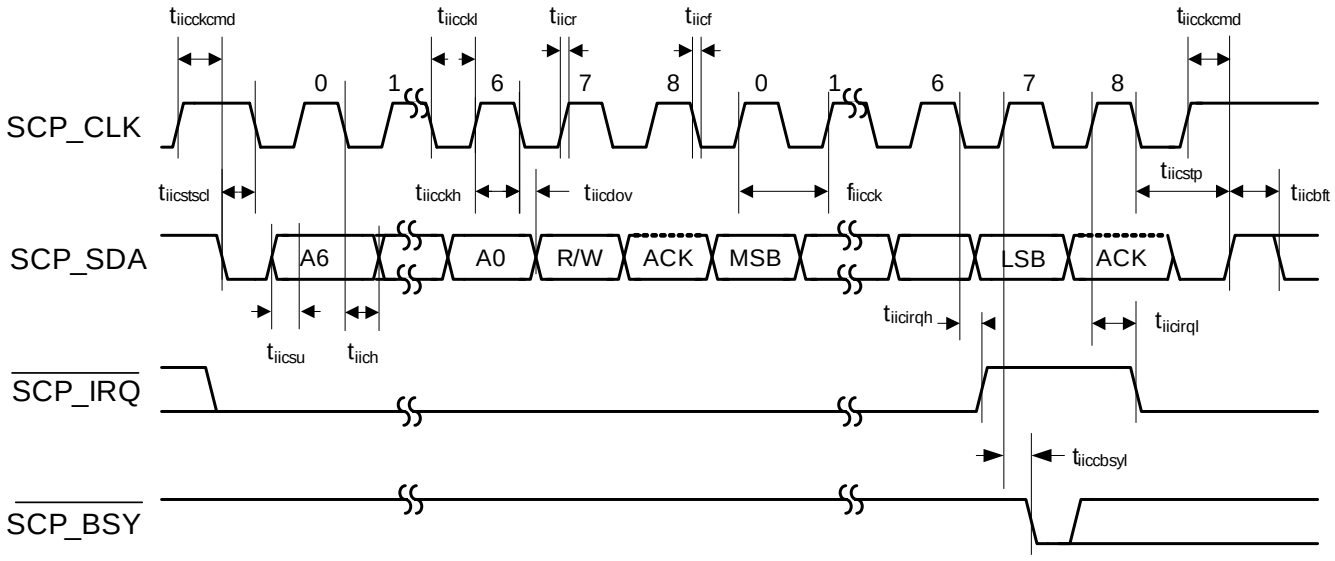


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.14 Switching Characteristics — Parallel Control Port - Intel Slave Mode

Parameter	Symbol	Min	Typical	Max	Unit
Address setup before PCP_CS and PCP_RD low or PCP_CS and PCP_WR low	t_{ias}	5	—	—	ns
Address hold time after PCP_CS and PCP_RD low or PCP_CS and PCP_WR high	t_{iah}	5	—	—	ns
Read					
Delay between PCP_RD then PCP_CS low or PCP_CS then PCP_RD low	t_{icdr}	0	—	—	ns
Data valid after PCP_CS and PCP_RD low	t_{idd}	—	—	18	ns
PCP_CS and PCP_RD low for read	t_{irpw}	24	—	—	ns
Data hold time after PCP_CS or PCP_RD high	t_{idhr}	8	—	—	ns
Data high-Z after PCP_CS or PCP_RD high	t_{idis}	—	—	18	ns
PCP_CS or PCP_RD high to PCP_CS and PCP_RD low for next read[1]	t_{ird}	30	—	—	ns
PCP_CS or PCP_RD high to PCP_CS and PCP_WR low for next write[1]	t_{irdtw}	30	—	—	ns
PCP_RD rising to PCP_IRQ rising	$t_{irdirqhl}$	—	—	12	ns
Write					
Delay between PCP_WR then PCP_CS low or PCP_CS then PCP_WR low	t_{icdw}	0	—	—	ns
Data setup before PCP_CS or PCP_WR high	t_{idsu}	8	—	—	ns
PCP_CS and PCP_WR low for write	t_{iwpw}	24	—	—	ns
Data hold after PCP_CS or PCP_WR high	t_{idhw}	8	—	—	ns
PCP_CS or PCP_WR high to PCP_CS and PCP_RD low for next read[1]	t_{iwtrd}	30	—	—	ns
PCP_CS or PCP_WR high to PCP_CS and PCP_WR low for next write[1]	t_{iwd}	30	—	—	ns
PCP_WR rising to PCP_BSY falling	$t_{iwrbsyl}$	—	2*DCLKP + 20	—	ns

1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the PCP_BSY pin/bit should be observed to prevent overflowing the input data buffer. AN288 *CS4953xx /CS497xxx Firmware User's Manual* should be consulted for the firmware speed limitations.

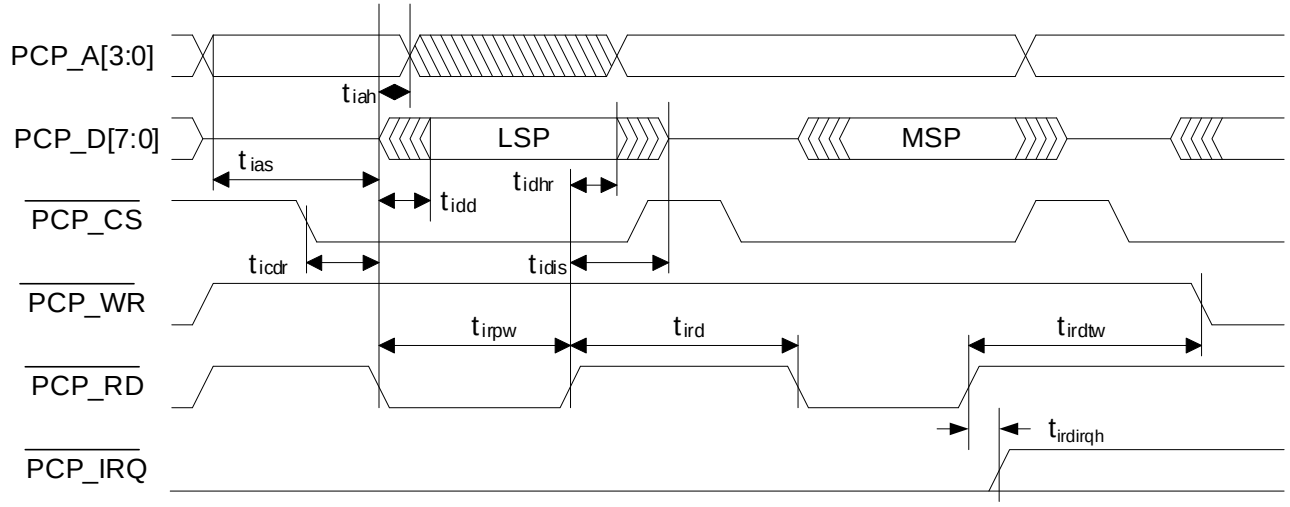


Figure 7. Parallel Control Port - Intel Slave Mode Read Cycle

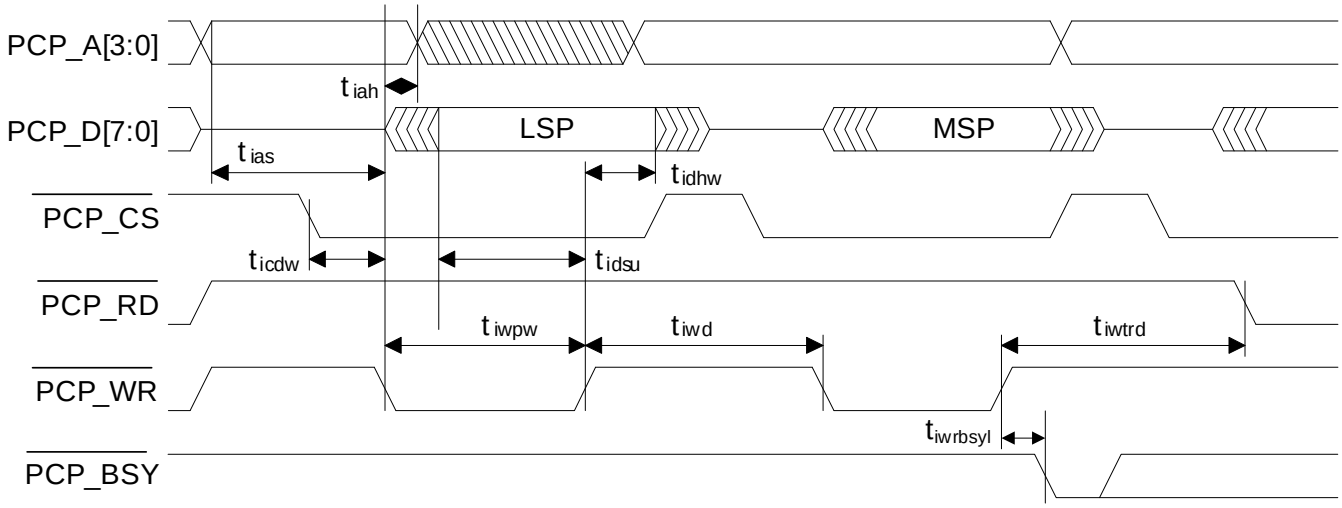


Figure 8. Parallel Control Port - Intel Slave Mode Write Cycle

5.16 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	—	ns
DAI_SCLK duty cycle	—	45	55	%
DAI_LRCLK transition from DAI_SCLK active edge	$t_{daisstlr}$	10	—	ns
DAI_SCLK active edge from DAI_LRCLK transition	$t_{daislrts}$	10	—	ns
Setup time DAI_DATAn	t_{daidsu}	10	—	ns
Hold time DAI_DATAn	t_{daidh}	5	—	ns

Note: In these diagrams, falling edge is the inactive edge of DAI_SCLK.

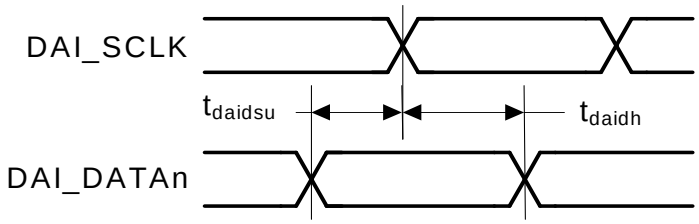


Figure 11. Digital Audio Input (DAI) Port Timing Diagram

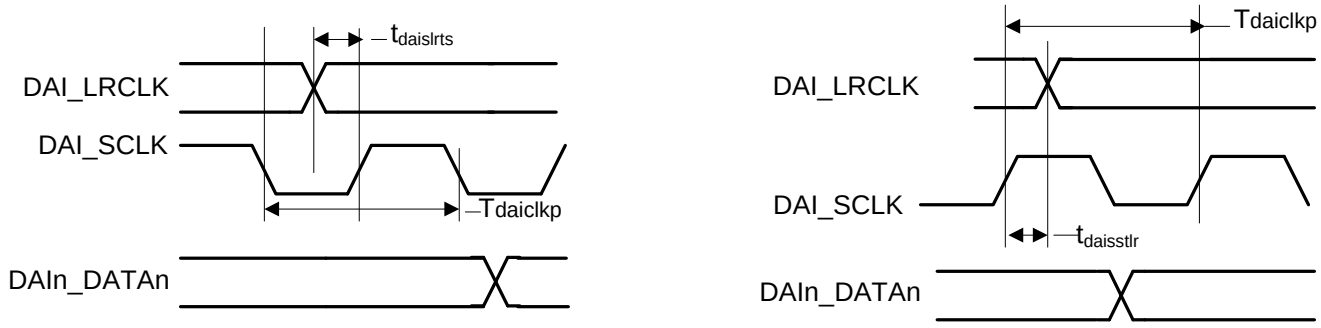
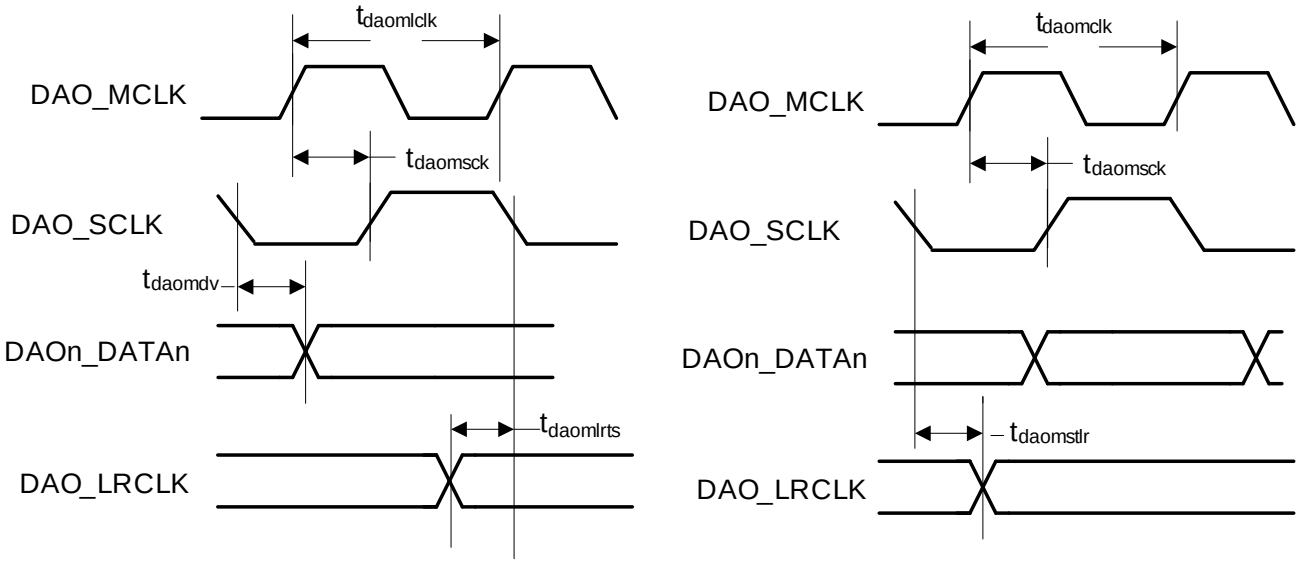


Figure 12. DAI Slave Timing Diagram

5.17 Switching Characteristics — Digital Audio Output Port

Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	—	ns
DAO_MCLK duty cycle	—	45	55	%
DAO_SCLK period for Master or Slave mode[1]	$T_{daosclk}$	40	—	ns
DAO_SCLK duty cycle for Master or Slave mode[1]	—	40	60	%
Master Mode (Output A1 Mode)[1,2]				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	—	19	ns
DAO_SCLK delay from DAO_LRCLK transition[3]	$t_{daomlrts}$	—	8	ns
DAO_LRCLK delay from DAO_SCLK transition[3]	$t_{daomstlr}$	—	8	ns
DAO1_DATA[3:0], DAO2_DATA[1:0] delay from DAO_SCLK transition[3]	t_{daomdv}	—	10	ns
Slave Mode (Output A0 Mode)[4]				
DAO_SCLK active edge to DAO_LRCLK transition	$t_{daosstlr}$	10	—	ns
DAO_LRCLK transition to DAO_SCLK active edge	$t_{daoslrts}$	10	—	ns
DAO_Dx delay from DAO_SCLK inactive edge	t_{daosdv}	—	12.5	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS4953xx driving both DAO_SCLK and DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 13. Digital Audio Port Output Timing Master Mode

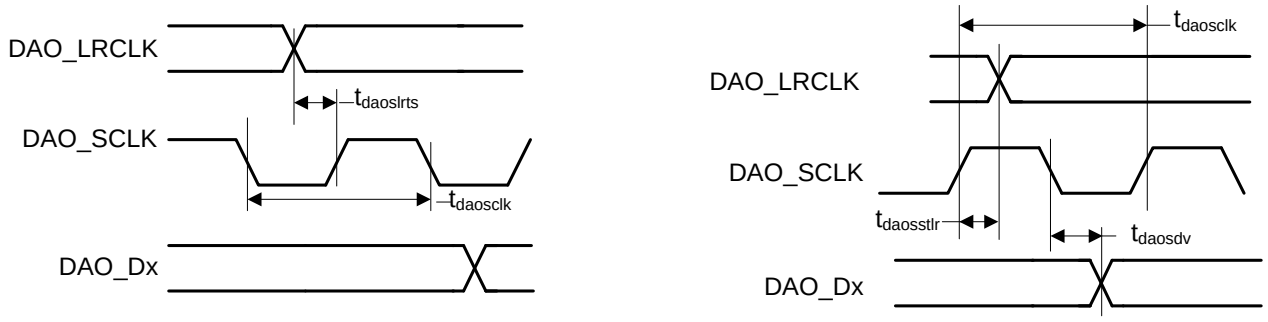


Figure 14. Digital Audio Output Timing, Slave Mode

5.18 Switching Characteristics — SDRAM Interface

Refer to Figure 15 through Figure 18.

(SD_CLKOUT = SD_CLKIN)

Parameter	Symbol	Min	Typical	Max	Unit
SD_CLKIN high time	t_{sdclkh}	2.3	—	—	ns
SD_CLKIN low time	t_{sdclkl}	2.3	—	—	ns
SD_CLKOUT rise/fall time	$t_{sdclkrf}$	—	—	1	ns
SD_CLKOUT Frequency	—	—	150	—	MHz
SD_CLKOUT duty cycle	—	45	—	55	%
SD_CLKOUT rising edge to signal valid	t_{sdcmdv}	—	—	3.8	ns
Signal hold from SD_CLKOUT rising edge	t_{sdcmdh}	—	1.1	—	ns
SD_CLKOUT rising edge to SD_DQMn valid	t_{sddqv}	—	3.8	—	ns
SD_DQMn hold from SD_CLKOUT rising edge	t_{sddqh}	1.38	—	—	ns
SD_DATA valid setup to SD_CLKIN rising edge	t_{sddsu}	1.3	—	—	ns
SD_DATA valid hold to SD_CLKIN rising edge	t_{sddh}	2.1	—	—	ns
SD_CLKOUT rising edge to ADDRn valid	t_{sdav}	—	3.8	—	ns

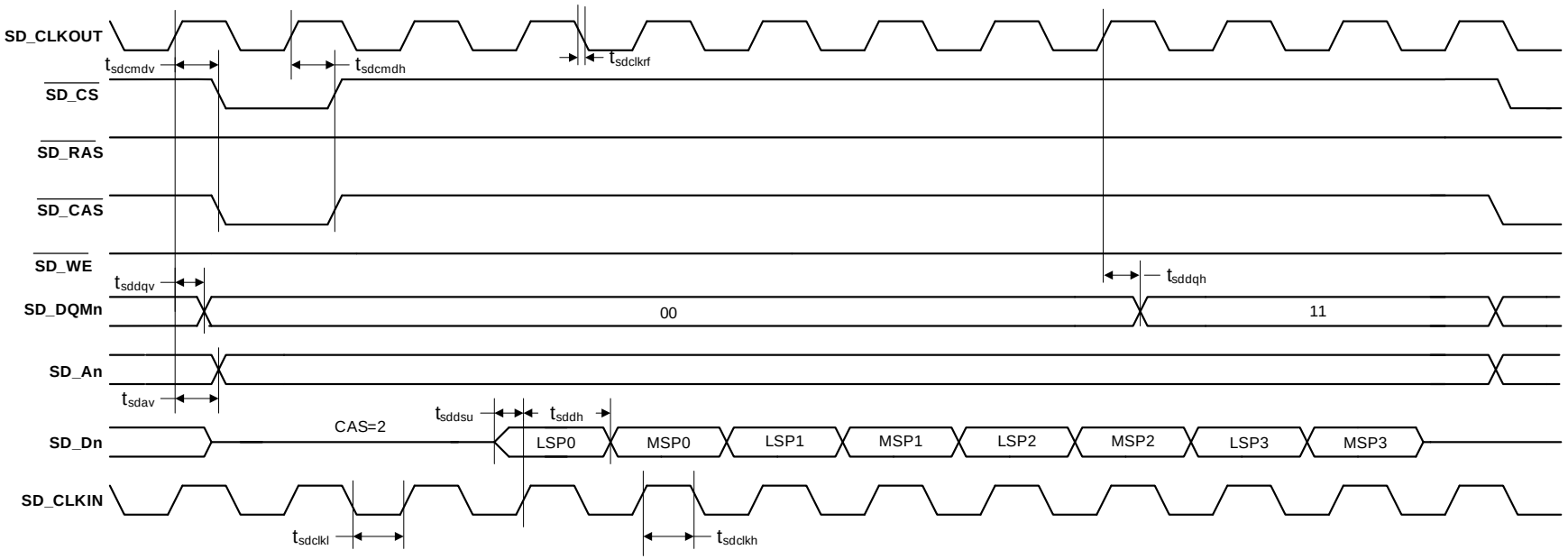


Figure 15. External Memory Interface - SDRAM Burst Read Cycle

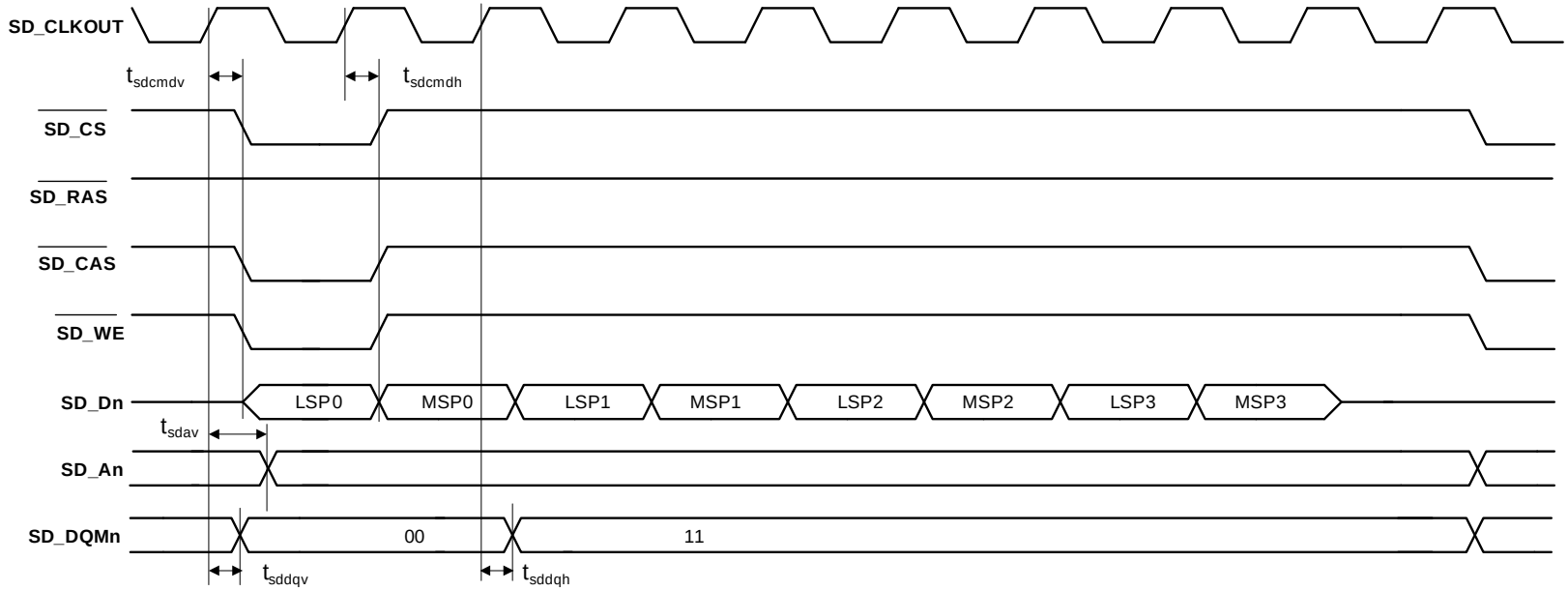


Figure 16. External Memory Interface - SDRAM Burst Write Cycle

6 Ordering Information

The CS4953xx family part number is described as follows:

CS495NNI-XYZ

where

NN - Product Number Variant

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

Table 5. Ordering Information

Part No.	Status	Grade	Temp. Range	Package	Status
CS495303-CVZ	NRND	Commercial	0 to +70 °C	128-pin LQFP	—
CS495303-CVZR[1]	NRND				—
CS495303-CQZ	EOL			144-pin LQFP	—
CS495304-CVZ	EOL			128-pin LQFP	—
CS495304-CVZR[1]	EOL				—
CS495304-DVZ	EOL	Automotive	-40 to +85 °C	128-pin LQFP	—
CS495304-DVZR[1]	EOL				—
CS495313-CQZ	EOL	Commercial	0 to +70 °C	144-pin LQFP	—
CS495313-CQZR[1]	EOL				—
CS495313-CVZ	NRND	Commercial	0 to +70 °C	128-pin LQFP	—
CS495313-CVZR[1]	NRND				—
CS495314-CVZ[2]	Active	Commercial	0 to +70 °C	128-pin LQFP	—
CS495314-CVZR[1,2]	Active				—
CS495314-CQZ	EOL			144-pin LQFP	—
CS495314-DVZ	Active			128-pin LQFP	—
CS495314-DVZR[1]	Note [3]	Automotive	-40 to +85 °C	128-pin LQFP	—

1. R = Tape and Reel
2. Recommended for new designs. See Section 2 for details about Cirrus Logic design recommendations.
3. Contact the factory for availability of the -D (automotive grade) package

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7 Environmental, Manufacturing, and Handling Information

Table 6. Environmental, Manufacturing, and Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS495303-CVZ	260 °C	3	7 Days
CS495303-CVZR			
CS495304-CVZ			
CS495304-CVZR			
CS495304-DVZ			
CS495304-DVZR			
CS495313-CQZ			
CS495313-CQZR			
CS495313-CVZ			
CS495313-CVZR			
CS495314-CVZ			
CS495314-CVZR			
CS495314-DVZ			
CS495314-DVZR			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8 Device Pinout Diagrams

8.1 128-pin LQFP Pinout Diagrams (CS495303/CS495313)

The CS495303/CS495313 DSP with a 128-pin package is **not** recommended for new designs. See Section 2 for details about this Cirrus Logic recommendation.

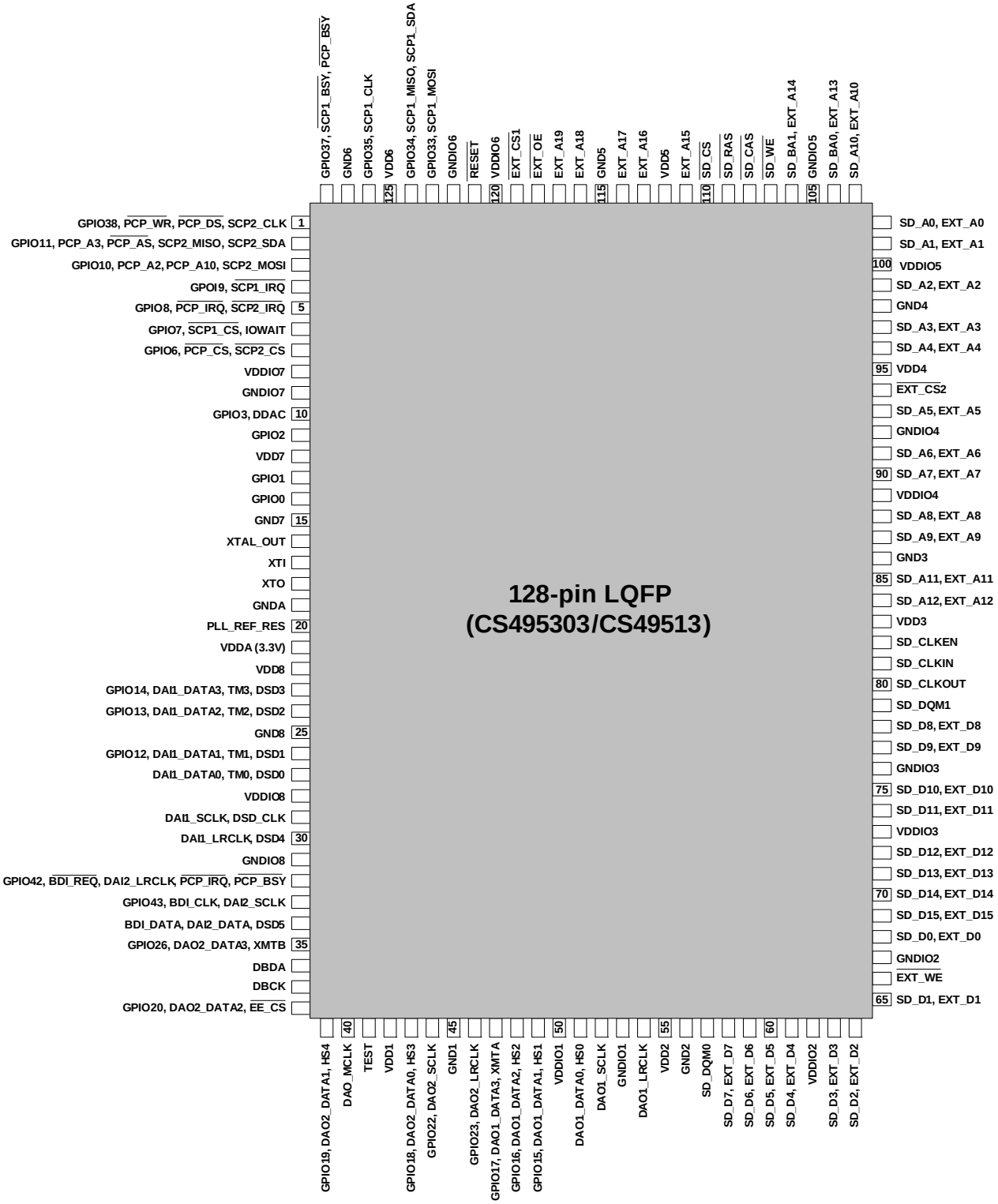

Figure 19. 128-pin LQFP Pin-Out Drawing (CS495303/CS495313)

8.3 144-pin LQFP Pinout Diagrams (CS495313)

The CS495313 DSP with a 144-pin package is **not** recommended for new designs. See Section 2 for details about this Cirrus Logic recommendation.

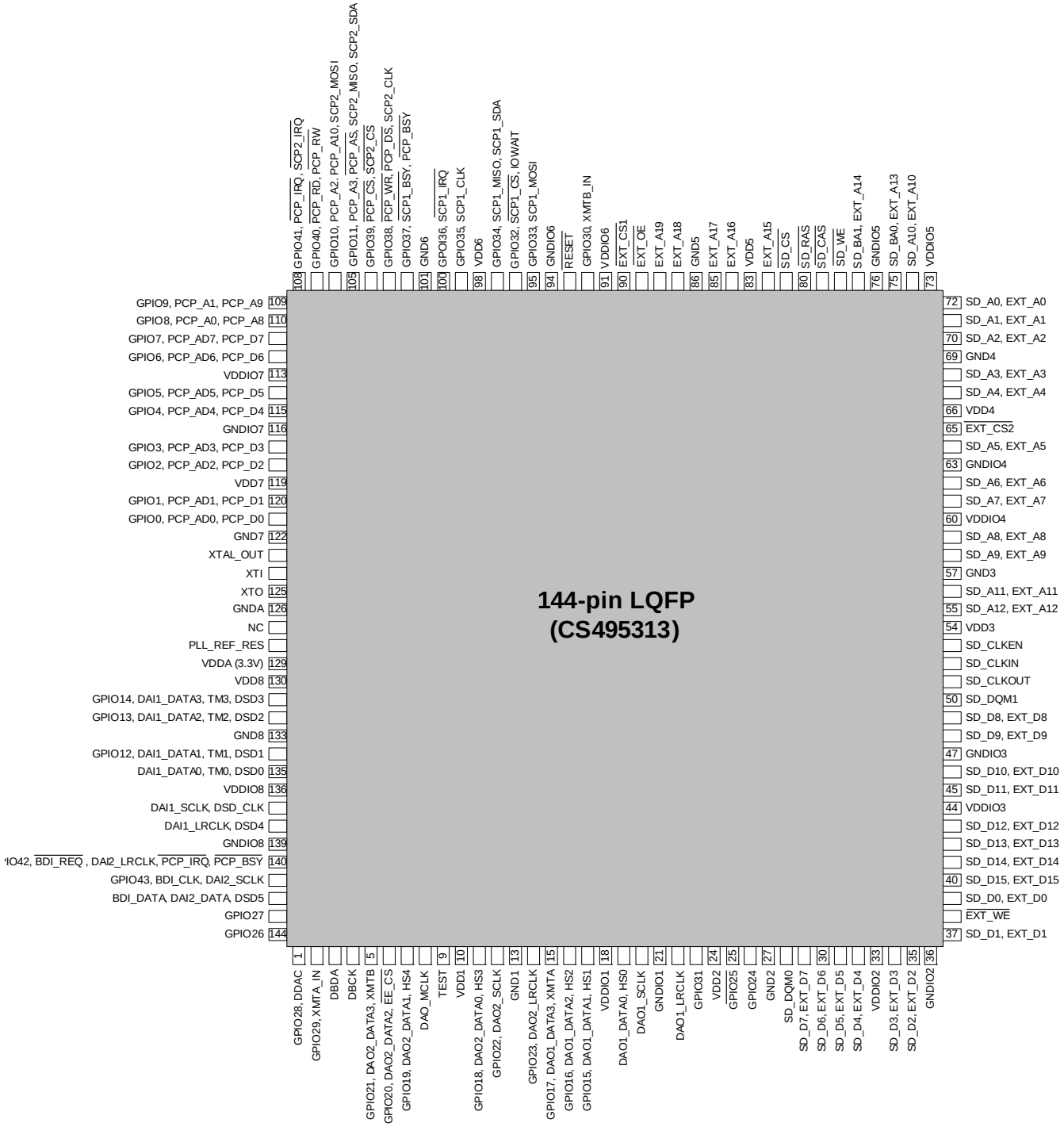

Figure 21. 144-pin LQFP Pin-Out Drawing (CS495313)

9 Package Mechanical Drawings

9.1 128-pin LQFP Package Drawing

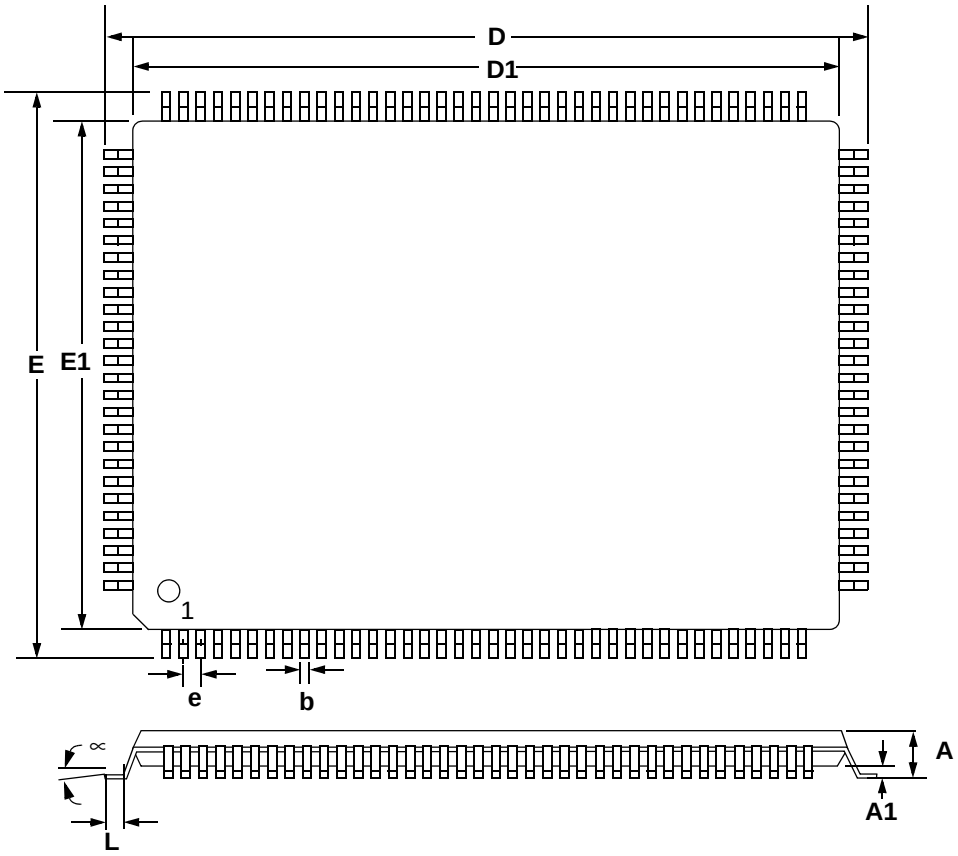

Figure 22. 128-pin LQFP Package Drawing

Table 7. 128-pin LQFP Package Characteristics

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.60	—	—	.063”
A1	0.05	—	0.15	.002”	—	.006”
b	0.17	0.22	0.27	.007”	.009”	.011”
D	22.00 BSC			.866”		
D1	20.00 BSC			.787”		
E	16.00 BSC			.630”		
E1	14.00 BSC			.551”		
e	0.50 BSC			.020”		
q	0°	3.5	7°	0°	3.5	7°
L	0.45	0.60	0.75	.018”	.024”	.030”
L1	1.00 REF			.039” REF		
TOLERANCES OF FORM AND POSITION						
ddd	0.08			.003”		

10 Revision History

Revision	Date	Changes
A1	February, 2006	Advance release.
A2	June, 2006	Updated part numbers for ordering (Tables 5 & 6), Updated V_{OH} and V_{OL} specification to include the current load used for testing
A3	July, 2006	Updated part numbers for ordering (Tables 5 & 6). Updated text in sections 3 and 4. Updated parameter descriptions in sections 5.1 and 5.3. Updated Tspickl, Tspickh, and Tspidov timing. Corrected Figure SPI Master Timing to use EE_CS. Added footnote to XTI table. Removed SCLK/LRCLK relative timing from DAI port timing. Removed SCLK/LRCLK slave relative timing from DAO port timing.
A4	October, 2007	Updated the Tspidsu, Tspickl, and Tspickh timing parameters for master mode SPI. This applies to both SPI ports.
PP1	May, 2008	Updated product feature list in Table 2. Updated Figure 19 and Figure 21.
PP2	June, 2008	Added typical crystal frequency values in Table Footnote 1 and minimum and maximum values of F_{xtal} in Section 5.8. Redefined Master mode clock speed for SCP_CLK in Section 5.11. Redefined DC leakage characterization data in Section 5.3, correcting units of measurement. Modified Footnote 1 under Section 5.10.
PP3	September, 2008	Removed references to External Parallel Flash / SRAM Interface.
PP4	June, 2009	Updated product number references in Section 5.9, Section 6, Section 7, Table 2,.Table 3, and Table 4. For all Active Low pins, changed Active Low pin designation from "#" character after the pin name to a line over the pin name as in "EE_CS". Removed Active Low designation from the BDI_REQ pin in the 128-pin pinout drawings in Figure 19 and Figure 20, and in the 144-pin pinout drawings in Figure 21 and Figure 22. Updated the pin names referred to in the timing diagrams in Figure 9, Figure 10, Figure 17, and Figure 18. Updated the parameters in Section 5.15.
PP5	July, 2009	Updated Figure 19, Figure 20, Figure 21. Removed CS495314-CQZ and CS495314-CQZR from Table 5 and Table 6. Added recommendation that CS4953x4 family be used with new designs. Updated Section 2
PP6	November, 2009	Removed references to UART port. Removed references to 11.2896, 18.432, and 27 MHz frequency clocks in Note 1 in Section 5.8 "Switching Characteristics — XTI" on page 12 and the minimum and maximum External Crystal Operating Frequency values in that same section. Updated Section 5.17 "Switching Characteristics — Digital Audio Output Port" on page 24. In Figure 21, "144-pin LQFP Pin-Out Drawing (CS495313)", on page 32, moved SCP2_SDA from Pin 106 to Pin 105, deleted duplicate EE_CS from Pin 25, and designated Pin 140 BDI_REQ as active low. Designated Pin 32, BDI_REQ as active low In Figure 19, "128-pin LQFP Pin-Out Drawing (CS495303/CS495313)", on page 30 and in Figure 20, "128-pin LQFP Pin-Out Drawing (CS495304/CS495314)", on page 31. In Section 5.3, the parameter, "Input leakage current (all digital pins with internal pull-up resistors enabled, and XTI)", Max value changes from 50 µA to 70 µA. In Section 5.13, the parameter SCP_CLK low to SCP_SDA out valid with symbol "tiicdov" maximum value changes from 18 ns to 36 ns.
PP7	June, 2010	Updated Table 5 to show status of various parts.

Contacting Cirrus Logic Support

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