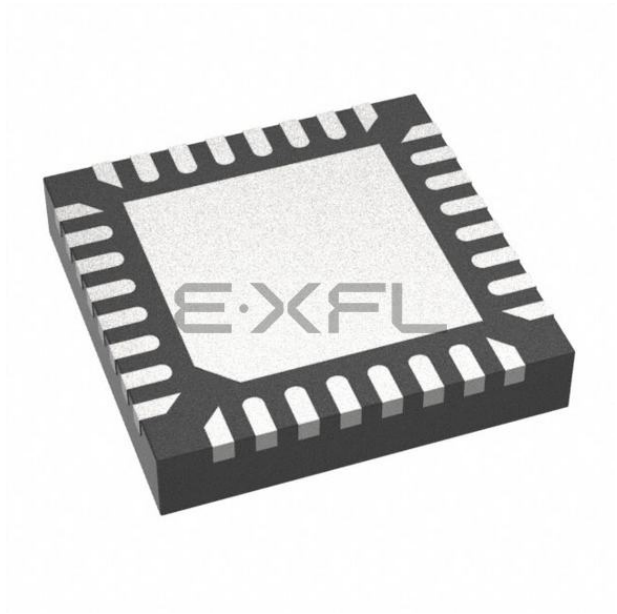

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini58tde

Table of Contents

List of Tables

1 GENERAL DESCRIPTION

The NuMicro® Mini58 series is pin-to-pin and function compatible with the NuMicro® Mini51 series, the 32-bit microcontroller (MCU) embedded with the ARM® Cortex®-M0 core. The Mini58 series can bridge the gap and replace the cost equivalent to traditional 8- and 16-bit microcontroller by 32-bit performance and rich functions. The Mini58 series supports a wide range of applications from low-end, price sensitive designs to computing-intensive ones and provides advanced high-end features in economical products.

The Mini58 series can run up to 50 MHz which is faster than 24 MHz in Mini51 series, and operate at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40℃ ~ +105℃. For the Mini58 series, the embedded program flash size upgrades from 16 Kbytes to 32 Kbytes and SRAM upgrades from 2 Kbytes to 4 Kbytes. The Mini58 series also offers size configurable Data Flash (shared with program flash), and 2.5 Kbytes flash for the ISP.

The Mini58 series has many high-performance peripheral functions, such as 22.1184 MHz internal RC oscillator (±1% accuracy), I/O port with up to 30 pins, four 32-bit timers, two UARTs with the RS485 function and IrDA function interface, one SPI interface, two I^2C interfaces, up to three 16-bit PWM generators providing six channels, an 8-channel 10-bit ADC, Watchdog Timer, Window Watchdog Timer, two Analog Comparators and a Brown-out Detector. All these peripherals have been incorporated into the Mini58 series to reduce component count, board space and system cost. Compared to the Mini51 series, the Mini58 series supports additional one UART and one I^2C interface for better and more flexible connectivity applications.

Additionally, the Mini58 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product. The Mini58 series also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

- Two I^2C devices
- Supports Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow for versatile rate control
- Supports multiple address recognition (four slave addresses with mask option)

- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 250 kSPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger or external pin trigger
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

4.2 NuMicro® Mini58 Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I^2C						
MINI58LDE	32 KB	4 KB	Configurable	2.5 KB	up to 30	2x32-bit	2	1	2	2	6	8x10-bit	v	v	LQFP48
MINI58ZDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(5x5)
MINI58TDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(4x4)
MINI58FDE	32 KB	4 KB	Configurable	2.5 KB	up to 17	2x32-bit	2	1	2	-	6	4x10-bit	v	v	TSSOP20

Table 4.2-1 NuMicro® Mini58 Series Product Selection Guide

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

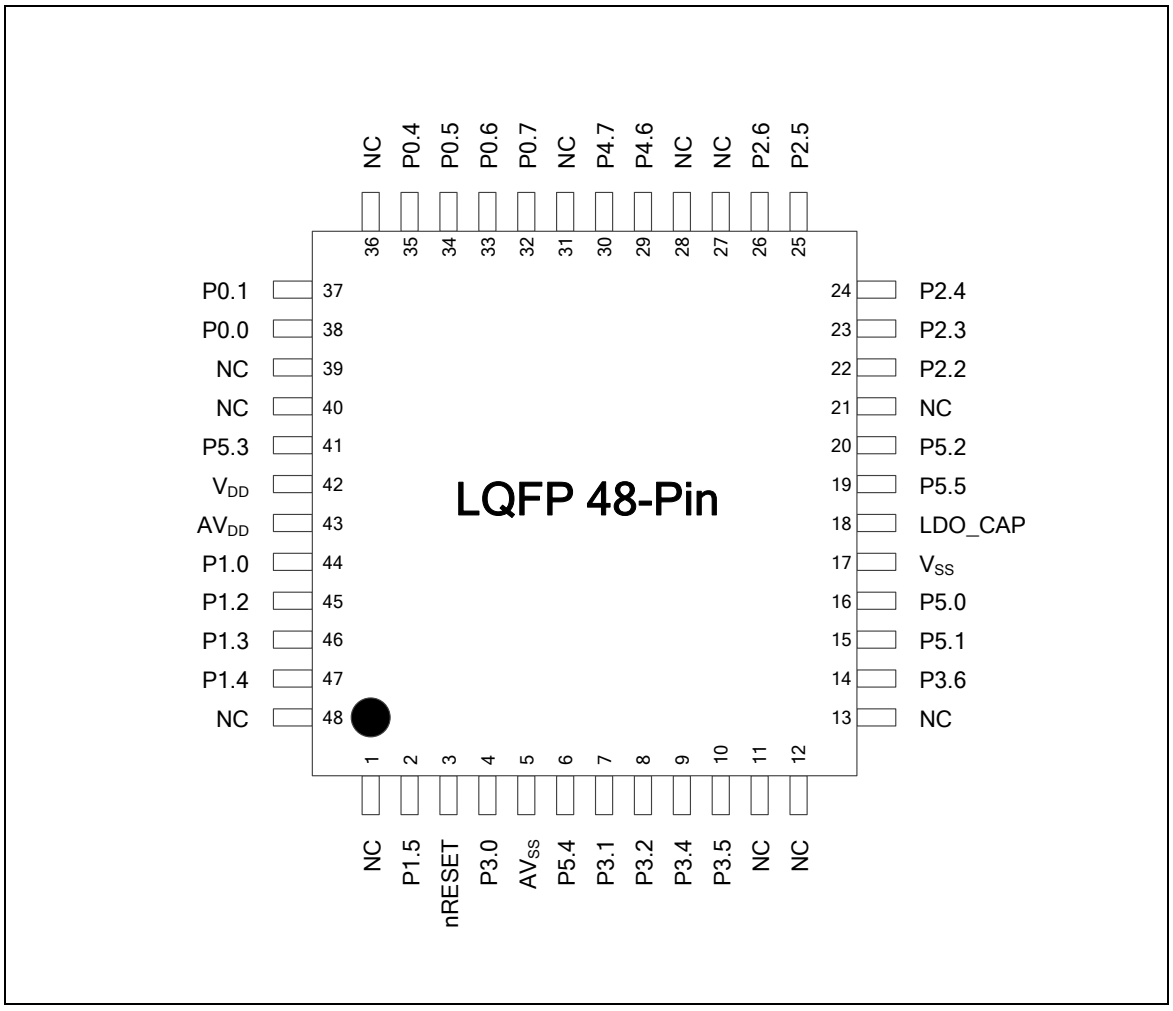


Figure 4.3-1 NuMicro® Mini58 Series LQFP 48-pin Diagram

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (SCS_AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])

(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG setting. User can set the CHIPRST (SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS (FMC_ISPCTL[1]) will not be reloaded from CONFIG setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ (SCS_AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD and GPIO
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table

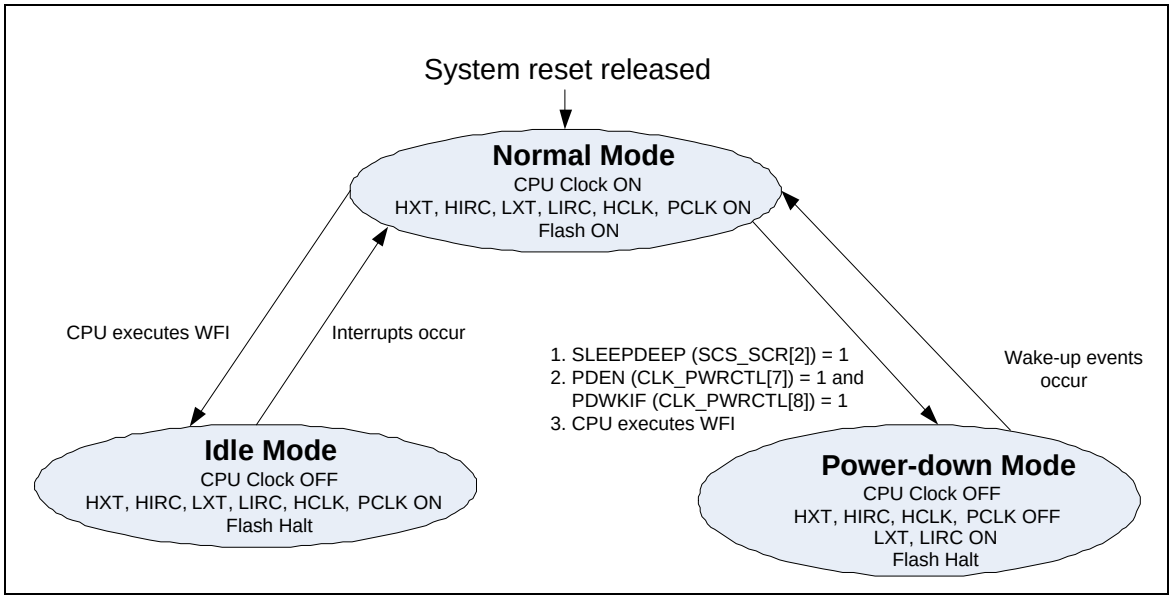


Figure 6.2-6 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in run mode.
2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in run mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.

	Normal Mode	Idle Mode	Power-down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (12/16 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
WWDT	ON	ON	Halt
UART	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, BOD and GPIO

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN (CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-up Source	Wake-up condition	System can enter Power-down mode again condition*

6.2.6.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Addressing Space	Token	Modules
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_7FFF	FLASH_BA	Flash Memory Space (32 KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4 KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO (P0~P5) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB Modules Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_00FF	WDT_BA	Watchdog Timer Control Registers
0x4000_4100 – 0x4000_47FF	WWDT_BA	Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI with Master/slave Function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
System Control Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Block Registers

Table 6.2-6 Address Space Assignments for On-Chip Modules

6.2.7 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer to count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-7 Exception Model

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
1 ~ 15	-	**-**	-	System exceptions	-
16	0	**BODOUT**	Brown-out	Brown-out low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM Brake interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	**-**	-	-	
28	12	**UART0_INT**	UART0	UART0 interrupt	Yes
29	13	**UART1_INT**	UART1	UART1 interrupt	Yes
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	**-**	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HIRC_TRIM_INT**	HIRC	HIRC trim interrupt	No
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt	Yes

Exception Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wake-Up
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt	No
36 ~ 40	20 ~ 24	**-**	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or Comparator 1 interrupt	Yes
42 ~ 43	26 ~ 27	**-**	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	**-**	-	-	

Table 6.2-8 System Interrupt Map Vector Table

6.2.8.4 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table based address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with the exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer Value
Exception Number * 0x04	Exception Entry Pointer using that Exception Number

Table 6.2-9 Vector Table Format

6.2.8.5 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.7 Enhanced PWM Generator

6.7.1 Overview

The NuMicro® Mini58 series has built in one PWM unit (PWM0) which is specially designed for motor driving control applications. The PWM0 supports six PWM generators which can be configured as six independent PWM outputs, PWM0_CH0~PWM0_CH5, or as three complementary PWM pairs, (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3) and (PWM0_CH4, PWM0_CH5) with three programmable dead-time generators.

Every complementary PWM pairs share one 8-bit prescaler. There are six clock dividers providing five divided frequencies (1, 1/2, 1/4, 1/8, 1/16) for each channel. Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The six PWM generators provide twelve independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched period and duty. Each PWM interrupt source with its corresponding enable bit can request PWM interrupt. The PWM generators can be configured as One-shot mode to produce only one PWM cycle signal or Auto-reload mode to output PWM waveform continuously.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the end of current period. The double buffering feature avoids glitch at PWM outputs.

Besides PWM, Motor controlling also need Timer, ACMP and ADC to work together. In order to control motor more precisely, we provide some registers that not only configure PWM but also Timer, ADC and ACMP, by doing so, it can save more CPU time and control motor with ease especially in BLDC.

6.7.2 Features

The PWM0 supports the following features:

- Six independent 16-bit PWM duty control units with maximum six port pins:
  - Six independent PWM outputs – PWM0_CH0, PWM0_CH1, PWM0_CH2, PWM0_CH3, PWM0_CH4, and PWM0_CH5
  - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion – (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3) and (PWM0_CH4, PWM0_CH5)
  - Three synchronous PWM pairs, with each pin in a pair in-phase – (PWM0_CH0, PWM0_CH1), (PWM0_CH2, PWM0_CH3) and (PWM0_CH4, PWM0_CH5)
- Group control bit – PWM0_CH2 and PWM0_CH4 are synchronized with PWM0_CH0, PWM0_CH3 and PWM0_CH5 are synchronized with PWM0_CH1
- One-shot (only support edge-aligned type) or Auto-reload mode PWM
- Up to 16-bit resolution
- Supports edge-aligned, center-aligned and precise center-aligned mode
- Supports asymmetric PWM generating in center-aligned and precise center-aligned mode
- Supports center loading in center-aligned and precise center-aligned mode
- Programmable dead-time insertion between complementary paired PWMs

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.8.2 Features

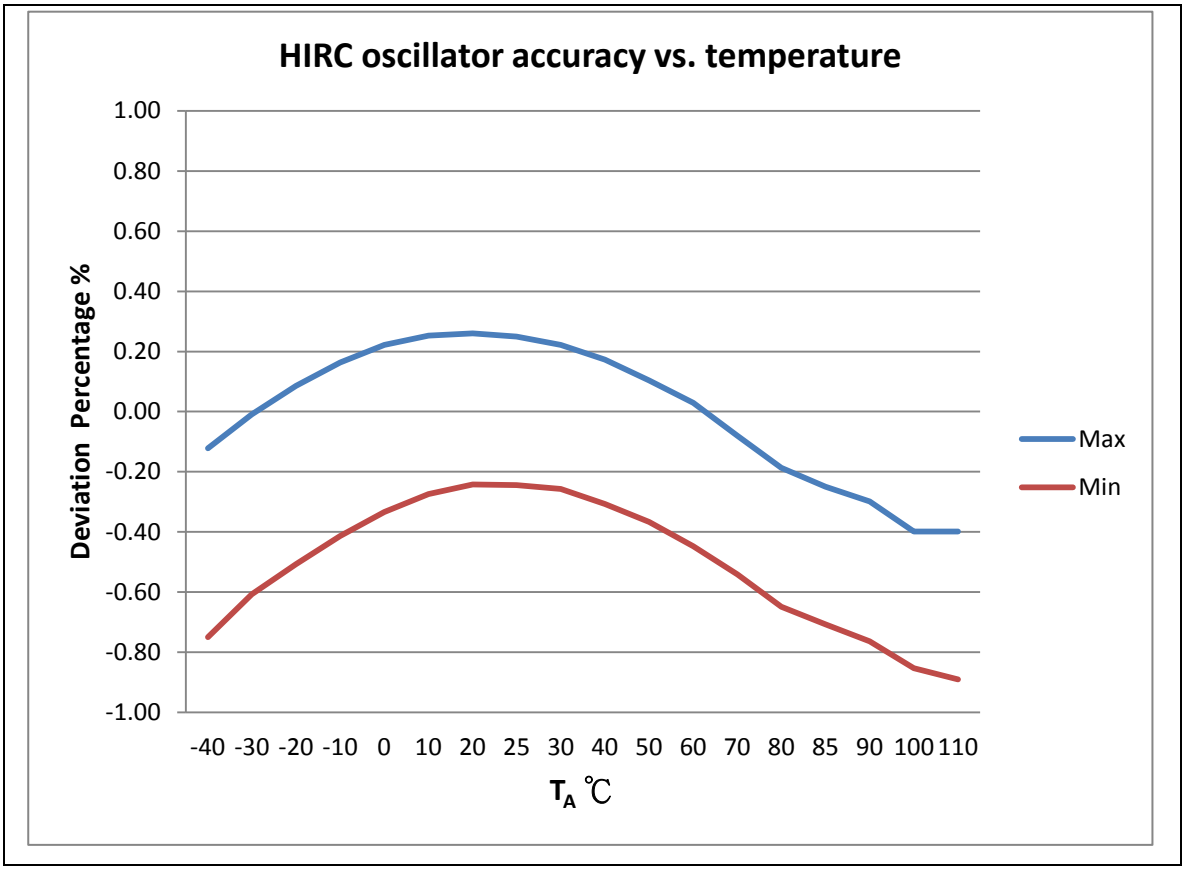
- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycles and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

I_{DD13}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	3.151	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	4 MHz	X	X	V
I_{DD14}		-	2.747	-	mA	5.5V	4 MHz	X	X	X
I_{DD15}		-	1.757	-	mA	3.3V	4 MHz	X	X	V
I_{DD16}		-	1.360	-	mA	3.3V	4 MHz	X	X	X
I_{DD17}	Operating Current Normal Run Mode HCLK = 32.768 kHz while(1){} Executed from Flash	-	176	-	µA	V_{DD}	LXT	HIRC	PLL	All Digital Modules
						5.5V	32.768 kHz	X	X	V
I_{DD18}		-	173	-	µA	5.5V	32.768 kHz	X	X	X
I_{DD19}		-	158	-	µA	3.3V	32.768 kHz	X	X	V
I_{DD20}		-	155	-	µA	3.3V	32.768 kHz	X	X	X
I_{DD21}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	168	-	µA	V_{DD}	HXT	LIRC	PLL	All Digital Modules
						5.5V	X	V	X	V[4]
I_{DD22}		-	167	-	µA	5.5V	X	V	X	X
I_{DD23}		-	150	-	µA	3.3V	X	V	X	V[4]
I_{DD24}		-	150	-	µA	3.3V	X	V	X	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 50MHz	-	12.386	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	24 MHz	X	V	V
I_{IDLE2}		-	7.346	-	mA	5.5V	24 MHz	X	V	X
I_{IDLE3}		-	10.784	-	mA	3.3V	24 MHz	X	V	V
I_{IDLE4}		-	5.838	-	mA	3.3V	24 MHz	X	V	X
I_{IDLE5}	Operating Current Idle Mode HCLK=22.1184 MHz	-	5.378	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	X	V	X	V
I_{IDLE6}		-	2.300	-	mA	5.5V	X	V	X	X
I_{IDLE7}		-	5.291	-	mA	3.3V	X	V	X	V

I_{TL}	Logic 1 to 0 Transition Current P0/1/2/3/4/5 (Quasi-bidirectional Mode) [*3]	-	-595	-750	μA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current P0/1/2/3/4/5	-1	-	+1	μA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P0/1/2/3/4/5 (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P0/1/2/3/4/5 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XTAL1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XTAL1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-0.3	-	0.2V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal nRESETPin Pull-up Resistor	40		150	kΩ	V_{DD} = 2.5 V ~ 5.5V
V_{ILS}	Negative-going Threshold (Schmitt input), P0/1/2/3/4/5	-0.3	-	0.3V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), P0/1/2/3/4/5	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-300	-400	-	μA	V_{DD} = 4.5 V, V_{SS} = 2.4 V
I_{SR12}		-50	-80	-	μA	V_{DD} = 2.7 V, V_{SS} = 2.2 V
I_{SR13}		-40	-73	-	μA	V_{DD} = 2.5 V, V_{SS} = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4/5 (Push-pull Mode)	-20	-26	-	mA	V_{DD} = 4.5 V, V_{SS} = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_{SS} = 2.2 V
I_{SR23}		-2.5	-5	-	mA	V_{DD} = 2.5 V, V_{SS} = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4/5 (Quasi-bidirectional, Open-Drain and Push-pull Mode)	10	15	-	mA	V_{DD} = 4.5 V, V_{SS} = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_{SS} = 0.45 V
I_{SK13}		5	8	-	mA	V_{DD} = 2.5 V, V_{SS} = 0.45 V

Notes:

1. nRESET pin is a Schmitt trigger input.



8.3.6 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-10	-	+10	%	V_{DD}=2.5V~ 5.5V T_A = 25℃
		-40	-	+40	%	V_{DD}=2.5V~ 5.5V T_A = -40℃~+105℃

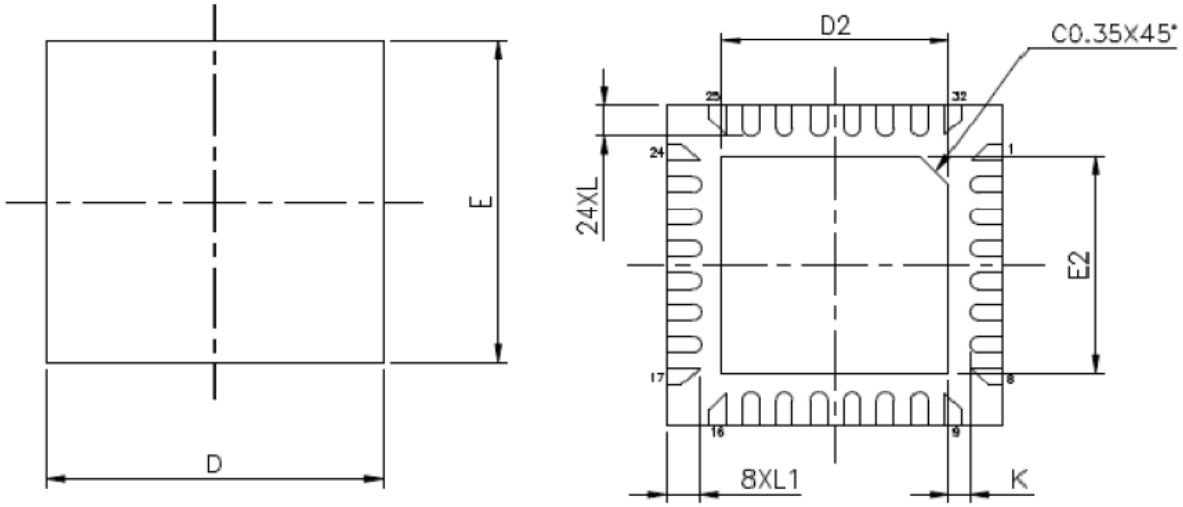
8.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Page Erase Time	-	20	-	ms	
T_{PROG}	Program Time	-	40	-	us	
I_{DD1}	Read Current	-	7	-	mA	
I_{DD2}	Program Current	-	8	-	mA	
I_{DD3}	Erase Current	-	12	-	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

9.2 33-pin QFN (4 mm x 4 mm)



	Symbol	Min	Nom	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0.0	0.02	0.05
L/F Thickness	A3		0.2 REF.	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4.00 BSC	
	E		4.00 BSC	
Lead Pitch	e		0.40 BSC	
Lead Length	L	0.35	0.4	0.45
	K	0.2	--	--

Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.75
E2		2.6	2.7	2.75