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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/mini58zde

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4.2 NuMicro® Mini58 Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I^2C						
MINI58LDE	32 KB	4 KB	Configurable	2.5 KB	up to 30	2x32-bit	2	1	2	2	6	8x10-bit	v	v	LQFP48
MINI58ZDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(5x5)
MINI58TDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(4x4)
MINI58FDE	32 KB	4 KB	Configurable	2.5 KB	up to 17	2x32-bit	2	1	2	-	6	4x10-bit	v	v	TSSOP20

Table 4.2-1 NuMicro® Mini58 Series Product Selection Guide

4.3 PIN CONFIGURATION

4.3.1 LQFP 48-pin

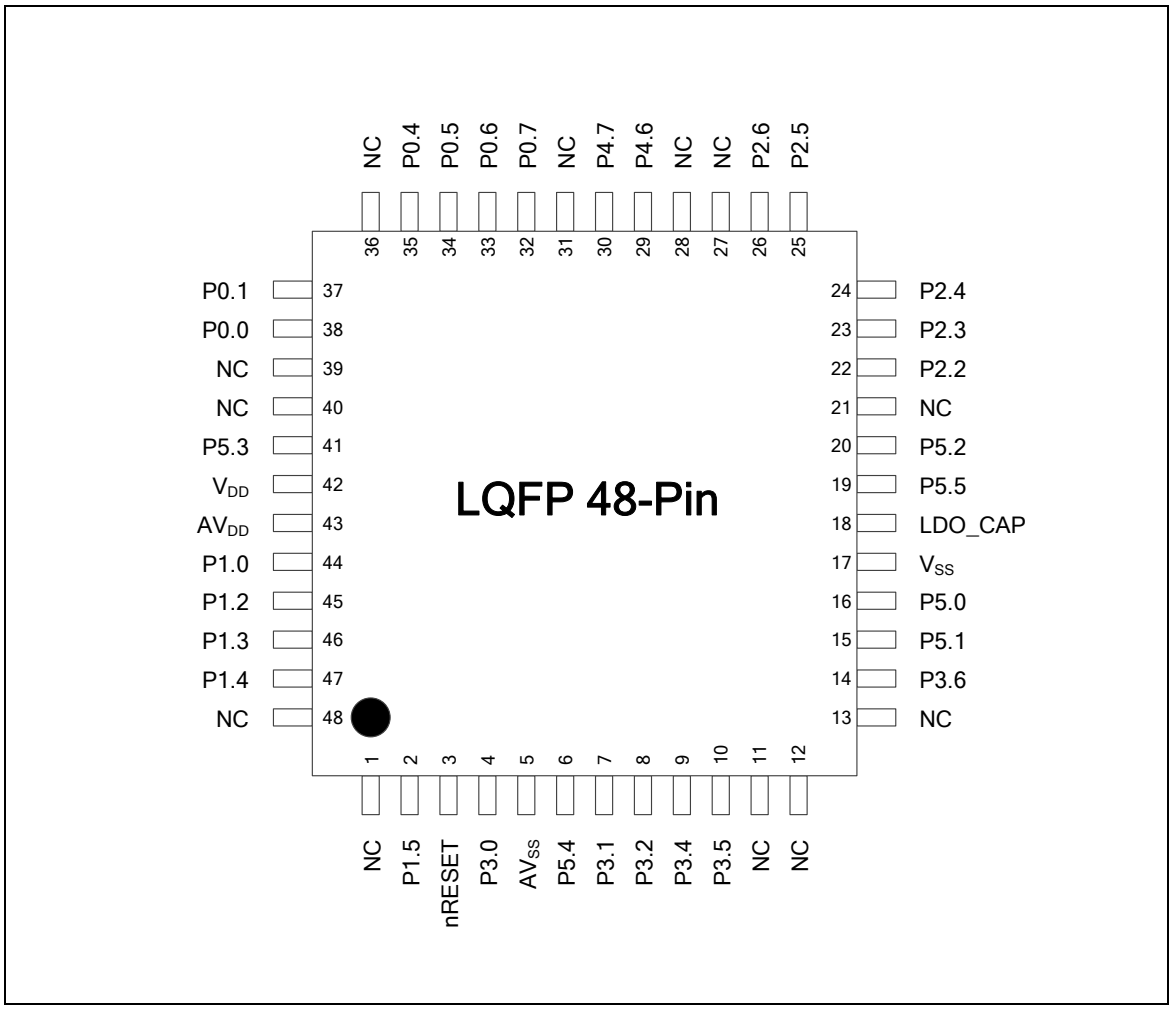


Figure 4.3-1 NuMicro® Mini58 Series LQFP 48-pin Diagram

4.4 Pin Description

Pin Number			Pin Name	Pin Type	Description
LQFP 48-pin	QFN 33-pin	TSSOP 20-pin			
1	---	---	NC	**---**	Not connected
2	1	4	P1.5	**I/O**	General purpose digital I/O pin
			ADC_CH5	**AI**	ADC analog input pin
			UART1_TXD	**O**	UART1 transmitter output pin
			ACMP0_P0	**AI**	Analog comparator positive input pin
3	2	5	nRESET	**I(ST)**	The Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	---	P3.0	**I/O**	General purpose digital I/O pin
			ADC_CH6	**AI**	ADC analog input pin
			ACMP1_N	**AI**	Analog comparator negative input pin
5	---	---	AV_{SS}	**AP**	Ground pin for analog circuit
6	4	---	P5.4	**I/O**	General purpose digital I/O pin
7	5	---	P3.1	**I/O**	General purpose digital I/O pin
			ADC_CH7	**AI**	ADC analog input pin
			ACMP1_P0	**AI**	Analog comparator positive input pin
8	6	6	P3.2	**I/O**	General purpose digital I/O pin
			INT0	**I**	External interrupt 0 input pin
			STADC	**I**	ADC external trigger input pin
			TM0_EXT	**I/O**	Timer 0 external capture / reset trigger input pin / toggle output pin
			ACMP1_P1	**AI**	Analog comparator positive input pin (not support in TSSOP20 package)
9	7	7	P3.4	**I/O**	General purpose digital I/O pin
			TM0_CNT_OUT	**I/O**	Timer 0 external event counter input pin / toggle output pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			ACMP1_P2	**AI**	Analog comparator positive input pin
10	8	8	P3.5	**I/O**	General purpose digital I/O pin
			TM1_CNT_OUT	**I/O**	Timer 1 external event counter input pin / toggle output pin
			I2C0_SCL	**I/O**	I^2C0 clock I/O pin
			ACMP1_P3	**AI**	Analog comparator positive input pin
11	---	---	NC	**---**	Not connected

- NVIC
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Idle mode
- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG setting. User can set the CHIPRST (SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS (FMC_ISPCTL[1]) will not be reloaded from CONFIG setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ (SCS_AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD and GPIO
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table

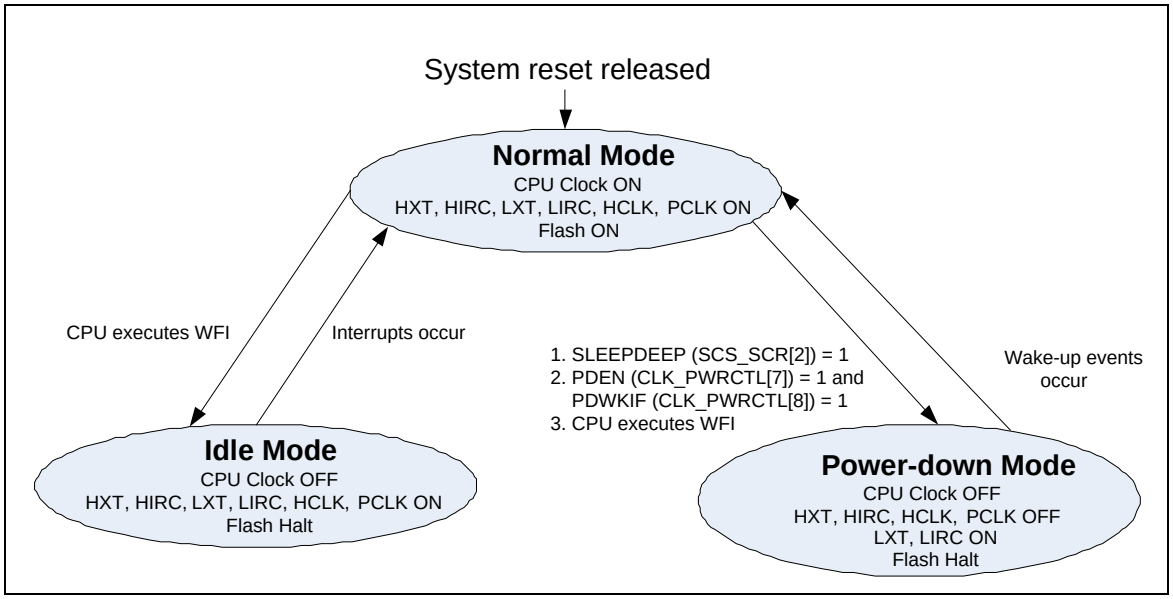


Figure 6.2-6 Power Mode State Machine

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PDEN (CLK_PWRCTL[7]) bit is set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 3 sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT) or 32.768 kHz (LXT) external low speed crystal oscillator
- Programmable PLL output clock frequency (PLL source can be selected from external 4 ~ 24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)) (PLL FOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

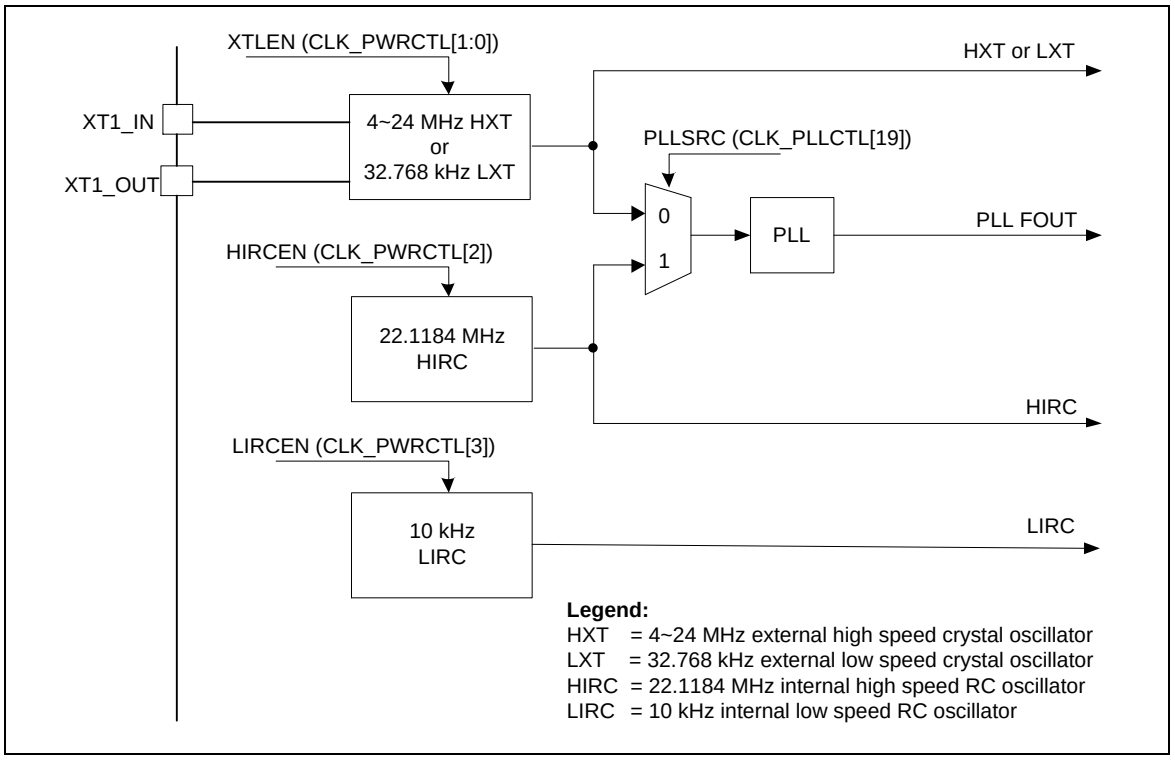


Figure 6.3-1 Clock Generator Block Diagram

	Peripheral Clok Selectable	Ext. CLK (HXT Or LXT)	HIRC	LIRC	HCLK	PLL
WDT	Yes	Yes	No	Yes	Yes	No
WWDT	Yes	Yes	No	Yes	Yes	No
Timer0	Yes	Yes	Yes	Yes	Yes	No
Timer1	Yes	Yes	Yes	Yes	Yes	No
I^2C0	No	-	-	-	-	-
I^2C1	No	-	-	-	-	-
SPI	Yes	Yes	No	No	Yes	Yes
UART0	Yes	Yes	Yes	No	No	Yes
UART1	Yes	Yes	Yes	No	No	Yes
PWM	No	-	-	-	-	-
ADC	Yes	Yes	Yes	No	Yes	Yes
ACMP	No	-	-	-	-	-

Table 6.3-1 Peripheral Clock Source Selection Table

Note: For the peripherals those peripheral clock are not selectable, its clock source is fixed to PCLK.

6.3.5 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripheral clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator (LIRC) clock
- 32.768 kHz external low speed crystal oscillator (LXT) clock (If PDLXT = 1 and XTLEN[1:0] = 10)
- Peripherals Clock (When 10 kHz low speed oscillator is adopted as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

6.3.6 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CLKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

- Each pin of PWM0_CH0 to PWM0_CH5 has independent polarity setting control
- Hardware fault brake protections
  - Supports software trigger
  - Two Interrupt source types:
    - Synchronously requested at PWM frequency when down counter comparison matched (edge- and center-aligned type) or underflow (edge-aligned type)
    - Requested when external fault brake asserted
      - BKP0: EINT0 or CPO1
      - BKP1: EINT1 or CPO0
- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register
- Supports mask aligned function
- Supports independently rising CMP matching, PERIOD matching, falling CMP matching (in Center-aligned type), period matching to trigger ADC conversion
- Timer comparing matching event trigger PWM to do phase change in BLDC application
- Supports ACMP output event trigger PWM to force PWM output at most one period low, this feature is usually for step motor control
- Provides interrupt accumulation function

6.10 UART Controller (UART)

6.10.1 Overview

The NuMicro® Mini58 series provides two channels of Universal Asynchronous Receiver/Transmitters (UART). The UART0 performs supports flow control function. The UART0 performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART0 controller also supports IrDA SIR Function, and RS-485 function mode. The UART0 channel supports six types of interrupts. The UART1 channel supports five types of interrupts. The UART1 only performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART0 has 16 bytes Receiver/Transmitter FIFO. The UART1 only has one Receiver/Transmitter buffer.

6.10.2 Features

- Full duplex, asynchronous communications
- Separates receive/transmit 16/16 bytes entry FIFO for data payloads (Only Available in UART0)
- Separates receive/transmit 1/1 byte buffer for data payloads (Only Available in UART1)
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (Only Available in UART0)
- Programmable receiver buffer trigger level (Only Available in UART0)
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (Only Available in UART0)
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UART_TOUT[15:8] register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode (Only Available in UART0)
  - Supports 3/16-bit duration for normal mode
- Supports RS-485 function mode (Only Available in UART0)
  - Supports RS-485 9-bit mode
  - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

6.13 Analog-to-Digital Converter (ADC)

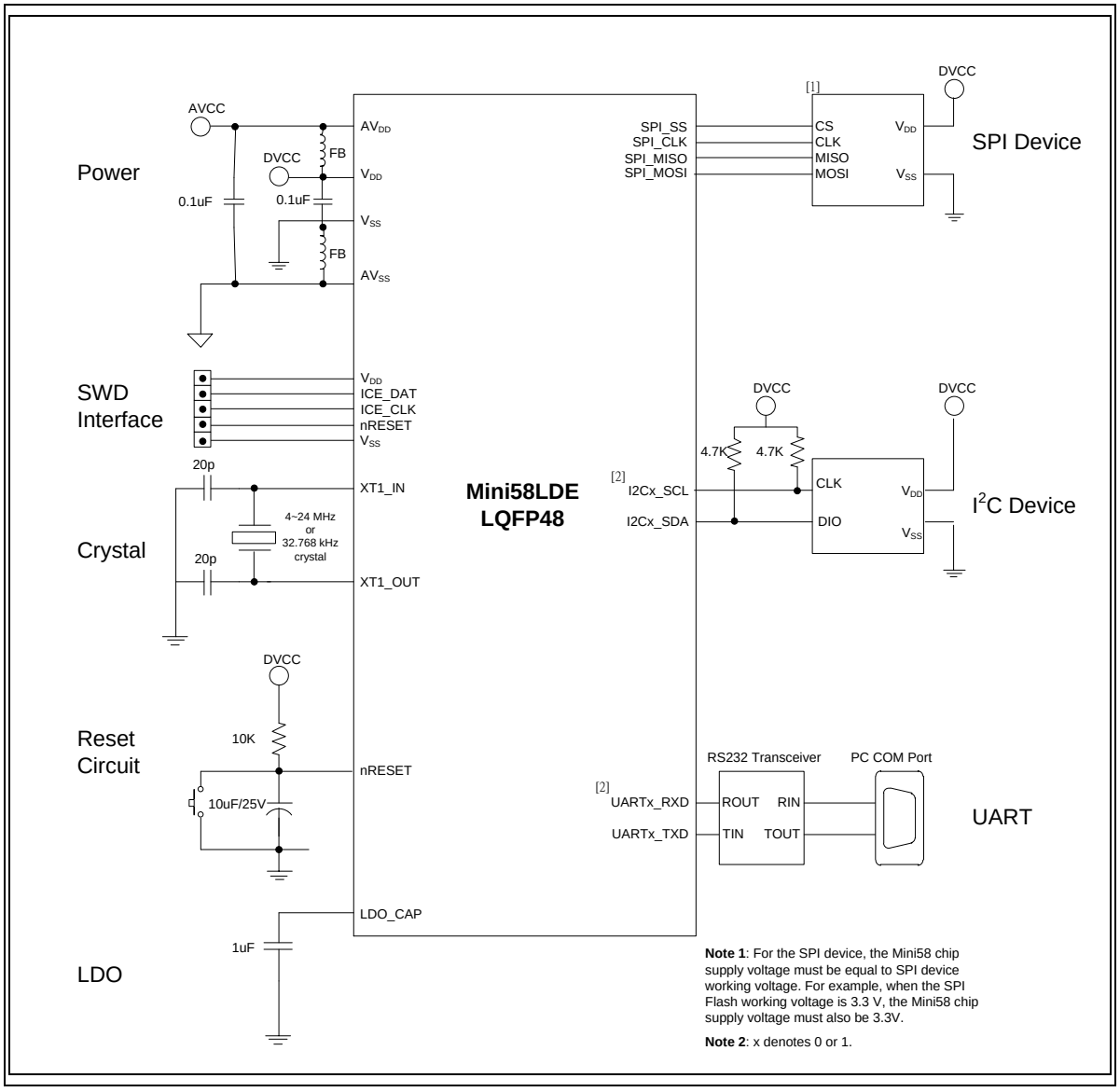
6.13.1 Overview

The Mini58 series contains one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with eight input channels. The A/D converters can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.13.2 Features

- Analog input voltage range: 0 ~ Analog Supply Voltage from AV_{DD}
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to eight single-end analog input channels
- Maximum ADC clock frequency is 6 MHz, and 14 ADC clocks per sample
- Two operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - PWM sequence mode: When PWM trigger, two of three ADC channels from 0 to 2 will automatically convert analog data in the sequence of channel [0,1] or channel[1,2] or channel[0,2] defined by MODESEL (ADC_SEQCTL[3:2])
- An A/D conversion can be started by:
  - Software write 1 to SWTRG bit
  - External pin STADC
  - PWM trigger with optional start delay period
- Each Conversion result is held in data register with valid and overrun indicators
- Conversion results can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: External analog voltage and internal fixed band-gap voltage

7 APPLICATION CIRCUIT



I_{IDLE8}		-	2.265	-	mA	3.3V	X	V	X	X
I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	4.577	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE10}		-	3.364	-	mA	5.5V	V	X	X	X
I_{IDLE11}		-	3.062	-	mA	3.3V	V	X	X	V
I_{IDLE12}		-	1.871	-	mA	3.3V	V	X	X	X
I_{IDLE13}	Operating Current Idle Mode HCLK = 4 MHz	-	2.838	-	mA	V_{DD}	HXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE14}		-	2.433	-	mA	5.5V	V	X	X	X
I_{IDLE15}		-	1.446	-	mA	3.3V	V	X	X	V
I_{IDLE16}		-	1.048	-	mA	3.3V	V	X	X	X
I_{IDLE17}	Operating Current Idle Mode HCLK = 32.768 kHz	-	167	-	µA	V_{DD}	LXT	HIRC	PLL	All Digital Modules
						5.5V	V	X	X	V
I_{IDLE18}		-	166	-	µA	5.5V	V	X	X	X
I_{IDLE19}		-	150	-	µA	3.3V	V	X	X	V
I_{IDLE20}		-	149	-	µA	3.3V	V	X	X	X
$I_{IDLE\ 21}$	Operating Current Idle Mode HCLK = 10 kHz	-	167	-	µA	V_{DD}	HXT	LIRC	PLL	All Digital Modules
						5.5V	X	V	X	V[4]
$I_{IDLE\ 22}$		-	166	-	µA	5.5V	X	V	X	X
$I_{IDLE\ 23}$		-	150	-	µA	3.3V	X	V	X	V[4]
$I_{IDLE\ 24}$		-	149	-	µA	3.3V	X	V	X	X
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)	-	6.2	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.				
I_{PWD2}		-	5.8	-	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.				
I_{IL}	Logic 0 Input Current P0/1/2/3/4/5 (Quasi-bidirectional Mode)	-	-70	-75	µA	V_{DD} = 5.5 V, V_{IN} = 0V				

2. XTAL1 is a CMOS input.

3. Pins of P0, P1, P2, P3, P4 and P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{IN} approximates to 2V.

4. Only enable modules which support 10 kHz LIRC clock source

4 MHz ~ 24 MHz	20 pF	20 pF
32.768 kHz	20 pF	20 pF

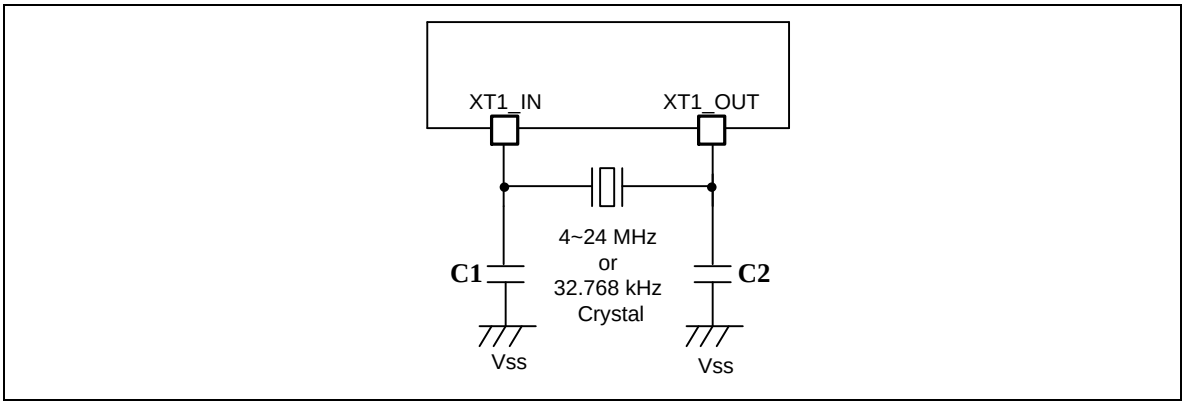


Figure 8.3-1 Mini58 Typical Crystal Application Circuit

8.3.5 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC}	Operating Current	-	700	-	μA	T_A = 25 ℃,V_{DD} = 5 V

I_{LVR}	Quiescent Current	-	1	5	μA	AV_{DD} =5.5V
V_{LVR}	Threshold Voltage	1.90	2.00	2.10	V	T_A=25℃
		1.70	1.90	2.05	V	T_A=-40℃
		2.00	2.20	2.45	V	T_A =105℃

8.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	-	140	μA	AV_{DD} =5.5V
V_{BOD}	Brown-out Detector (Falling edge)	4.2	4.38	4.55	V	BODEN = 1, BOD_VL [1:0]=11
		3.5	3.68	3.85	V	BODEN = 1, BOD_VL [1:0]=10
		2.5	2.68	2.85	V	BODEN = 1, BOD_VL [1:0]=01
		2.0	2.18	2.35	V	BODEN = 1, BOD_VL [1:0]=00
V_{BOD}	Brown-out Detector (Rising edge)	4.3	4.52	4.75	V	BODEN = 1, BOD_VL [1:0]=11
		3.5	3.8	4.05	V	BODEN = 1, BOD_VL [1:0]=10
		2.5	2.77	3.05	V	BODEN = 1, BOD_VL [1:0]=01
		2.0	2.25	2.55	V	BODEN = 1, BOD_VL [1:0]=00

8.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage	1.6	2	2.4	V	-
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	0.5	-	-	ms	

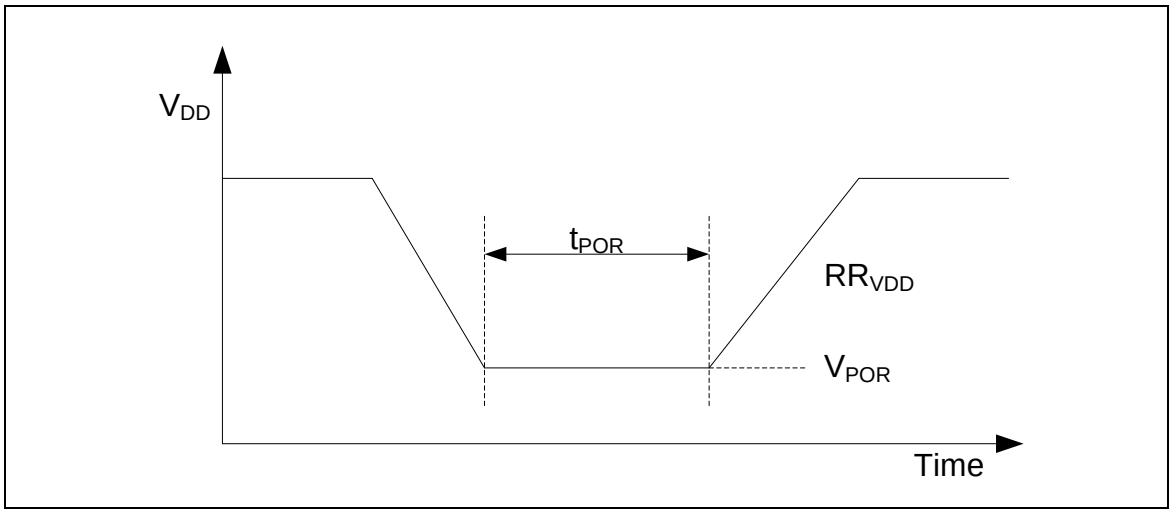
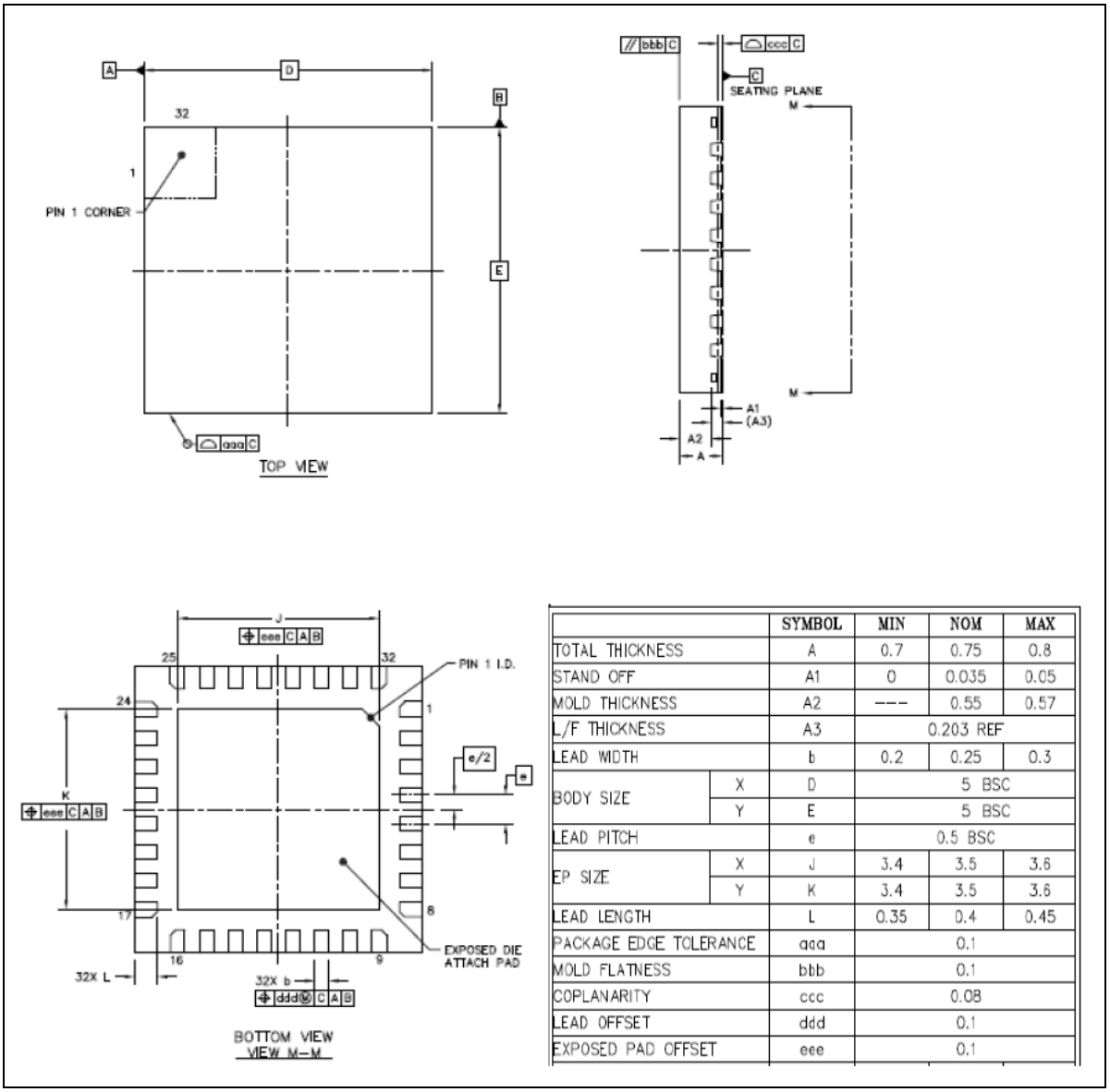


Figure 8.4-1 Power-up Ramp Condition

8.4.6 Comparator

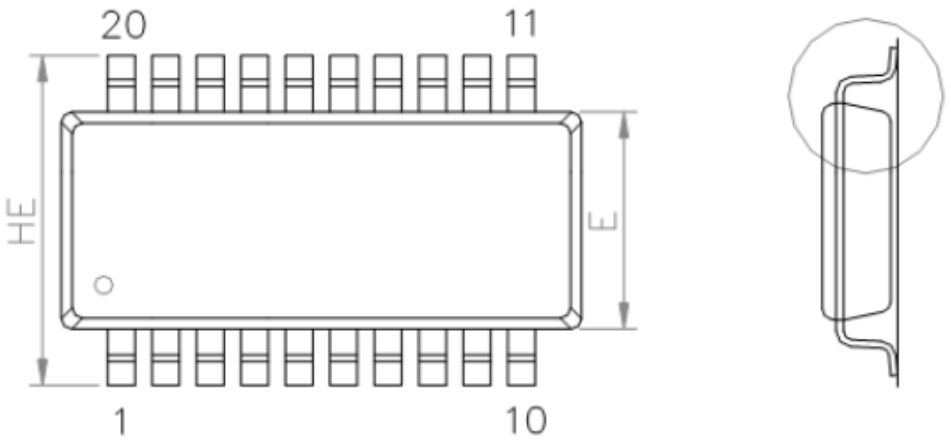
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	40	80	μA	AV_{DD}=5V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} – 0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{COM}=1.2 V, V_{DIFF}=0.1 V
V_{HYS}	Hysteresis	-	±30	±60	mV	V_{COM}=1.2 V
T_{STB}	Stable time	-	-	1	μs	

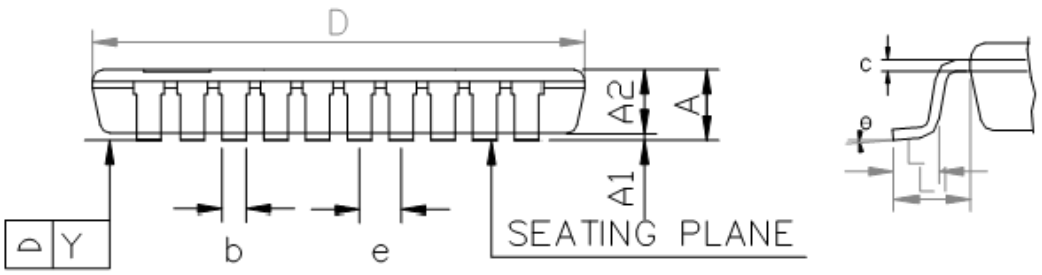
9.3 33-pin QFN (5 mm x 5 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

9.4 20-pin TSSOP





SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		