Infineon Technologies - SAF-XC164LM-16F20F BA Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164lm-16f20f-ba

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Table of Contents

1 Summary of Features

For a quick overview or reference, the XC164LM's properties are listed here in a condensed way.

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 × 16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with up to 63 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 0/2/4 Kbytes[1)] On-Chip Data SRAM (DSRAM)
  - 2 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 32/64/128[1)] Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 16-Channel General Purpose Capture/Compare Unit (CAPCOM2)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip Real Time Clock, Driven by the Main Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 47 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader

1) Depends on the respective derivative. See **Table 1 "XC164LM Derivative Synopsis" on Page 6**.

- On-Chip Debug Support via JTAG Interface
- 64-Pin Green LQFP Package for the -16F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)
- 64-Pin TQFP Package for the -4F/8F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164LM please refer to your responsible sales representative or your local distributor.

This document describes several derivatives of the XC164LM group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164LM** throughout this document.

Table 1 XC164LM Derivative Synopsis

Derivative[1)]	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAF-XC164LM-16F40F SAF-XC164LM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1
SAF-XC164LM-8F40F SAF-XC164LM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1,
SAF-XC164LM-4F40F SAF-XC164LM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1

1) This Data Sheet is valid for:
devices starting with and including design step BA for the -16F derivatives, and for
devices starting with and including design step AA for -4F/8F derivatives.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
Port 3	28-39, 42	IO	Port 3 is a 13-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special).The following Port 3 pins also serve for alternate functions:
P3.1	28	O	T6OUT: [GPT2] Timer T6 Toggle Latch Output,
		I/O	RxD1: [ASC1] Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN: [Fast External Interrupt 1] Input (alternate pin A),
		I	TCK: [Debug System] JTAG Clock Input
P3.2	29	I	CAPIN: [GPT2] Register CAPREL Capture Input,
		I	TDI: [Debug System] JTAG Data In
P3.3	30	O	T3OUT: [GPT1] Timer T3 Toggle Latch Output,
		O	TDO: [Debug System] JTAG Data Out
P3.4	31	I	T3EUD: [GPT1] Timer T3 External Up/Down Control Input,
		I	TMS: [Debug System] JTAG Test Mode Selection
P3.5	32	I	T4IN: [GPT1] Timer T4 Count/Gate/Reload/Capture Inp.
		O	TxD1: [ASC0] Clock/Data Output (Async./Sync.),
		O	BRKOUT: [Debug System] Break Out
P3.6	33	I	T3IN: [GPT1] Timer T3 Count/Gate Input
P3.7	34	I	T2IN: [GPT1] Timer T2 Count/Gate/Reload/Capture Inp.
		I	BRKIN: [Debug System] Break In
P3.8	35	I/O	MRST0: [SSC0] Master-Receive/Slave-Transmit In/Out.
P3.9	36	I/O	MTSR0: [SSC0] Master-Transmit/Slave-Receive Out/In.
P3.10	37	O	TxD0: [ASC0] Clock/Data Output (Async./Sync.),
		I	EX2IN: [Fast External Interrupt 2] Input (alternate pin B)
P3.11	38	I/O	RxD0: [ASC0] Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN: [Fast External Interrupt 2] Input (alternate pin A)
P3.13	39	I/O	SCLK0: [SSC0] Master Clock Output / Slave Clock Input.,
		I	EX3IN: [Fast External Interrupt 3] Input (alternate pin A)
P3.15	42	O	CLKOUT: System Clock Output (= CPU Clock),
		O	FOUT: Programmable Frequency Output

3 Functional Description

The architecture of the XC164LM combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources (see **Figure 3**).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164LM.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164LM.

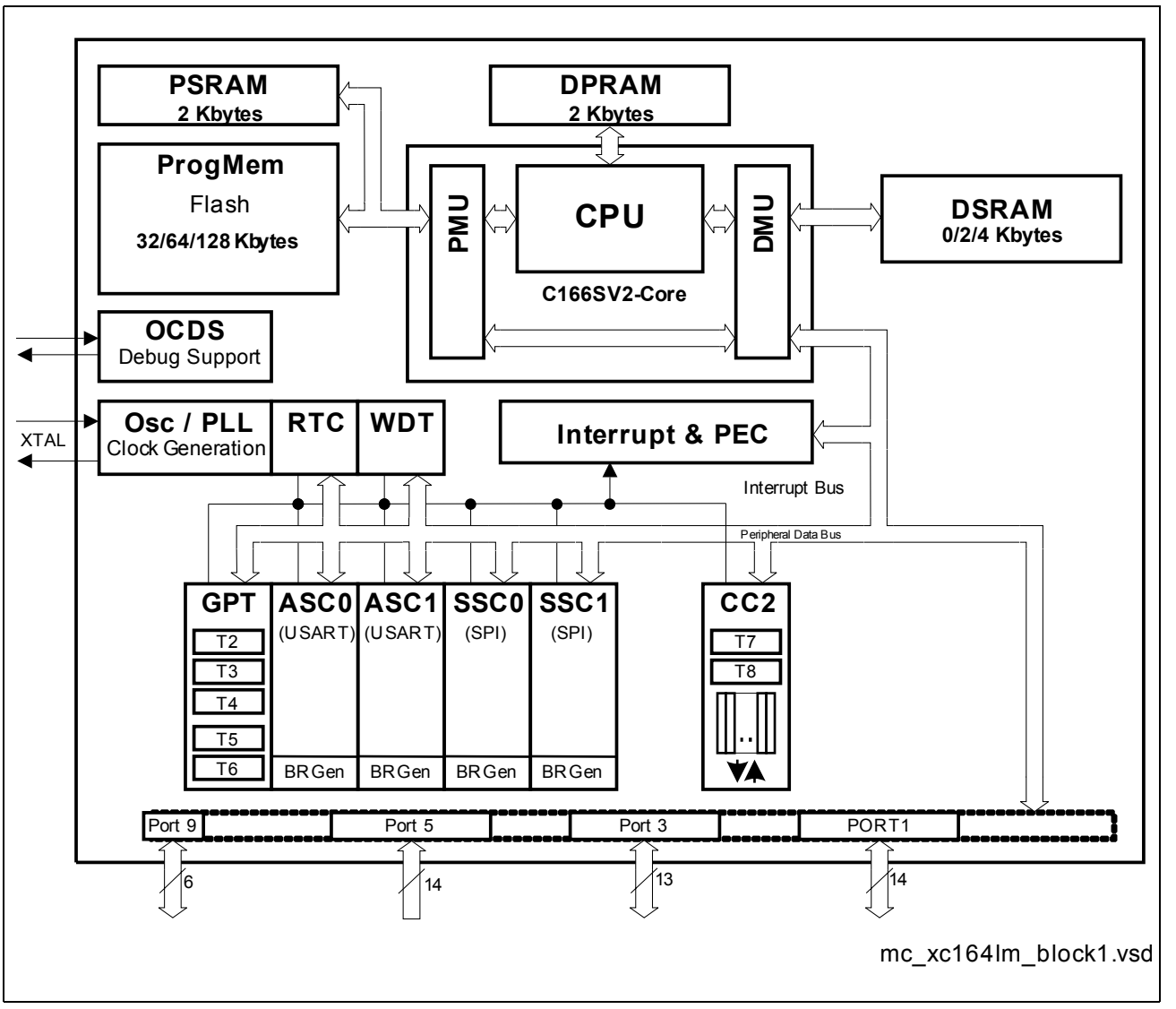

Figure 3 Block Diagram

example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a 32-/16-bit division is started within 4 cycles, while the remaining 15 cycles are executed in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164LM instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Table 4 XC164LM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
Unassigned node	–	xx'0080$_H$	20$_H$ / 32$_D$
Unassigned node	–	xx'0084$_H$	21$_H$ / 33$_D$
Unassigned node	–	xx'00A0$_H$	28$_H$ / 40$_D$
Unassigned node	–	xx'00A4$_H$	29$_H$ / 41$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	–	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'0134$_H$	4D$_H$ / 77$_D$
Unassigned node	–	xx'0138$_H$	4E$_H$ / 78$_D$
Unassigned node	–	xx'013C$_H$	4F$_H$ / 79$_D$
Unassigned node	–	xx'0140$_H$	50$_H$ / 80$_D$
Unassigned node	–	xx'0150$_H$	54$_H$ / 84$_D$
Unassigned node	–	xx'0154$_H$	55$_H$ / 85$_D$
Unassigned node	–	xx'0158$_H$	56$_H$ / 86$_D$
Unassigned node	–	xx'015C$_H$	57$_H$ / 87$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$
Unassigned node	–	xx'0164$_H$	59$_H$ / 89$_D$
Unassigned node	–	xx'0168$_H$	5A$_H$ / 90$_D$
Unassigned node	–	xx'016C$_H$	5B$_H$ / 91$_D$
Unassigned node	–	xx'0170$_H$	5C$_H$ / 92$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

The XC164LM also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	xx’0000$_H$	00$_H$	III
• Software Reset		RESET	xx’0000$_H$	00$_H$	III
• W-dog Timer Overflow		RESET	xx’0000$_H$	00$_H$	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	xx’0008$_H$	02$_H$	II
• Stack Overflow	STKOF	STOTRAP	xx’0010$_H$	04$_H$	II
• Stack Underflow	STKUF	STUTRAP	xx’0018$_H$	06$_H$	II
• Software Break	SOFTBRK	SBRKTRAP	xx’0020$_H$	08$_H$	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	xx’0028$_H$	0A$_H$	I
• PMI Access Error	PACER	BTRAP	xx’0028$_H$	0A$_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx’0028$_H$	0A$_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx’0028$_H$	0A$_H$	I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps • TRAP Instruction	–	–	Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

3.5 Capture/Compare Unit (CAPCOM2)

The CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, an external count input for CAPCOM timer T7 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer (T7 or T8, respectively), and programmed for capture or compare function.
10 registers of the CAPCOM2 module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare

register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

3.6 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

3.10 Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can be disabled until the EINIT instruction has been executed (compatible mode), or it can be disabled and enabled at any time by executing instructions DISWDT and ENWDT (enhanced mode). Thus, the chip's start-up procedure is always monitored. The software has to be designed to restart the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/4/128/256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded and the low byte is cleared. Thus, time intervals between 13 µs and 419 ms can be monitored (@ 40 MHz).
The default Watchdog Timer interval after reset is 3.28 ms (@ 40 MHz).

3.12 Parallel Ports

The XC164LM provides up to 47 I/O lines which are organized into three input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

Table 7 Summary of the XC164LM's Parallel Ports

Port	Control	Alternate Functions
PORT1	Pad drivers	Capture inputs or compare outputs, Serial interface lines
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, System clock output CLKOUT (or FOUT)
Port 5	–	Timer control signals
Port 9	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs

3.13 Power Management

The XC164LM provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC164LM into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC164LM's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittent operation of the XC164LM by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

4 Electrical Parameters

The operating range for the XC164LM is defined by its electrical parameters. For proper operation the indicated limitations must be respected when designing a system.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	1)
Junction temperature	T_J	-40	150	°C	Under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDI}	-0.5	3.25	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDP}	-0.5	6.2	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DDP} + 0.5	V	2)
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–

1) Moisture Sensitivity Level (MSL) 3, conforming to Jedec J-STD-020C for 260 °C.

2) Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for VDDI.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164LM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ 1)
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode 2)3)
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	$V_{DDP} - V_{DDI}$ 4)
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin 5)6)
Overload current coupling factor for digital I/O pins 7)	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$	–	50	mA	6)
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode 8)
Ambient temperature	T_A	0	70	°C	SAB-XC164…
		-40	85	°C	SAF-XC164…
		-40	125	°C	SAK-XC164…

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP}$ + 0.5 V ($I_{OV} > 0$) or $V_{OV} < V_{SS}$ - 0.5 V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.
Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1.

6) Not subject to production test - verified by design/characterization.

The used mechanism to generate the master clock is selected by register PLLCON.

CPU and EBC are clocked with the CPU clock signal f_{CPU}. The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called “TCP”.

The other peripherals are supplied with the system clock signal f_{SYS} which has the same frequency as the CPU clock signal f_{CPU}.

Bypass Operation

When bypass operation is configured (PLLCTRL = $0x_B$) the master clock is derived from the internal oscillator (input clock signal XTAL1) through the input- and output-prescalers:

$f_{MC} = f_{OSC} / ((PLLIDIV + 1) \times (PLLODIV + 1))$.

If both divider factors are selected as ‘1’ (PLLIDIV = PLLODIV = ‘0’) the frequency of f_{MC} directly follows the frequency of f_{OSC} so the high and low time of f_{MC} is defined by the duty cycle of the input clock f_{OSC}.

The lowest master clock frequency is achieved by selecting the maximum values for both divider factors:

$f_{MC} = f_{OSC} / ((3 + 1) \times (14 + 1)) = f_{OSC} / 60$.

Phase Locked Loop (PLL)

When PLL operation is configured (PLLCTRL = 11_B) the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times$ **F**) which results from the input divider, the multiplication factor, and the output divider (**F** = PLLMUL+1 / (PLLIDIV+1 $\times$ PLLODIV+1)). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC}, the timing must be calculated using the minimum TCP possible under the respective circumstances.
The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 13**).